PM7346

S/UNI™-QJET

SATURN QUAD USER NETWORK INTERFACE FOR J2/E3/T3

TECHNICAL OVERVIEW

PRELIMINARY

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CONTENTS

1 INTRODUCTION

This document provides an overview of PM7346 S/UNI-QJET. Please refer to PMC-960835 S/UNI-QJET Data Sheet for a detailed description of this device.

The S/UNI-QJET is a versatile four-channel device that can be used in cell-based and packet-based applications. Each channel has integrated J2, E3, T3 framers and direct cell-mapped or Physical Layer Convergence Protocol (PLCP) framed ATM cell processors as shown in Figure 1:

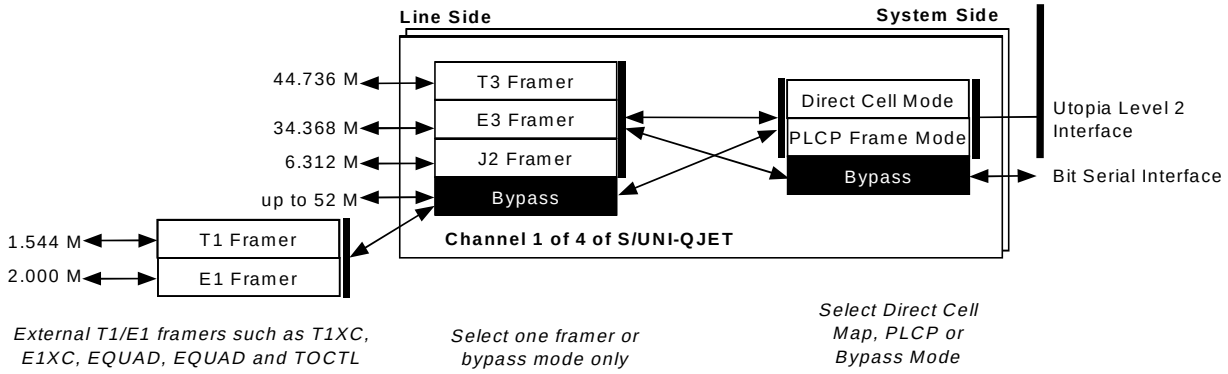

Figure 1: S/UNI-QJET Functional Overview.

The flexibility offered by S/UNI-QJET allows each channel to be independently configured as an ATM physical layer device, as a framer, or as a cell delineation device. As an ATM physical layer device, S/UNI-QJET supports T3, E3 and J2 rates using an internal framer in conjunction with either PLCP-framed or direct cell-mapped ATM cell processor. Other rates, such as T1 and E1, can be supported using external framers such as T1XC, TQUAD, TOCTL, E1XC or EQUAD.

In the receive direction, the ATM cell processor performs cell descrambling, HCS error detection, idle cell filtering, header descrambling and accumulates the number of idle and assigned cells in one second saturating counters. In the transmit direction, the cell processor performs optional ATM cell scrambling, header scrambling, HCS generation and programmable idle cell insertion.

The S/UNI-QJET supports a 50 MHz 8 or 16-bit wide UTOPIA Level 2 compliant interface with parity support and multi-PHY control signals. For each channel, rate decoupling between the line and ATM layer device is provided by a four cell FIFO in transmit and receive directions.

As a quad J2/E3/T3 framer, the S/UNI-QJET can generate gapped transmit and receive clocks to allow for a glueless interface to a data link layer device, such as PM7366 FREEDM-8, that access payload data bits only. The S/UNI-QJET provides integral transmit and receive HDLC controllers, with a deep 128 byte FIFO, to process data link messages carry in the T3 C-bit parity, E3 G.832 or J2 G.704 framing format.

The S/UNI-QJET can be used as a quad ATM cell delineation device when the internal J2/E3/T3 framers are bypassed and only the cell processing blocks are activated. In this mode, each channel of the S/UNI-QJET can individually support cell rates up to 52 Mbit/s.

The available modes are summarized in Table 1:

Table 1: Valid S/UNI-QJET Operational Modes.

Rate	Format	Framer Only	SMDS PLCP Mapping	ATM Direct Mapping
T3 (44.736 Mbit/s)	C-bit Parity	✓	✓	✓
	M23	✓	✓	✓
E3 (34.368 Mbit/s)	G.751	✓	✓	✓
	G.832	✓	n/a	✓
J2 (6.312 Mbit/s)	G.704 & NTT	✓	n/a	✓
E1 (2 Mbit/s)	CRC-4	external	✓	✓
	PCM30	external	✓	✓
T1 (1.544 Mbit/s)	ESF	external	✓	✓
	SF	external	✓	✓
Arbitrary Cell Rate (up to 52 Mbit/s)		bypass	n/a	✓

The S/UNI-QJET provides an 8-bit microprocessor interface for configuration, control, and status monitoring. It supports a standard five signal P1149.1 JTAG test port for boundary scan board test purposes. The SUNI-QJET is implemented using low power 3.3V CMOS technology with 5V tolerant inputs. It is available in a high-density 256 pin Super Ball Grid Array (SBGA) package with a physical dimension of 27mm by 27mm.

2 APPLICATION EXAMPLES

The S/UNI-QJET can be configured as an ATM physical layer device. On the line side, it connects to one or more J2/E3/T3 line interface units and on the system side, the S/UNI-QJET interfaces to the ATM layer device, such as PM7322 RCMP-800, over an 8 or 16 bit wide UTOPIA Level 2 interface (as shown in Figure 2).

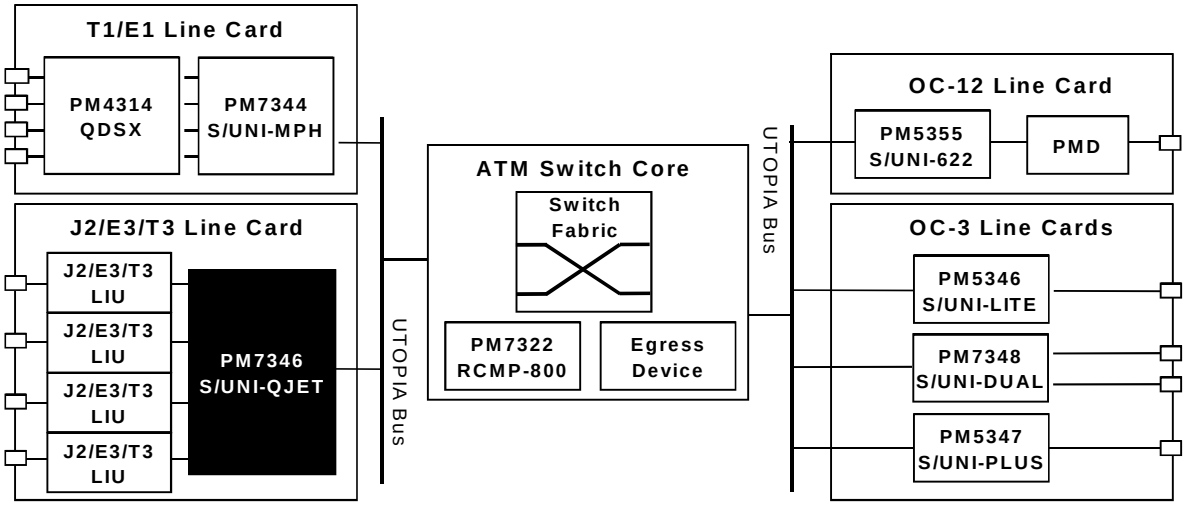

Figure 2: S/UNI-QJET, as an ATM PHY, in an ATM Switch.

S/UNI-QJET can be configured as a quad J2/E3/T3 framer for use in router, frame relay switch and multiplexer applications (as shown in Figure 3). In an unchannelized J2/E3/T3 line card, S/UNI-QJET interfaces directly to one or more PM7366 FREEDM-8 HDLC controllers. Each FREEDM-8 can process two high-speed links, such as T3 and E3, or it can process up to eight lower speed links such as J2. The S/UNI-QJET can gap all the overhead bits such that only the payload data is passed to and from FREEDM-8. On the line side, S/UNI-QJET is connected to one or more J2/E3/T3 line interface units. On the system side, S/UNI-QJET interfaces with a data link device over a serial bit interface.

In a PPP-Over-SONET application, the S/UNI-QJET interfaces to PM5342 SPECTRA-155 to map three T3 data streams onto three corresponding STS-1 services that are collectively carried over an OC-3 link.

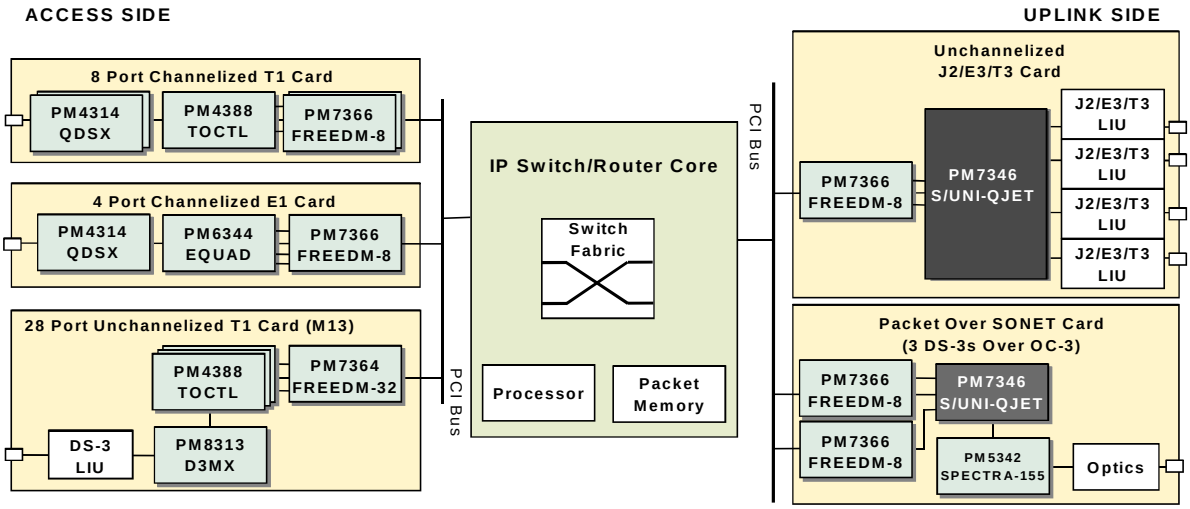

Figure 3: S/UNI-QJET, as a Quad Framer Device, in a Frame Relay Equipment.

The S/UNI-QJET can be configured as a cell processor to provide cell mapping functions for xDSL modems in an ATM based Digital Subscriber Loop Access Multiplexer (DSLAM) equipment. As shown in Figure 4, each S/UNI-QJET provides four cell processors. Two S/UNI-QJETs are required in an 8 port xDSL line card.

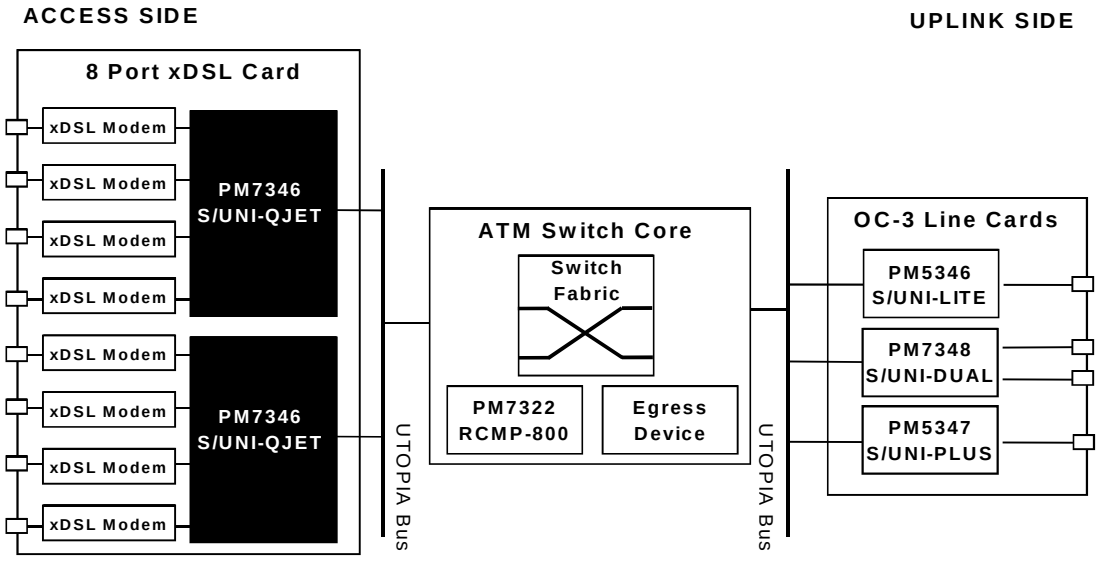

Figure 4: S/UNI-QJET, as a Cell Processor, in a DSLAM Equipment.

3 FUNCTIONAL OVERVIEW

This section describes the major functional blocks of S/UNI-QJET. A simplified block diagram of S/UNI-QJET is show in Figure 5.

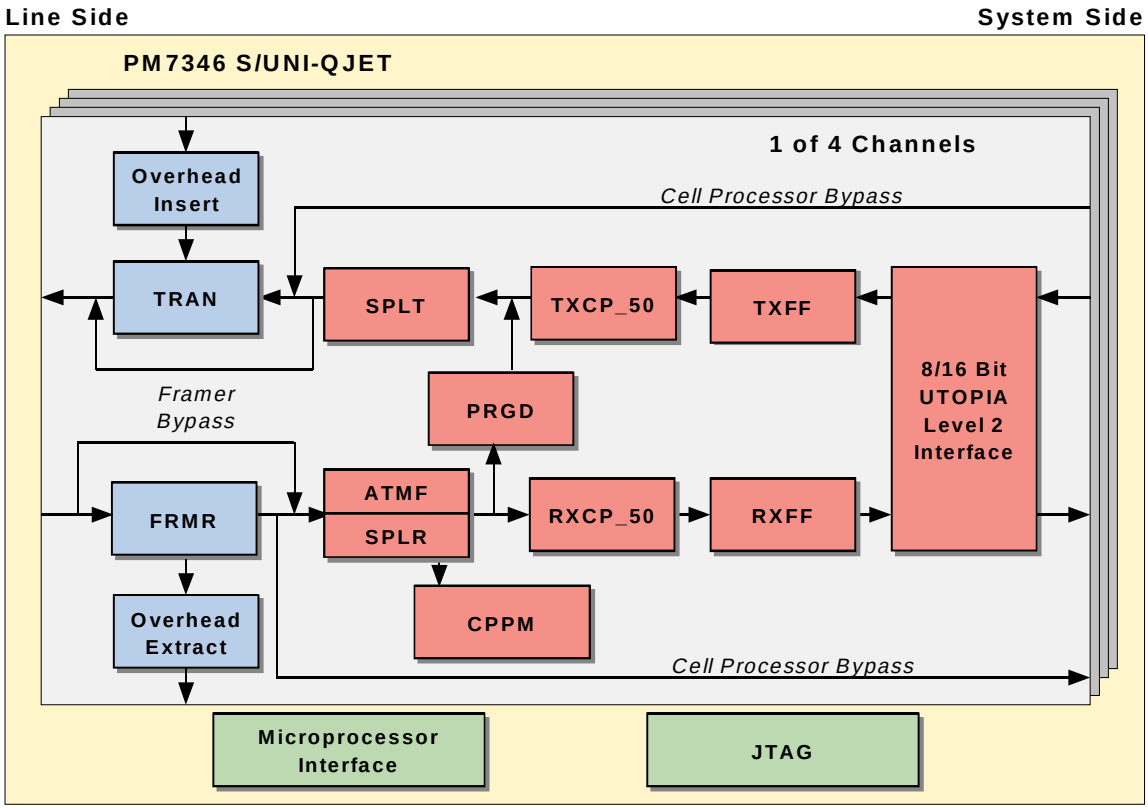

Figure 5: S/UNI-QJET Block Diagram.

3.1 Receive Operation

The steps in the receive operation are summarized below:

Block Name	Functional Overview
FRMR: Receive Framer:	The receive framer consists of three independent framers: • T3-FRMR to decode a T3 frame in either M23 or C-bit parity formats. • E3-FRMR to decode an E3 frame in either G.751 or G.832 formats. • J2-FRMR to decode a J2 frame in either G.704 or NTT formats. The operations of the FRMR are further described in Section 4: J2/E3/T3 framer overview.
Overhead Extract	The Overhead Extract block consists of several sub-blocks that complement the FRMR in performing framer decoding functions: • RBOC: The Bit-Oriented Code Detector is only used in T3 C-bit parity. RBOC detects the presence of 63 of the 64 possible bit-oriented codes contained in the T3 C-bit parity far end alarm and control (FEAC) channel. The 64th code (111111b) is similar to the HDLC flag sequence and is ignored. • RDLC: This block receives LAPD/HDLC frames on any serial HDLC bit stream such as the T3 C-bit parity Path Maintenance Data Link, the E3 G.832 Network Requirement byte or the General Purpose data link, the E3 G.751 Network Use bit, or the J2 m-bit data link. A 128 byte FIFO is provided to buffer the received HDLC messages in between microprocessor accesses. • PMON: The Performance Monitor Accumulator interfaces with FRMR to count framing errors. • Rx O/H Access: Extracts the receive J2/E3/T3 overhead bits on the ROH[x], ROHFP[x], and ROHCLK[x] pins.
ATMF: ATM Cell Delineator	The ATMF block provides HCS-based cell delineation for non-PLCP based transmission formats. This block is described in Section 5: ATM Cell Delineation.
SPLR:	The SPLR block supports DS1, T3, E1 and G.751 E3

Block Name	Functional Overview
PLCP Layer Receiver	PLCP frame processing. This block is described in Section 6: PLCP Frame Processing.
CPPM: Cell and PLCP Performance Monitor	The CPPM block interfaces directly to the SPLR to accumulate PLCP error events: • bit interleaved parity error events, • framing octet error events, • far end block error events.
RCXP_50: Receive Cell Processor	The RXCP_50 block supports optional cell payload unscrambling, optional cell header unscrambling, header check sequence (HCS) verification, idle cell filtering and performance monitoring. For PLCP based systems, cell delineation is performed by the SPLR block. For non-PLCP based systems, cell delineation is performed by the ATMF block.
RXFF: Receive FIFO	The RXFF provides FIFO management and the receive cell interface. The receive FIFO contains four cells and provides the cell rate decoupling function between the transmission system physical layer and the ATM layer. The FIFO interface is UTOPIA Level 2 compliant.

3.2 Transmit Operation

The steps in the transmit operation are summarized below:

Block Name	Functional Overview
TXFF: Transmit FIFO	The TXFF block provides FIFO management and the transmit cell interface. The transmit FIFO contains four cells and provides the cell rate decoupling function between the transmission system physical layer and the ATM layer. The FIFO interface is UTOPIA Level 2 compliant.
TXCP_50: Transmit Cell Processor	The TXCP_50 block supports ATM cell payload scrambling, header check sequence (HCS) generation and idle/unassigned cell generation.
SPLT: SMDS PLCP Layer Transmitter	The SPLT block supports DS1, T3, E1 and G.751 E3 based PLCP frame insertion. This block is described in Section 6: PLCP Frame Processing.
Overhead Insert	The Overhead Insert block consists of several sub-blocks that complement the TRAN in performing frame encode functions: • XBOC: The Bit Oriented Code Generator

Block Name	Functional Overview
	transmit 63 of the possible 64 bit oriented codes (BOC) in the C-bit parity Far End Alarm and Control (FEAC) channel. It can be used to automatically transmit J2 RAI. • TDPR: The Facility Data Link Transmitter provides a serial data link for the C-bit parity path maintenance data link in T3, the serial Network Operator byte or the General Purpose datalink in G.832 E3, the National Use bit datalink in G.751 E3 or the m-bit datalink in J2. • Tx O/H Access: Can be programmed to insert the transmit J2/E3/T3 overhead bits from the TOH[x], TOHFP[x], and TOHCLK[x] pins.
TRAN: Transmit Framer	The transmit framer consists of three independent framers: • T3-TRAN to transmit a T3 frame in either M23 or C-bit parity formats. • E3-TRAN to transmit an E3 frame in either G.751 or G.832 formats. • J2-TRAN to transmit a J2 frame in G.704 and NTT formats. The operations of the TRAN are described in Section 4: J2/E3/T3 framer overview.

3.3 Auxiliary Blocks

Block Name	Functional Overview
PRGD: Pseudo-Random Sequence Generator/Detector	The PRGD block is a software programmable test pattern generator, receive and analyzer that may be used to send and receive pseudo-random binary sequence (PRBS) patterns to and from the transmission line. The PRGD block can be programmed to generate any PRBS with length up to 32 bits or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rate between 10^{-1} to 10^{-7}.
JTAG Test Access Port	The JTAG Test Access Port provides JTAG support for boundary scan purposes. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-QJET

Block Name	Functional Overview
	identification code is 073460CD hexadecimal.
Microprocessor Interface	The microprocessor interface block provides normal and test mode registers and the logic required to connect to a microprocessor. The normal mode registers are required for normal operation and test mode registers are used to enhance the testability of the device.

4 J2/E3/T3 FRAMER OVERVIEW

4.1 T3 Framer Operation

The S/UNI-QJET supports both M23 and C-bit parity T3 framing formats. This format can be extended to support direct byte mapping or PLCP mapping of ATM cells. An overview of the T3 frame format is shown in Figure 6.

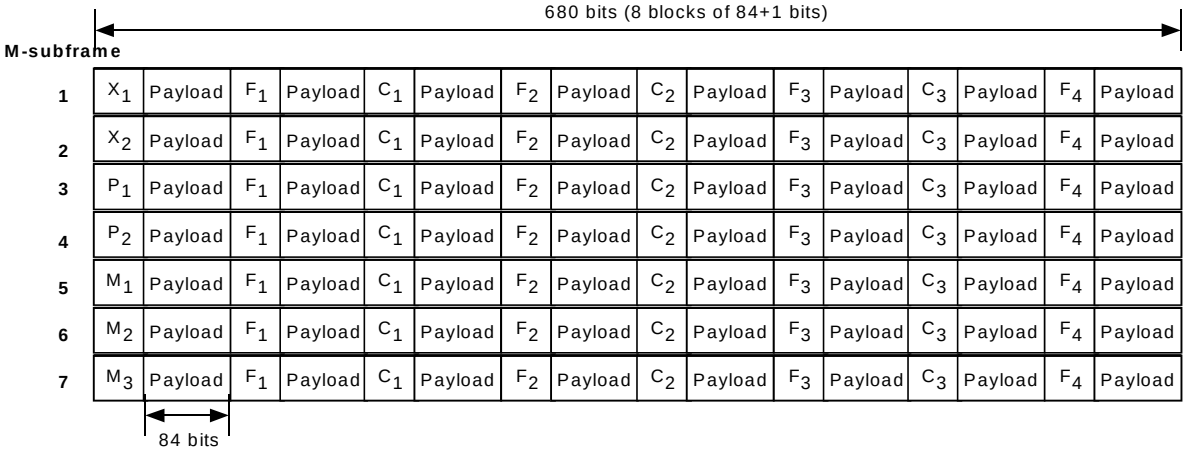

Figure 6: T3 Frame Format.

The T3 receiver decodes a B3ZS-encoded signal and provides indications of line code violations (LCVs). The B3ZS decoding algorithm and the LCV definition are software selectable.

While in-frame, the T3 receiver continuously checks for line code violations, M-bit or F-bit framing bit errors, and P-bit parity errors. When C-bit parity mode is selected, both C-bit parity errors and far end block errors are accumulated.

When the C-bit parity framing format is detected, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted. HDLC messages in the Path Maintenance Data Link are received by an internal data link receiver.

The T3 transmitter allows for the insertion of the overhead bits into a T3 bit stream and produces a B3ZS-encoded signal. Status signals such as far end receive failure (FERF), the alarm indication signal (AIS) and the idle signal can be inserted when the transmission of these signals is enabled

The processing of the overhead bits in the T3 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream.

Control Bit	Transmit Operation	Receive Operation
Xx: X-Bit Channel	Inserts the FERF signal on the X-bits.	Monitors and detects changes in the state of the FERF signal on the X-bits.
Px: P-Bit Channel	Calculates the parity for the payload data over the previous M-frame and inserts it into the P1 and P2 bit positions.	Calculates the parity for the received payload. Errors are accumulated in internal registers.
Mx: M-Frame Alignment Signal	Generates the M-frame alignment signal (M1=0, M2=1, M3=0).	Finds the M-frame alignment by searching for the F-bits and the M-bits. Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Fx: M-subframe Alignment Signal	Generates the M-subframe signal (F1=1, F2=0, F3=0, F4=1).	Finds M-frame alignment by searching for the F-bits and the M-bits. Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Cx: C-Bit Channels	<u>M23 Operation:</u> The C bits are passed through transparently in M23 framer only mode except for the C-bit Parity ID bit which toggles every M-frame. <u>C-bit Parity Operation:</u> The C-bit Parity ID bit is forced to logic 1. The second C-bit in M-subframe 1 is set to logic 1. The third C-bit in M-subframe 1 provides a far-end alarm and control (FEAC) signal. The FEAC	The state of the C-bit parity ID bit is stored in a register. This bit indicates whether an M23 or C-bit parity format is received. <u>C-bit Parity Operation:</u> The FEAC channel on the third C-bit in M-subframe 1 is detected by the RBOC block. Path parity errors and FEBEs on the C-bits in M-subframes 3 and 4 are accumulated in counters. The path maintenance datalink signal is extracted by the receive HDLC controller.

Control Bit	Transmit Operation	Receive Operation
	channel is sourced by the XBOC block. The 3 C-bits in M-subframe 3 carry path parity information. The value of these 3 C-bits is the same as that of the P-bits. The 3 C-bits in M-subframe 4 are the FEBE bits. The 3 C-bits in M-subframe 5 contain the 28.2 Kbit/s path maintenance datalink. The remaining C-bits are unused and set to logic 1.	

4.2 E3 Framer Operation

The E3 framer decodes an HDB3-encoded signal and frames to the E3 bit stream. The E3 framer supports both G.751 and G.832 frame formats.

The E3 Framer searches for frame alignment in the incoming serial stream based on G.751 or G.832 format. For the G.751 format, the E3 framer expects to see the correct framing pattern error-free for three consecutive frames before declaring an in-frame condition. For the G.832 format, the E3 framer expects to see the correct framing pattern error free for two consecutive frames before declaring an in-frame condition. Once the frame alignment is established, the incoming data is continuously monitored for framing bit errors and byte interleaved parity errors (in G.832 format).

The E3 transmitter generates the frame alignment signal and inserts it into the incoming serial stream based on G.751 or G.832 format. All overhead and status bits in each frame format can be individually controlled by register bits or by transmit overhead insertion pins.

4.2.1 G.751 E3 Framer Operation

The S/UNI-QJET provides support for the G.751 E3 frame format. This format can be extended to allow for direct byte mapping or PLCP mapping of ATM cells. The G.751 E3 frame format is shown in Figure 7.

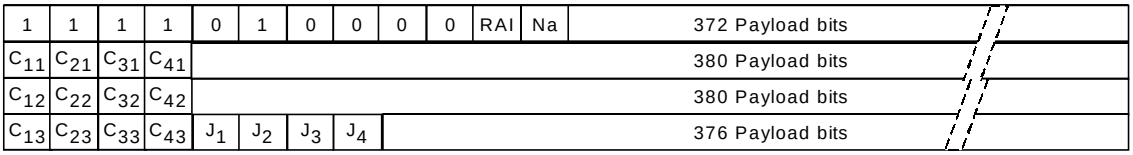

Figure 7: G.751 E3 Frame Fromat

The processing of the overhead bits in the G.751 E3 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream.

Control Bit	Transmit Operation	Receive Operation
Frame Alignment Signal	Inserts the frame alignment signal 1111010000b.	Finds frame alignment by searching for the frame alignment signal. When the pattern has been detected for three consecutive frames, an in-frame condition is declared. When errors are detected in four consecutive frames, an out-of-frame condition is declared.
RAI: Remote Alarm Indication	Optionally asserts the RAI signal under a register control or when LOS, OOF, AIS and LCD conditions are detected.	Extracts the RAI signal and outputs it on the ROH output pin. The state of the RAI signal is also written to a register bit.
Na: National Use Bit	Asserts the National Use bit under a register control or from the internal HDLC controller.	Extracts the National Use bit and stores the value in a register bit.
Cjk: Justification Service Bits	When the device is configured as an E3 G.751 framer device, the Justification Service Bits can be inserted on the TDATI[x] input pin the same way as normal payload data. When the device is configured for ATM application, the Justification Service Bits are used as payload bits.	Extracts the Justification Service Bits on the ROH output pin when the Cjk bits are configured as overhead.
Jk: Tributary	When the device is	Extracts the Tributary Justification

Control Bit	Transmit Operation	Receive Operation
Justification Bits	configured as a E3 G.751 framer, the Tributary Justification Bits can be inserted on the TDATI[x] input pin the same way as normal payload data. When the device is configured for ATM application, the Tributary Justification Bits are used a payload bits.	Bits on the ROH output pin when the Pk bits are configured as overhead.

4.2.2 G.832 E3 Framer Operation

The S/UNI-QJET provides support for the G.832 E3 frame format. This format can be extended to allow for direct byte mapping or PLCP mapping of ATM cells. The G.832 E3 frame format is shown in Figure 8.

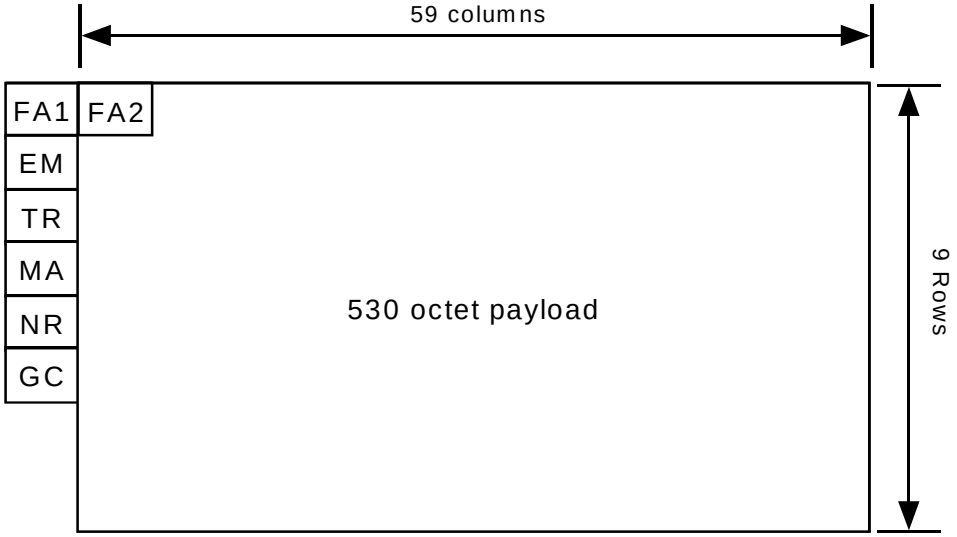

Figure 8: G.832 E3 Overhead Processing

The processing of the overhead bits in the G.832 E3 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream.

Control	Transmit Operation	Receive Operation
FA1, FA2: Frame Alignment Pattern	Inserts the G.832 E3 frame alignment pattern (F628H).	Searches the receive stream for the G.832 E3 frame alignment pattern. When the pattern is detected for two consecutive frames, an in-frame condition is declared. Note that there is no ATM cell alignment with the G.832 E3 frame. Therefore cell delineation must be performed to locate the ATM cell boundaries.
EM: Error Monitor, BIP-8	Inserts the calculated BIP-8 by computing even parity over all transmit bits, including the overhead bits of the previous 125 µs frame.	Computes the incoming BIP-8 value over one 125 µs frame. The result is held and compared against the value in the EM byte of the subsequent frame.
TR: Trail Trace	Inserts the 16 byte trail access point identifier specified in internal registers.	Extracts the repetitive trail access point identifier and verifies that the same pattern is received. Compares the received pattern to the expected pattern programmed in a register.
MA: Maintenance and Adaptation Byte	Inserts the FERF, FEBE, Payload Type bits, Tributary Unit Multiframe Indicator bits and the Timing Marker bit as programmed in a register or as indicated by detection of receive OOF or BIP-8 errors.	Extracts and reports the FERF bit value when it has been the same for 3 or 5 consecutive frames. S/UNI-QJET also extracts and accumulates FEBE occurrences and extracts the Payload Type, Tributary Unit Multiframe, and Timing Market indicator bits and reports them through microprocessor accessible registers.
NR: Network Operator Byte	Inserts the Network Operator byte from the TOH overhead stream or optionally from the TDPR. When not configured for Tandem Connection Maintenance, all 8 bits of the Network Operator byte are inserted from TOH or from the TDPR.	Extracts the Network Operator byte and outputs it on ROH or optionally terminates it in the RDLC. When not configured for Tandem Connection Maintenance, all 8 bits of the Network Operator byte are extracted and presented on ROH or to the RDLC.
GC:	Inserts the GC byte from the	Extracts the GC byte and outputs it

Control	Transmit Operation	Receive Operation
General Purpose Communication Channel	TOH overhead stream or optionally from the TDPR block.	on ROH or optionally terminates it in the RDLC block.

4.3 J2 Framer Operation

The S/UNI-QJET supports the G.704 and NTT J2 frame format. This format can be extended to allow for direct byte mapping of ATM cells as specified in G.804. The J2 format consists of 789 bit frames each 125 µs long, consisting of 96 bytes of payload, 2 reserved bytes and 5 F-bits. The frames are grouped into 4 frame multiframes as shown in Figure 9.

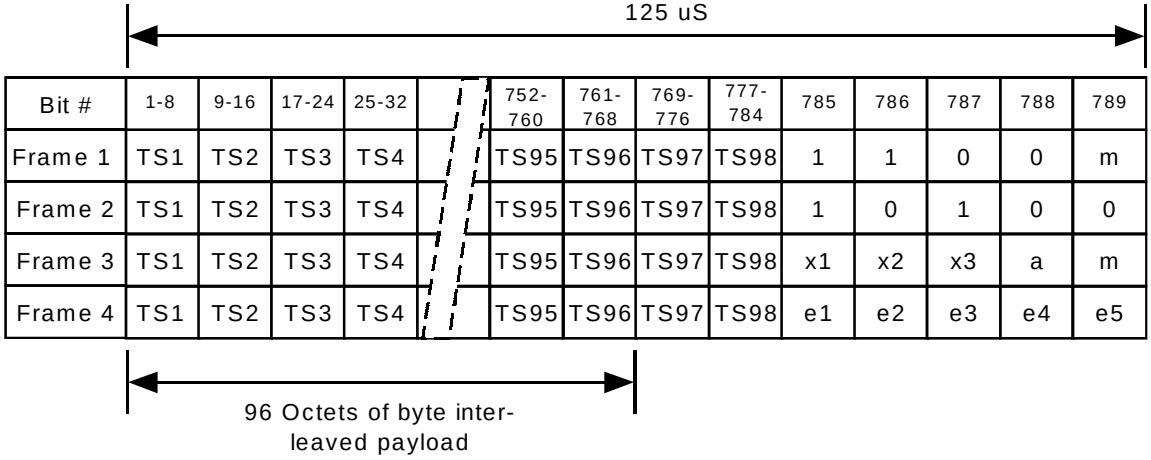

Figure 9: G.704 J2 Frame Format

The J2 framer decodes a unipolar or B8ZS encoded signal and frames to the resulting 6,312 Kbit/s J2 bit stream. Once in frame, the J2 framer provides indications of frame and multiframe boundaries and marks overhead bits, x-bits, m-bits and reserved channels (TS97 and TS98). Indications of loss of signal, bipolar violations, excessive zeroes, change of frame alignment, framing errors, and CRC errors are provided and accumulated in internal counters.

The J2 transmitter inserts the overhead bits into a J2 bit stream and produces a B8ZS-encoded signal. The J2 transmitter adheres to the framing format specified in G.704 and NTT Technical Reference for High Speed Digital Leased Circuit Services.

The processing of the overhead bits in the J2 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream.

Control	Transmit Operation	Receive Operation
TS1-TS96: Byte Interleaved Payload	Inserts the ATM cells into TS1 to TS96 octets.	Extracts the ATM cell octet payload and performs cell delineation.
TS97-TS98: Signaling channels	Inserts the signaling bytes from either register bits or from the TOH and TOHINS inputs. These bits can be optionally inserted via TDATI input when in framer only mode.	Extracts signaling bytes on the ROH output.
Frame Alignment Signal	Inserts the frame alignment signal automatically.	Finds J2 frame alignment by searching for the frame alignment signal.
M-bits: 4kHz Data Link	Inserts the 4 KHz data link signal from the internal HDLC controller or from the bit oriented code generator.	Extracts the 4 KHz data link signal for the internal HDLC controller.
X-bits: Spare Bits	Inserts the spare bits via register bits or via TOH and TOHINS input pins.	Extracts and presents the x-bits on register bits. The X-bit states can be debounced and presented on the ROH output pin. An interrupt change can be generated to signal a change in the X-bit state.
A-bit: Remote Loss of Frame Indication	Inserts the A-bit via register bit. The A-bit can be optionally be asserted when the J2 framer is in loss of frame condition.	Extracts and presents the A-bit on a register bit. The A-bit state can be debounced and presented on the ROH output pin. An interrupt can be generated to signal a change in the A-bit state.
E1-E5: CRC-5 Check Sequence	Automatically calculates and inserts the CRC-5 check sequence.	Calculates the CRC-5 check sequence for the received data stream. Discrepancies with the received CRC-5 code can be configured to generate an interrupt. CRC-5 errors are accumulated in an internal counter.

5 ATM CELL DELINEATION

The S/UNI-QJET's ATM Cell Delinator (ATMF) block performs header check sequence (HCS) based cell delineation for non-PLCP based transmission formats. The ATMF block accepts a bit serial cell stream and performs cell delineation to locate cell boundaries.

Cell delineation is the process of framing to ATM cell boundaries using the HCS field in the ATM cell header as shown in Figure 10. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation correct HCS calculations are assumed to indicate cell boundaries.

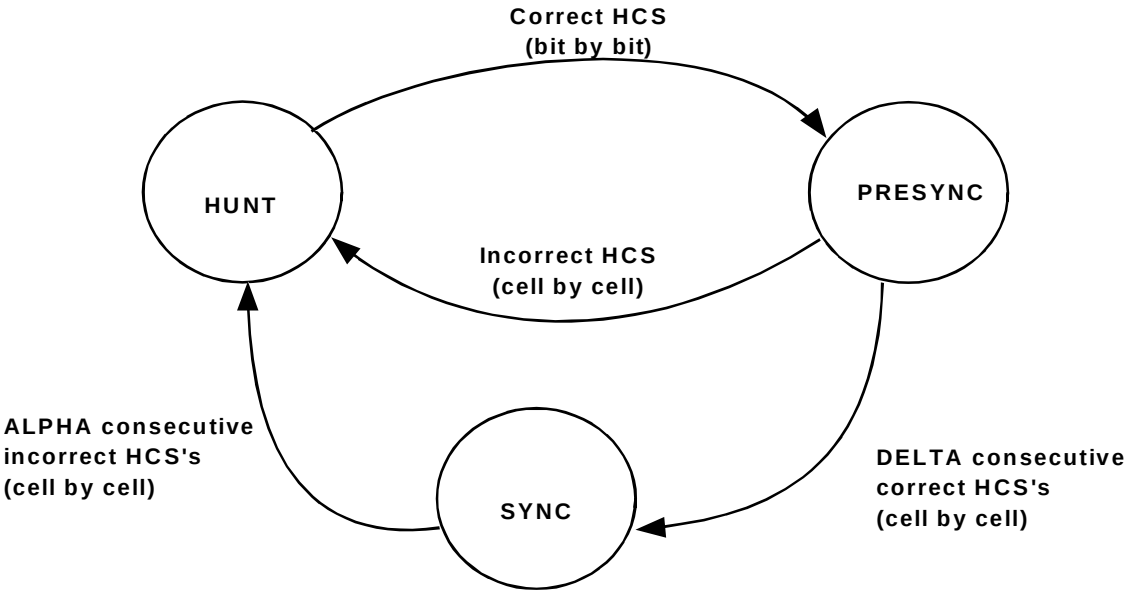

Figure 10: Cell delineation State Diagram..

The ATMF performs a sequential bit-by-bit, nibble-by-nibble (for T3 direct mapped) or a byte-by-byte (J2 and E3 direct mapped) hunt for a correct HCS sequence. This state is referred to as the HUNT state. When receiving a bit serial cell stream from an upstream transmission system, the bit, nibble or byte boundaries are determined from the location of the overhead.

When a correct HCS is found, the ATMF locks on the particular cell boundary and assumes the PRESYNC state. This state verifies that the previously detected HCS pattern was not a false indication. If the HCS pattern was a false indication then an incorrect HCS should be received within the next DELTA cells. At that point a transition back to the HUNT state is executed. If an incorrect HCS is not found in this PRESYNC period then a transition to the SYNC state is

made. In this state synchronization is not relinquished until ALPHA consecutive incorrect HCS patterns are found. In such an event a transition is made back to the HUNT state

The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6 as recommended in ITU-T Recommendation I.432. These values result in a maximum average time to frame of 127 µs for a T3 stream carrying ATM cells directly mapped into the T3 information payload.

Loss of cell delineation (LCD) is detected by counting the number of incorrect cells while in the HUNT state. The count value which determines when LCD is declared can be set in an internal register.

6 PLCP FRAME PROCESSING

The S/UNI-QJET provides support for four different PLCP frame formats:

- T3 PLCP frame format,
- DS1 PLCP frame format,
- G.751 E3 PLCP frame format,
- E1 PLCP frame format.

6.1 T3 PLCP Frame Format

The T3 PLCP frame (as shown in Figure 11) provides the transmission of 12 ATM cells every 125 µs. The PLCP frame is nibble aligned to the overhead bits in the T3 frame. There is no relationship between the start of the PLCP frame and the start of the T3 M-frame. A trailer is inserted at the end of each PLCP frame. The number of nibbles inserted (13 or 14) varies continuously such that the resulting PLCP frame rate can be locked on to an 8 kHz reference clock.

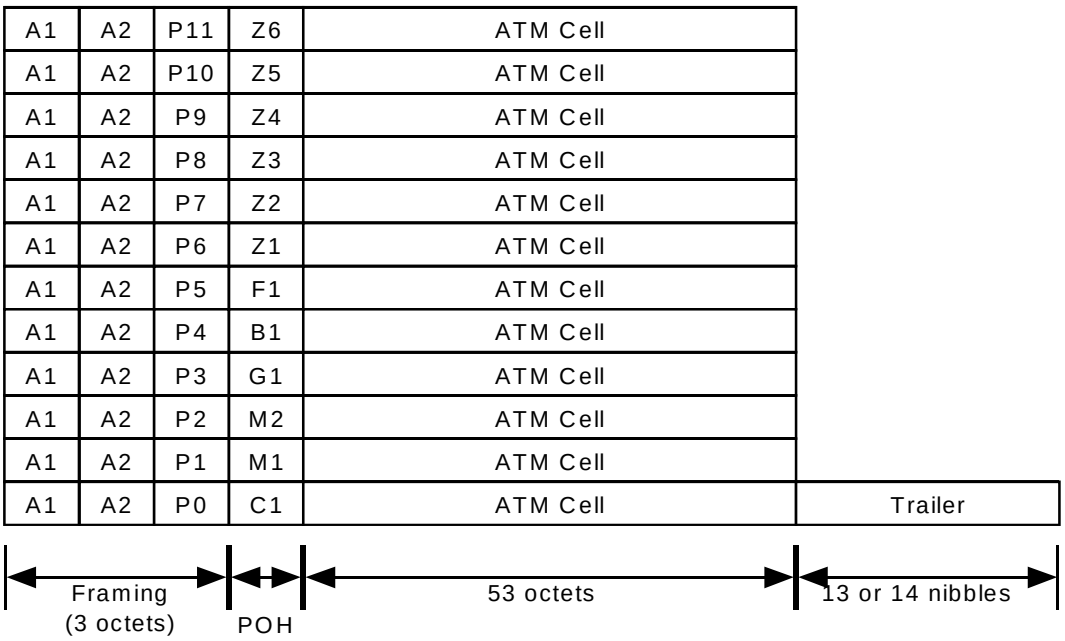

Figure 11: T3 PLCP Frame Format (with a Frame Rate of 125 µs).

6.2 DS1 PLCP Frame Format

The DS1 PLCP frame provides the transmission of 10 ATM cells every 3 ms. The PLCP frame (as shown in Figure 12) is octet aligned to the framing bit in the DS1 frame. There is no relationship between the start of the PLCP frame and the start of the DS1 frame. A trailer is inserted at the end of each PLCP frame. The number of octets inserted is fixed at six.

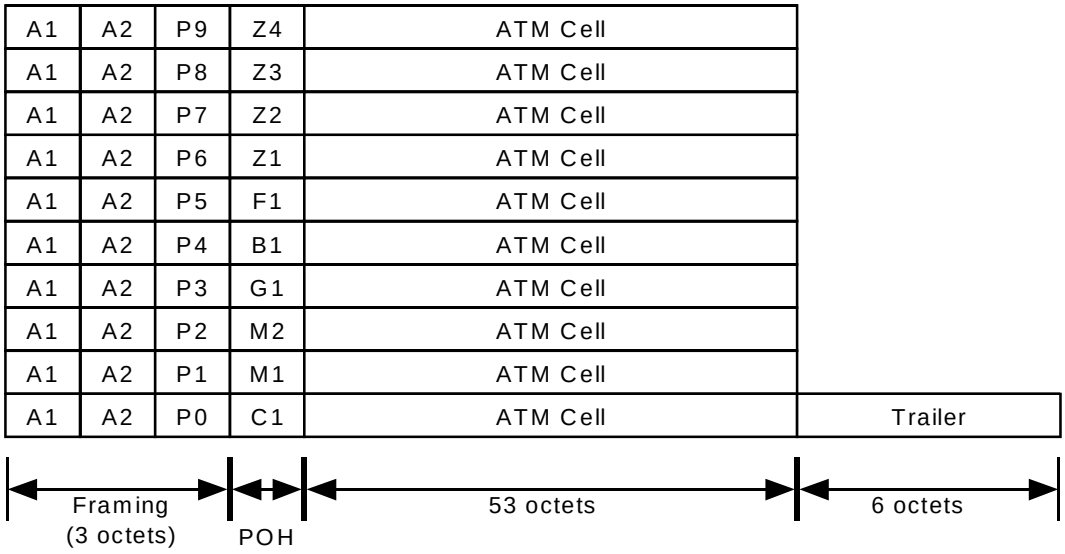

Figure 12: DS1 PLCP Frame Format (with a Frame Rate of 3 ms).

6.3 G.751 E3 PLCP Frame Format

The G.751 E3 PLCP frame provides the transmission of 9 ATM cells every 125 µs. The PLCP frame (as shown in Figure 13) is octet aligned to the 16 overhead bits in the G.751 E3 frame. There is no relationship between the start of the PLCP frame and the start of the E3 frame. A trailer is inserted at the end of each PLCP frame. The number of octets inserted is nominally 18, 19, or 20 and is based on the number of E3 overhead octets (4, 5 or 6) that have been inserted during the PLCP frame period. The nominal octet stuffing can be varied by ±1 octet to allow the E3 PLCP frame to be locked to an external 8 KHz reference clock. Thus the trailer can be 17, 18, 19, 20 or 21 octets in length.

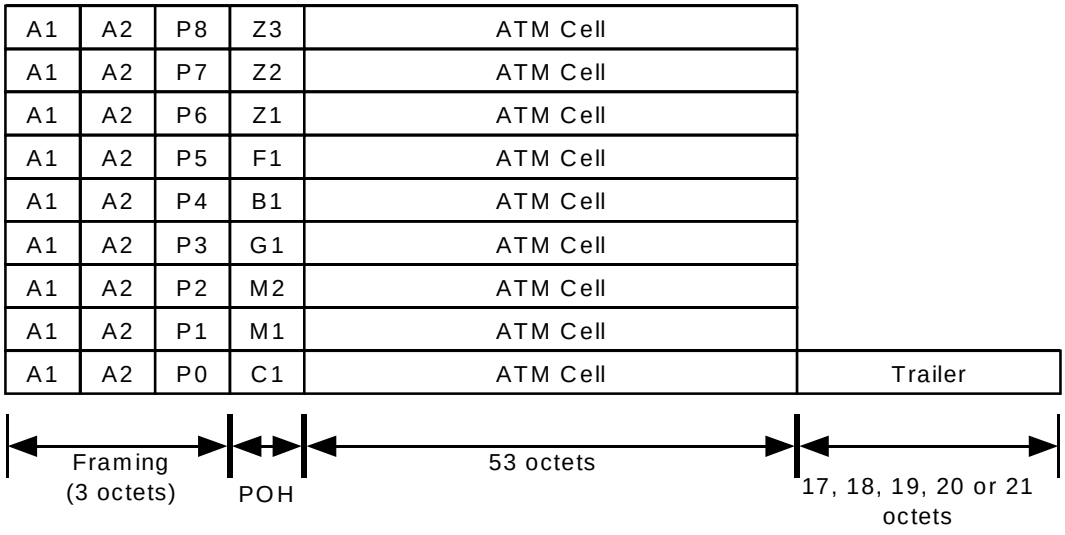

Figure 13: G.751 E3 PLCP Frame Format (with a Frame Rate of 125 µs).

6.4 E1 PLCP Frame Format

The E1 PLCP frame provides the transmission of 10 ATM cells every 2.375 ms. Thirty of the thirty-two available E1 channels are used for transporting the PLCP frame (as shown in Figure 14). The remaining two channels are reserved for E1 framing and signaling functions. The PLCP frame is octet aligned to the channel boundaries in the E1 frame. The PLCP frame is aligned to the 125 µs E1 frame (the A1 octet of the first row of the PLCP frame is inserted in timeslot 1 of the E1 frame).

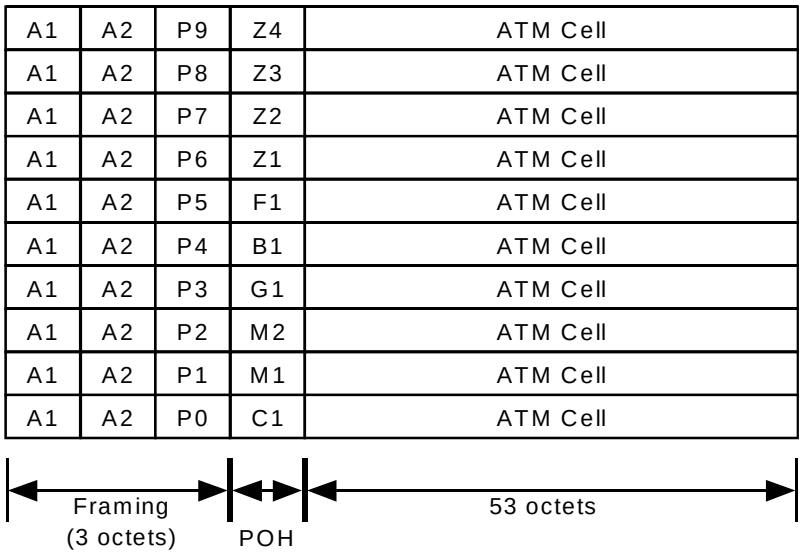

Figure 14: E1 PLCP Frame Format (with a frame rate of 2.375 ms).

6.5 PLCP Overhead Processing

Table 2: PLCP Overhead Processing

Overhead Field	Transmit Operation	Receive Operation
A1, A2: Frame Alignment Pattern	Inserts the PLCP frame alignment pattern (F628H)	Searches the receive stream for the PLCP frame alignment pattern.
PO-P11: Path Overhead Identifier	Inserts the path overhead identifier codes in accordance with the PLCP frame alignment.	Identifies the PLCP path overhead bytes by monitoring the sequence of the POI bytes.
Z1-Z6: Growth:	These octets are unused and are nominally programmed with all zeros. Access to these octets is provided by the PLCP transmit overhead access port.	These octets are ignored and are extracted on the RPOH pin.
F1: User Channel	This octet is unused and the value inserted in this octet is controlled by an internal register or by TPOH pin.	This octet is ignored and is extracted on the RPOH pin.
B1: Bit Interleaved Parity	This octet contains an 8-bit interleaved parity (BIP) calculated across the entire PLCP frame (excluding the A1, A, Pn octets and the trailer). The B1 value is calculated based on even parity and the value inserted in the current frame is the BIP result calculated for the previous frame.	The bit interleaved parity is calculated for the current frame and stored. The B1 octet contained in the subsequent frame is extracted and compared against the calculated value. Differences between the two values provide an indication of the end-to-end bit error rate. These differences are accumulated in an internal counter.
G1: Path Status	The first four bit positions provide a PLCP far end block error function and indicates the number of B1 errors detected at the near end. The FEBE field has nine legal values (0000b-1000b) indicating between zero and eight B1 errors.	The G1 byte provides the PLCP FEBE function and is accumulated in an internal counter. PLCP yellow alarm is detected or removed when the yellow bit is set to logic one or zero for ten consecutive frames. The yellow alarm state and the link status signal state are contained in an

Overhead Field	Transmit Operation	Receive Operation
	The fifth bit position is used to transmit PLCP yellow alarm. The last three bit positions provide the link status signal used in IEEE-802.6 DQDB implementations. Yellow alarm and link status signal insertion is controlled by the internal registers or by TPOH pin.	internal register.
M1, M2: Control Information	These octets carry the DQDB layer management information. Internal register controls the nominal value inserted in these octets. These octets are unused in ATM Forum T3 UNI specification and should be programmed with all zeros.	These octets are ignored and are extracted on the RPOH pin.
C1: Cycle/Stuff Counter	The coding of this octet depends on the PLCP frame format. For DS1 and E3 PLCP formats, this octet is programmed with all zeros. For the T3 PLCP format, this octet indicates the number of stuff nibbles (13 or 14) at the end of each PLCP frame. The C1 value is varied in a three frame cycle where the first frame always contains 13 stuff nibbles, the second frame always contains 14 nibbles, and the third frame contains 13 or 14 nibbles. For the G.751 E3 PLCP format, this octet indicates the number of stuff octets (17 to 21) at the end of the PLCP frame. Depending on the alignment of the G.751 E3	Interprets the trailer length according to the selected PLCP frame format and the received C1 code.

Overhead Field	Transmit Operation	Receive Operation
	frame to the E3 PLCP frame, 18, 19 or 20 octets are nominally stuffed. The stuffing may be varied by ±1 octet so that the PLCP frame rate can be locked to an external 8 KHz timing reference.	

NOTES

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