PM4388
TOCTL

TECHNICAL OVERVIEW

May, 1997

Issue 2

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OVERVIEW

The PM4388 TOCTL is a feature-rich octal T1 framer ideal for data communication equipment requiring high density T1 line interfaces. This document provides an overview of the TOCTL. A complete description of this device is contained in PMC-960840, *Octal T1 Framer Datasheet*.

The TOCTL integrates eight T1 framers in a single device to terminate eight duplex T1 signals. Each of the eight T1 framers can be independently configured, monitored and controlled in software. Device drivers written for T1XC and TQUAD can be easily ported to work with TOCTL. The TOCTL is PMC-Sierra's third generation T1 framer following the successful leads of PM4341 T1XC and PM4344 TQUAD.

The TOCTL is implemented using low power 3.3V CMOS technology to minimize power consumption. It has 5V tolerant inputs to interface with 5V devices. To allow for a dramatic increase in board level density, the TOCTL is packaged in a 128 pin PQFP with a physical dimension of 14 mm by 20mm.

A simplified TOCTL block diagram is shown in Figure 1. On the line side, the TOCTL provides jitter attenuation in both the receive and transmit directions. Each framer can be configured to process DS1 data stream in superframe (SF), extended superframe[1] (ESF) or in bypass format. On the system side, the TOCTL supports several timing modes to seamlessly interface to an HDLC controller or a system backplane.

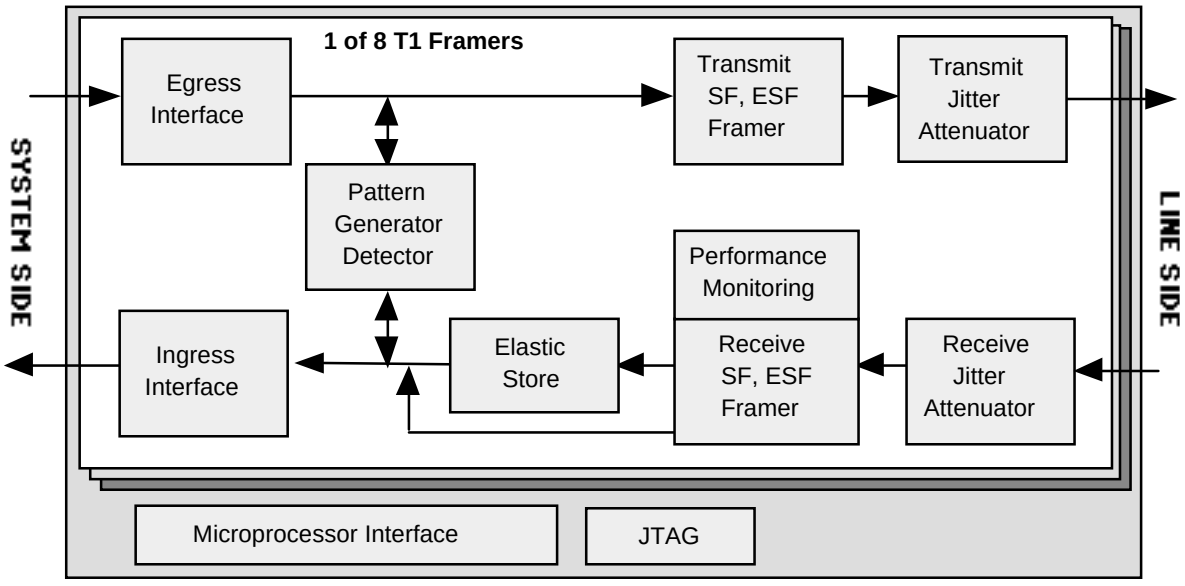

Figure 1. A simplified TOCTL Block Diagram

[1]The 12-frame SF format and the 24-frame ESF format are specified in ANSI T1.107-1995.

APPLICATION EXAMPLES

The TOCTL is ideal for Internet Access Equipment aggregating large numbers of T1 lines. On the line side, it can interface to T1 line interface units (LIUs) or 28 T1s can be multiplexed/demultiplexed onto a T3 facility using an M13 scheme as shown in Figure 2. Internet access product manufacturers will be able to use the TOCTL to achieve greater than 50% savings in board space and greater than 50% reduction in power while improving product reliability over less integrated solutions.

On the system side, the TOCTL can interface directly to a high density HDLC controller to terminate data encapsulated in HDLC protocol. The TOCTL supports transfer of PCM data to and from 1.544 Mbit/s or 2.048 Mbit/s backplane buses and supports fractional T1 backplane interface with asymmetric transmit/receive N*DS0 rates.

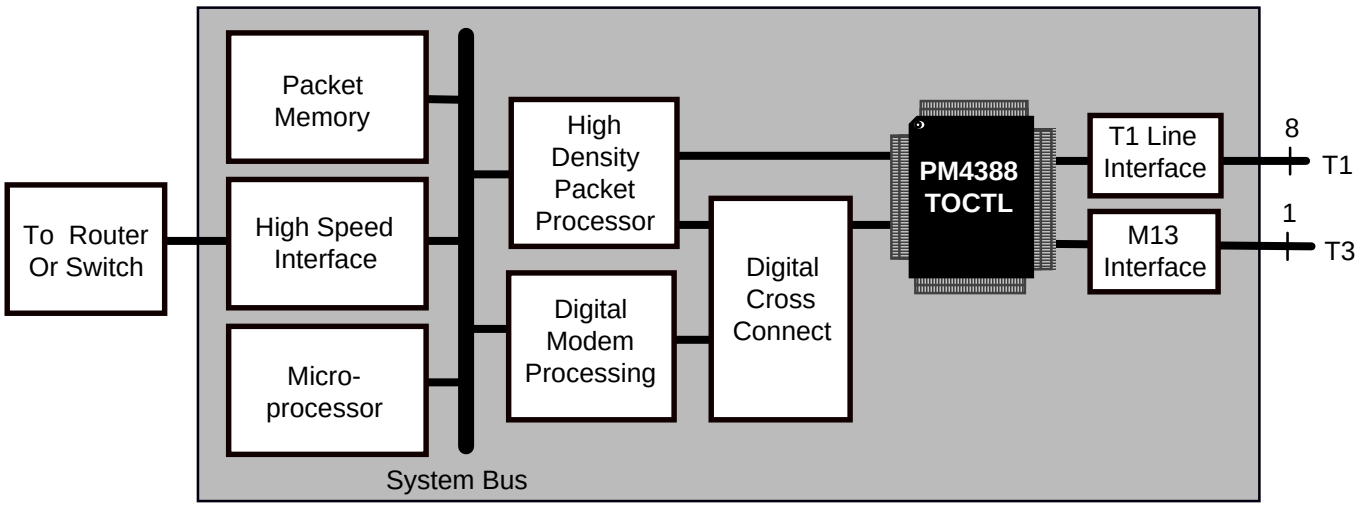

Figure 2: TOCTL in a Typical Internet Access Equipment Architecture.

The TOCTL can seamlessly interface to two PM4314 QDSX to support eight T1 links as shown in Figure 3. The QDSX integrates four full-featured T1/E1 duplex DSX-1 compatible line interface circuits in a single device. The QDSX is currently in production and is packaged in a 128 PQFP. A complete information on the QDSX is contained in PMC-950847, *QUAD T1/E1 Line Interface Device Telecom Standard Product Datasheet.*

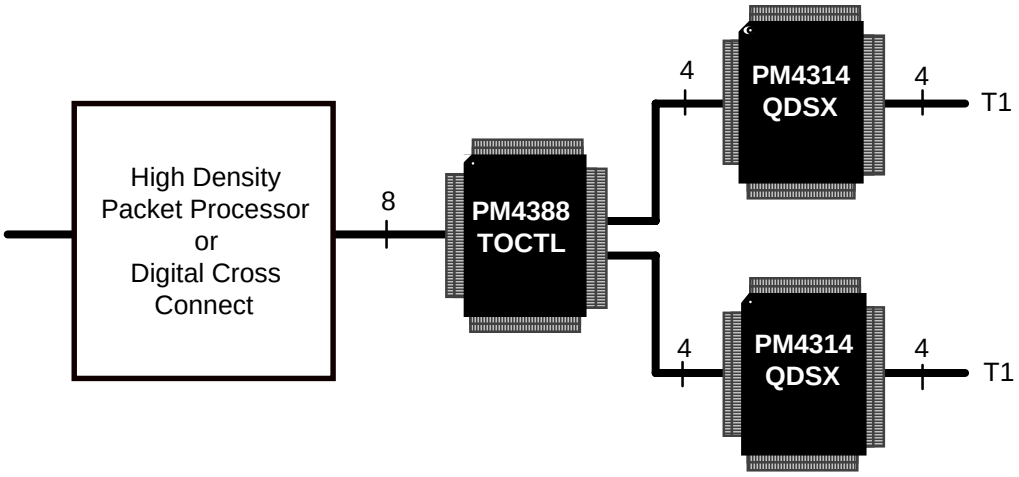

Figure 3: 8 Channel T1 Interface for Frame Relay or Internet Access Equipment.

Four TOCTLS can be used with one PM8313 D3MX to implement an M13 scheme as shown in Figure 4. The D3MX integrates a complete M13 multiplexer/demultiplexer in a single device. On the receive side, the D3MX demultiplexes 28 T1 lines from a T3 link. The 28 T1 lines are terminated using the four TOCTLs. On the transmit side, the D3MX multiplexes 28 T1 lines onto a T3 facility. The D3MX is currently in production and is packaged in a 208 pin PQFP package. A complete information on D3MX is contained in PMC-920702, *M13 Multiplexer Telecom Standard Product Datasheet*.

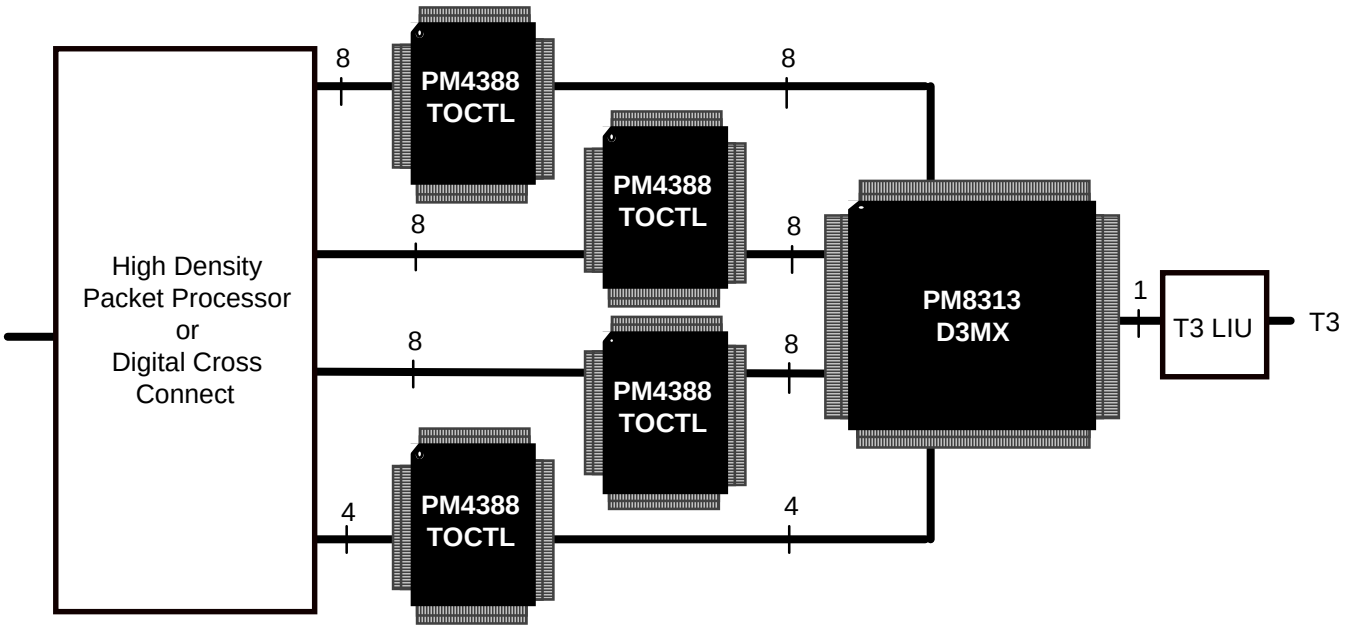

Figure 4: M13 Interface using D3MX and 4 TOCTLs.

FUNCTIONAL DESCRIPTION

Transmit and Receive Jitter Attenuators

Each framer in the TOCTL contains two separate jitter attenuators: one between the receive line data and the ingress interface and the other between the egress interface and the transmit line data. Each digital jitter attenuator provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. These jitter attenuators meet the transfer requirements of AT&T TR-62411, ANSI T1.408 and ANSI T1.403 specifications.

Transmit and Receive Framers

In the receive direction, the TOCTL examines the incoming data to establish synchronization with the selected framing format. If enabled, robbed-bit signals are extracted from the appropriate channels and can be provided via a serial stream on the *ingress signaling* (ISIG[x]) pin or via software access by the external microprocessor. The TOCTL provides user control over signaling freezing, signaling bit fixing and signaling debounce on a per-DS0 basis.

The TOCTL indicates the presence or absence of the Yellow, Red and AIS alarm conditions. This allows an external microprocessor to integrate the alarm conditions using any system specific algorithm. The TOCTL has a built-in alarm integrator compatible with ANSI T1.403 and TR-TSY-00191.

In the transmit direction, the TOCTL inserts SF or ESF framing and datalink information into the 1.544 Mbit/s stream. Frame insertion may optionally be bypassed. The framer provides per-DS0 control over zero-code supression (GTE, Bell or Jammed-Bit-8), idle code insertion, sign and data inversion, digital milliwatt code and robbed-bit signaling.

The TOCTL supports the per-DS0 insertion and detection of pseudo-random or repetitive patterns. It can generate and detect inband loopback code sequences in either framed or unframed data streams. The TOCTL provides three loopback modes to assist in network and system diagnostics:

- line loopback,
- diagnostic digital loopback,
- per-DS0 loopback.

Ingress Interface

The TOCTL's ingress interface allows the received line data to be presented to the system using one of four possible modes:

- Clock Master: Full DS1
- Clock Master : NxDS0
- Clock Slave: ICLK Reference
- Clock Slave: External Signaling

1) Clock Master: Full DS1

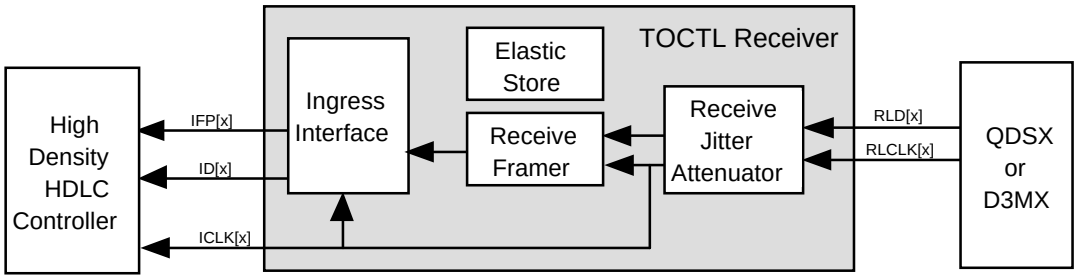

Figure 5: Ingress Clock Master: Full DS1 Mode.

In *Clock Master: Full DS1* mode, each recovered T1 *receive line data* (RLD[x]) is passed through the receive jitter attenuator and the receive framer using the *receive line clock* (RLCLK[x]). Minimal transmission delay is incurred on the data stream as the elastic store is bypassed.

The received data appears on *ingress data* (ID[x]) timed to the *ingress clock* (ICLK[x]). ICLK[x] is a jitter attenuated version of the RLCLK[x]. The ingress frame alignment is indicated by the *ingress frame pulse* (IFP[x]) signal.

2) Clock Master: NxDS0.

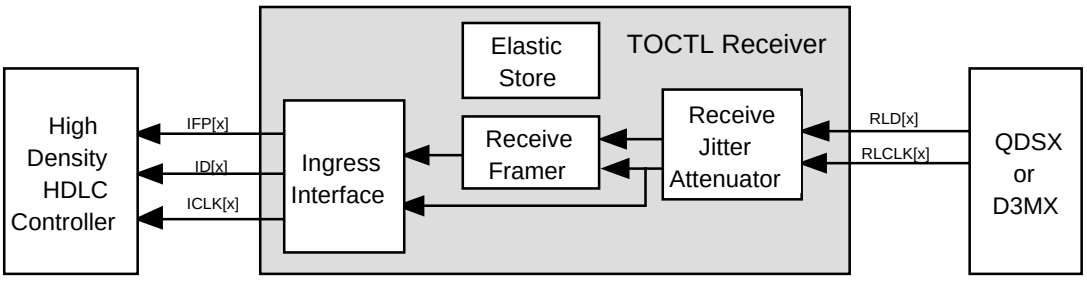

Figure 6: Ingress Clock Master: NxDS0 mode.

In *Clock Master: NxDS0* mode, ICLK[x] is derived from RLCLK[x], and is gapped on a per-DS0 basis so that a subset of the 24 channels in the T1 frame is extracted on ID[x]. The framing bit position is always gapped, so the number of ICLK[x] pulses is controllable from 0 to 192 pulses per frame on a per-DS0 basis.

If all 24 channels in the T1 frame is extracted, this mode is similar to the *Clock Master: Full DS1* mode. However instead of requiring an IFP[x] signal to indicate the frame alignment, the gapped period of the ICLK[x] can be used for the same purpose.

3) Clock Slave: ICLK Reference

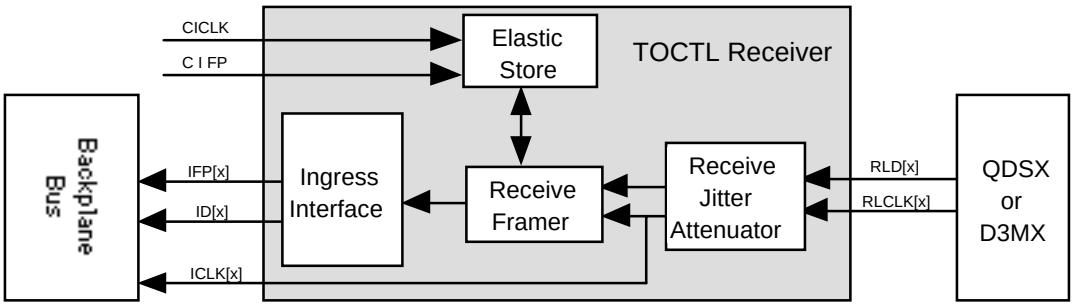

Figure 7: Ingress Clock Slave: ICLK Reference mode.

In the *Clock Slave: ICLK Reference* mode, the elastic store is enabled to permit CICLK to specify the ingress-side timing. The ingress data on ID[x] is bit aligned to the 1.544 MHz *common ingress clock* (CICLK) and is frame aligned to the *common ingress frame pulse* (CIFP). CICLK is either a 1.544 MHz clock or a 2.048 MHz clock with optional gapping for adaptation to non-uniform backplane data streams. ICLK[x] is either a 1.544 MHz jitter attenuated version of RLCLK[x] or an 8 kHz version of RLCLK[x] (by dividing RLCLK[x] by 193). IFP[x] indicates either the frame or superframe alignment on ID[x].

4) Clock Slave: External Signaling.

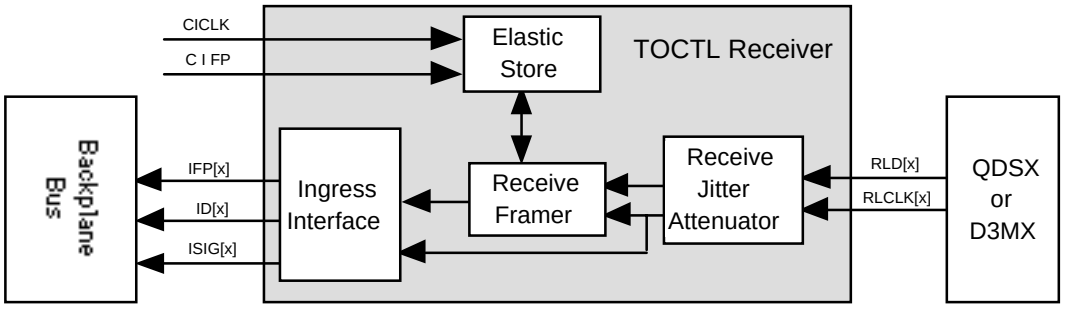

Figure 8: Ingress Clock Slave: External Signaling Mode.

In the *Clock Slave: External Signaling* mode, the elastic store is enabled to permit the use of a common ingress clock for all eight framers. The ingress data on ID[x] and signaling ISIG[x] are bit aligned to the 1.544 MHz common ingress clock (CICLK) and are frame aligned to the *common ingress frame pulse* (CIFP). CICLK is either a 1.544 MHz clock or a 2.048 MHz clock with optional gapping for adaptation to non-uniform backplane data streams. ISIG[x] contains the robbed-bit signaling state (ABCD or ABAB) in the lower four bits of each channel.

Note that the ICLK[x] pins used in *Clock Slave: ICLK Reference* mode are the same pins used for ISIG[x].

Egress Interface

The TOCTL's egress interface allows data to be inserted into the transmit line using one of four possible modes:

- Clock Master: Full DS1
- Clock Master: NxDS0
- Clock Slave: EFP Enabled
- Clock Slave: External Signaling

1) Clock Master: Full DS1

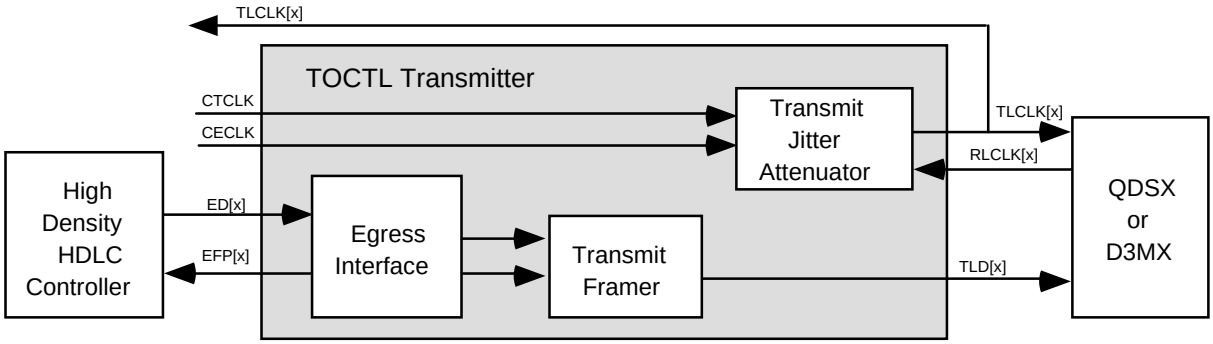

Figure 9: Egress Clock Master: Full DS0 Mode.

In the *Clock Master: Full DS1* mode, the *transmit clock output* (TLCLK[x]) "pulls" data from an upstream data source. The frame alignment is indicated to the upstream data source using the *egress frame pulse* EFP[x] signal. TLCLK[x] may be generated by the PLL in the Transmit Jitter Attenuator, referenced to either *common egress clock* (CECLK), *common transmit clock* (CTCLK), or *receive line clock* (RLCLK[x]). TLCLK[x] may also be derived directly from CTCLK or the 37.056 MHz *crystal clock input* (XCLK).

2) Clock Master: NxDS0.

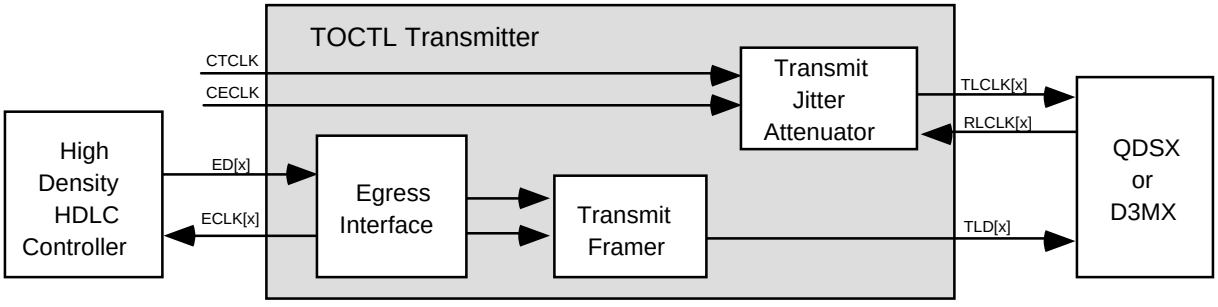

Figure 10: Egress Clock Master: NxDS0 Mode.

The *Clock Master: NxDS0* mode is identical to the *Clock Master: Full DS1* mode except that the frame alignment is not indicated to the upstream device. Instead, *egress clock* (ECLK[x]) is gapped on a per-DS0 basis so that a subset of the 24 channels in the T1 frame is inserted on ED[x]. The framing bit position is always gapped, so the number of ECLK[x] pulses is controllable from 0 to 192 pulses per frame on a per-DS0 basis. The parity functions are not available in the NxDS0 mode.

3) Clock Slave: EFP Enabled.

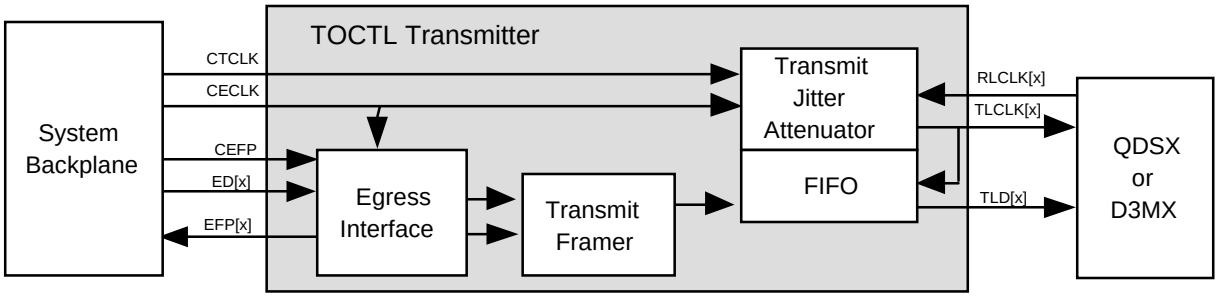

Figure 11: Egress Clock Slave: EFP Enabled Mode

In the *Clock Slave: EFP Enabled* mode, the egress interface is timed by the *common egress clock* (CECLK). CECLK is either a 1.544 MHz or a 2.048 MHz clock with optional gapping for adaptation from non-uniform system clocks. The transmitter is either frame-aligned or superframe-aligned to the *common egress frame pulse* (CEFP). EFP[x] is configurable to indicate the frame alignment or the superframe alignment of ED[x].

4) Clock Slave: External Signaling.

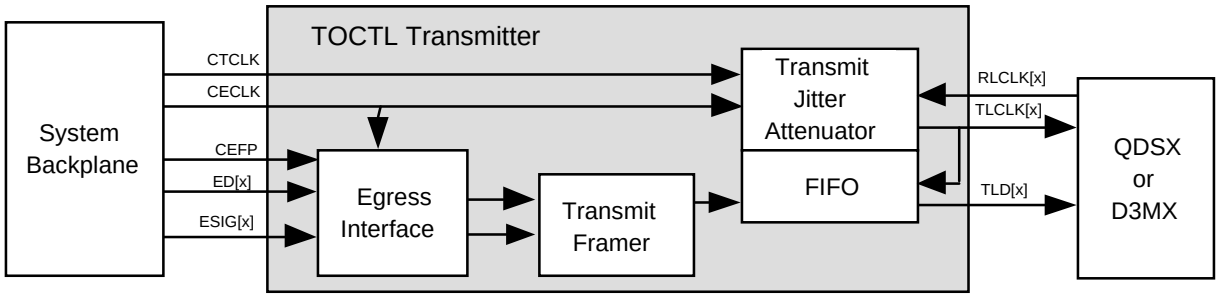

Figure 12: Egress Clock Slave: External Signaling Mode.

In the *Clock Slave: External Signaling* mode, the egress interface is timed by the common egress clock (CECLK). CECLK is either a 1.544 MHz or a 2.048 MHz clock with optional gapping for adaptation from non-uniform system clocks. The transmitter is either frame-aligned or superframe-aligned to the *common egress frame pulse* (CEFP). The *egress signaling* (ESIG[x]) pin allows the robbed-bit signaling data to be inserted into *transmit line data* (TLD[x]).

Performance Monitoring

The TOCTL accumulates the following error and event counters. The counters are sized such that they must be polled once per second to avoid overflow.

Counter	Description
Bit Error Event	A 12 bit counter to accumulate CRC-6 errors in ESF format or framing bit errors in SF format.
Framing Bit Error	A 9 bit counter for framing bit errors.
Out Of Frame Event	A 5 bit counter for OOF events.
Change of Frame Alignment	A 3 bit counter for Change of Frame Alignment events.

ESF Subchannel Processing

The extended superframe (ESF) format is composed of a sequence of 24 frames of 193 bits. The 8 Kbit/s overhead bits are allocated as follows:

- A 2 Kbit/s framing subchannel, this is used by the termination equipment to establish synchronization and to extract other channel information.
- A 2 Kbit/s cyclic redundancy check (CRC) is provided to monitor transmission quality of the DS1 facility. The CRC-6 is generated from the bits of the preceding frame.
- A 4 Kbit/s facility data link (FDL) (also called embedded operations channel) used for maintenance information and supervisory control.

Use of the FDL for carrying performance information and control signals across the network interface is specified in ANSI T1.403. Two signal formats can be used on the FDL:

1) Bit-oriented signals of repeated bit patterns which carry priority messages and command and response messages.
2) Message-oriented signals using a LAPD protocol which carry performance monitoring information.

Bit oriented codes are received on the FDL channel as a 16 bit sequence consisting of 8 ones, a zero, 6 code bits and a trailing zero (111111110xxxxx0). The codeword must be repeated at least 10 times. The TOCTL is able to detect and transmit 63 of the possible 64 bit oriented codes in the FDL channel as defined in ANSI T1.403 and in TR-TSY-000194. The 64th code (111111) is similar to the LAPD flag sequence used in the message-oriented signals and is not a valid bit-oriented codeword.

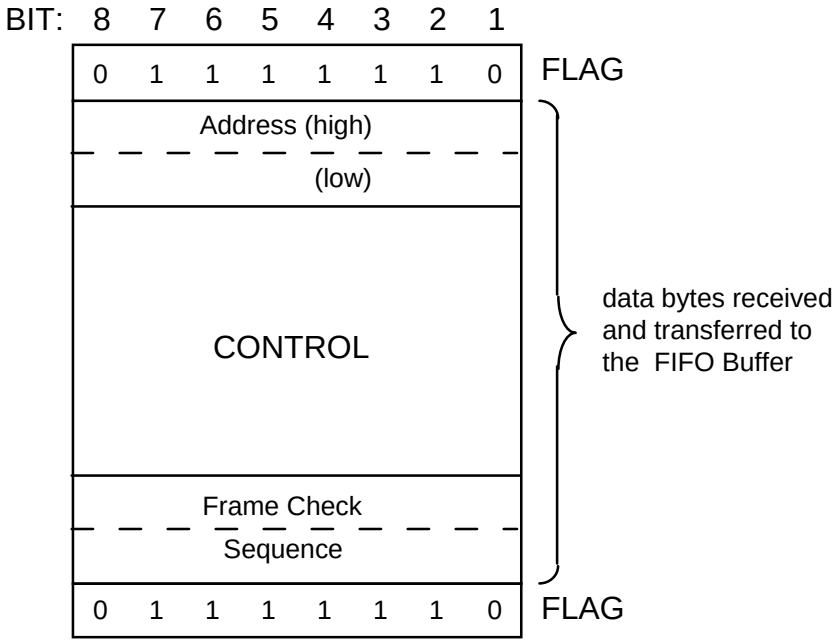

Figure 13: Message-Oriented Frame Structure.

Message-oriented performance reports conform to Q.921 protocol as shown in Figure 13. The TOCTL is able to receive and transmit message-oriented data carried in FDL. In the transmit direction, the message report to be transmitted is written into the *Transmit Data* register by a microprocessor. The TOCTL transmits the message, performs zero-bit stuffing and generates the CRC-CCITT *frame check sequence* (FCS). Zero stuffing by the transmitter prevents the occurrence of the flag pattern (01111110) in the bits between the opening and closing flags of a frame. This is accomplished by inserting a zero after any sequence of five consecutive ones.

In the receive direction, the TOCTL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data and validates the FCS. Received message is placed into a 128 byte FIFO buffer to be accessed by the microprocessor.

Pattern Generator/Detector (PRBS)

Advanced Internet access products require the ability to support T1 diagnostic testing. In typical T1 framers, this function is implemented using external *pseudo random binary sequence* (PRBS) devices. The TOCTL provides a 32-bit fully programmable PRBS generator and detector for each T1 framer. The PRBS function enables the Internet service provider to conduct line testing and verification during service installation and enables ongoing line quality monitoring. It also permits the generation and detection of fractional T1 loopback codes.

To test the reliability of a digital communication link, a specific test pattern is generated at the source, carried through the network, and compared at the destination. The *bit error ratio* (BER) can be measured at the destination by comparing the received data with the expected test patterns.

In TOCTL, each one of the eight framers has a built in *pattern generator/detector* (PRGD) block. The PRGD block is capable of generating and detecting pseudo-random and repetitive patterns including those defined in

ITU-T O.151. At the source, one or more DS0 channels in a T1 link can be configured to carry the test patterns. If multiple DS0s are selected, as in the case of a fractional T1 or a full T1, they are collectively treated as a single data stream and BER testing is conducted on the aggregate DS0s. If a subset of the T1 link is selected for error monitoring, the remaining DS0 can continue to carry data. Therefore, it is not necessary to take down the entire T1 link in order to perform BER testing.

PRGD can be used to test the integrity of the system backplane. To accomplish this, the received data is substituted with test patterns generated by the PRGD block. The data is looped from the *ingress data* (ID[x]) pin through the system backplane to the *egress data* (ED[x]) pin where the received data can be compared by the PRGD block against expected test patterns.

Microprocessor Interface

The TOCTL provides a parallel microprocessor interface for controlling the operation of the TOCTL device.

JTAG

The TOCTL supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1. The boundary scan register allows testing of board inter-connectivity by making all inputs visible and all outputs controllable via the standard 5-pin JTAG port.

A COMPARISON OF TQUAD AND TOCTL

This is a high-level comparison between PM4388 TOCTL and PM4344 TQUAD.

TOCTL Functions Not Available in TQUAD

This section outlines the new features added to TOCTL that are not available on the TQUAD. Specifically, the TOCTL includes the following new functions not available in TQUAD:

- 8 channel device instead of 4 (in the same 128 PQFP package).
- Improved HDLC handling with 128 byte FIFO to lower microprocessor overhead.
- Programmable PRBS generator/detector at DS0 or DS1 rates.
- Low power 3.3V device with 5V tolerant inputs.
- JTAG boundary scan testing.
- Per-DS0 loopbacks to allow for circuit testing.
- Maskable interrupt generated on the detection of signaling change of state.
- Jitter attenuation in both receive and transmit directions.
- DS1 idle code inband detection and automatic Yellow alarm generation.

TQUAD Functions Not Available in TOCTL

This section lists the features that are supported in the TQUAD but not in the TOCTL. Specifically, the TOCTL does not support the following features found in TQUAD:

- No dual rail NRZ data, clock recovery, B8ZS/AMI line decoding nor BPV/pulse density violation detection. These functions are supported by PMC's PM4314 QDSX. Dual rail I/Os are not required where T1 interfaces to a M13 multiplexer/demultiplexer.
- No ANSI 12.5% pulse density enforcement over 192 bit window.
- No T1DM or SLC®96 framing modes.
- No DMA servicing of HDLC data.
- No multiplexed backplane data stream mode.
- No 12.352 MHz crystal option for the *crystal clock input* (XCLK). Only 37.056 MHz is supported.
- No hardware access to the robbed-bit signaling unless the receive streams are referenced to a common ingress clock AND the transmit streams are referenced to a common egress clock. Robbed-bit signals are always accessible via software access from an external microprocessor.

CONTACTING PMC-SIERRA

The PM4388 TOCTL package includes a data book, application notes, and a short form data sheet. Please contact PMC-Sierra for additional information:

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GLOSSARY

AIS	Alarm Indication Signal. This is a signal consisting of unframed all-ones serial digital data. It is transmitted when there is no good data to transmit (due to an upstream failure), and is useful for maintaining a timing reference to downstream equipment. This signal can be detected and transmitted by the TQUAD.
AMI	Alternate Mark Inversion. This is a ternary coding scheme for electrical transmission of digital data. Each binary one that is transmitted is represented by a RZ pulse which is of opposite polarity of the preceding pulse. Each binary zero that is transmitted is represented by a space (no pulse).
ANSI	American National Standards Institute. This is a non-profit, non-government federation of standards-making and standards-using organizations. It publishes standards, but does not develop them. Compliance with an American National Standard is voluntary and does not preclude anyone from manufacturing, marketing, purchasing, or using products, processes, or procedures not conforming to the standards.
B8ZS	Block Eight Zeros Substitution. This refers to a zeros suppression scheme which replaces eight consecutive zeros with a decodeable sequence of LCVs. Zero suppression is important to ensure proper operation of clock recovery circuits
BERT	Bit Error Rate Tester. A device for testing the reliability of a digital datacommunications link. The BERT generates specific data patterns that are routed through a communications device for comparison at the receiving end. The errors are counted by the BERT.
CRC	Cyclic Redundancy Check. This is a scheme for error monitoring by making a Boolean cyclic polynomial calculation over a digital data payload. The transmitter transmits the results of this calculation, and the receiver compares this to it's own calculation. If there is a difference, it is assumed that one or more bits have been corrupted during transmission of the digital payload. Of the standardized DS1 formats, only ESF uses a CRC.
DS1	Digital Signal, Level 1. This term refers to a standardized (ANSI T1.107) format for transmitting serial digital data at 1544 kbit/s.
ELST	Elastic Store. This is PMC-Sierra's mnemonic for the functional block within the TOCTL which provides the elastic store function. The ELST is used for adapting the received data to the system backplane rate. Since these signals are not necessarily synchronized, they may slip with respect to each other. The function of the ELST is to control the slips such that they occur on the frame boundaries indicated on the backplane. For example, if the received data is faster than the system backplane then the ELST will drop full frames of data while maintaining the timeslot alignment on the backplane.
ESF	Extended Superframe Format. This is a standardized (ANSI T1.107) DS1 format. It makes use of the DS1 F-Bits to provide a 24-frame signaling multiframe, CRC error checking, and an out-of band maintenance channel.
F-Bit	Framing Bit. This term denotes the first bit of each DS1 frame which is used for carrying the framing overhead information. The specific use of this bit depends on the DS1 framing format.

FEAC	Far-End Alarm and Control. This term is applied to channels in a transmitted data stream which are reserved for carrying alarm and control information to and from the far-end equipment.
FIFO	First-In First-Out buffer. This term refers to a digital buffer which outputs data in the same order as it was input.
ISDN	Integrated Services Digital Network. This is a world-wide public telecommunications network that is implemented as a set of digital switches and paths supporting a broad range of services.
ITU-T	International Telecommunication Union - Telephony. This is a committee within a United Nations treaty organization. The charter is "to study and issue recommendations on technical, operating, and tariff questions relating to telegraphy and telephony." Its primary objective is end-to-end compatibility of international telecommunications connections.
LCV	Line Code Violation. This term denotes a received bipolar pulse which violates the AMI or B8ZS ternary coding scheme. LCV events are detected and accumulated by the TQUAD.
LOS	Loss-of-Signal. This term refers to the state a clock recovery unit is in when there is no input signal. Since DS1 requires either a minimum pulse density or the use of a zero code suppression scheme (such as B8ZS), the TQUAD monitors for LOS by monitoring the number of consecutive spaces (zeros) received.
NRZ	Non-Return-to-Zero. This refers to the common electrical coding scheme for serial digital data. Logical ones are represented as a pulse which is high for the full bit period. Logical zeros are represented as no pulse for the full bit period. This scheme is useful for serial digital data which has an associated clock signal.
OOF	Out-Of-Frame alignment. This is the state a DS1 framer is in if it cannot find the frame alignment pattern within the received serial 1544 kbit/s data.
PCM	Pulse-Coded Modulation. Digital serial data representing analog signals on telephone subscriber loops.
PLL	Phase-Locked Loop. The generic term for a feed-back system which generates a clock with a fixed (locked) phase/frequency relationship to some reference clock.
RZ	Return-to-Zero. This refers to an electrical coding scheme for serial digital data. Logical ones are represented as a pulse which is high for half the bit period then returns to low (zero) for the remainder of the bit period. Logical zeros are represented as no pulse. This scheme is useful for serial digital data from which a clock must be recovered.
SF	Superframe Format. This is a standardized (ANSI T1.107) DS1 format. It makes use of the DS1 F-Bit to maintain a 12-frame signaling multiframe.
SLC®96	Subscriber Loop Carrier 96. This is a standardized (Bellcore TR-TSY-000008) DS1 format. It is similar to SF, but makes use of the F-Bits such that it also carries a datalink. This datalink is used for concentrating up to four DS1 streams for an aggregate of 96 (4 x 24) 64kbps channels.
T1	Transmission format level 1. This term is used loosely to describe systems carrying DS1-formatted signals electrically over cable.

T1DM	T1 Data Multiplexer. This is a standardized (Bellcore TA-TSY-000278) DS1 format. It uses Timeslot 24 of the DS1 frame to pass additional framing information as well as a datalink.

NOTES:

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