PM6344

EQUAD

EQUAD with QDSX Reference Design

Issue 1: September, 1996

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OVERVIEW

This document describes an implementation of a design based on both PMC-Sierra's PM6344 EQUAD and PM4314 QDSX devices. The EQUAD with QDSX Reference Design embodies PMC-Sierra's guidelines and suggestions for designing a four port E1 interface card.

In addition to the PM6344 EQUAD and PM4314 QDSX devices, the EQUAD with QDSX Reference Design incorporates an on-board microcontroller (Microchip PIC16C74) for providing the local maintenance functions.

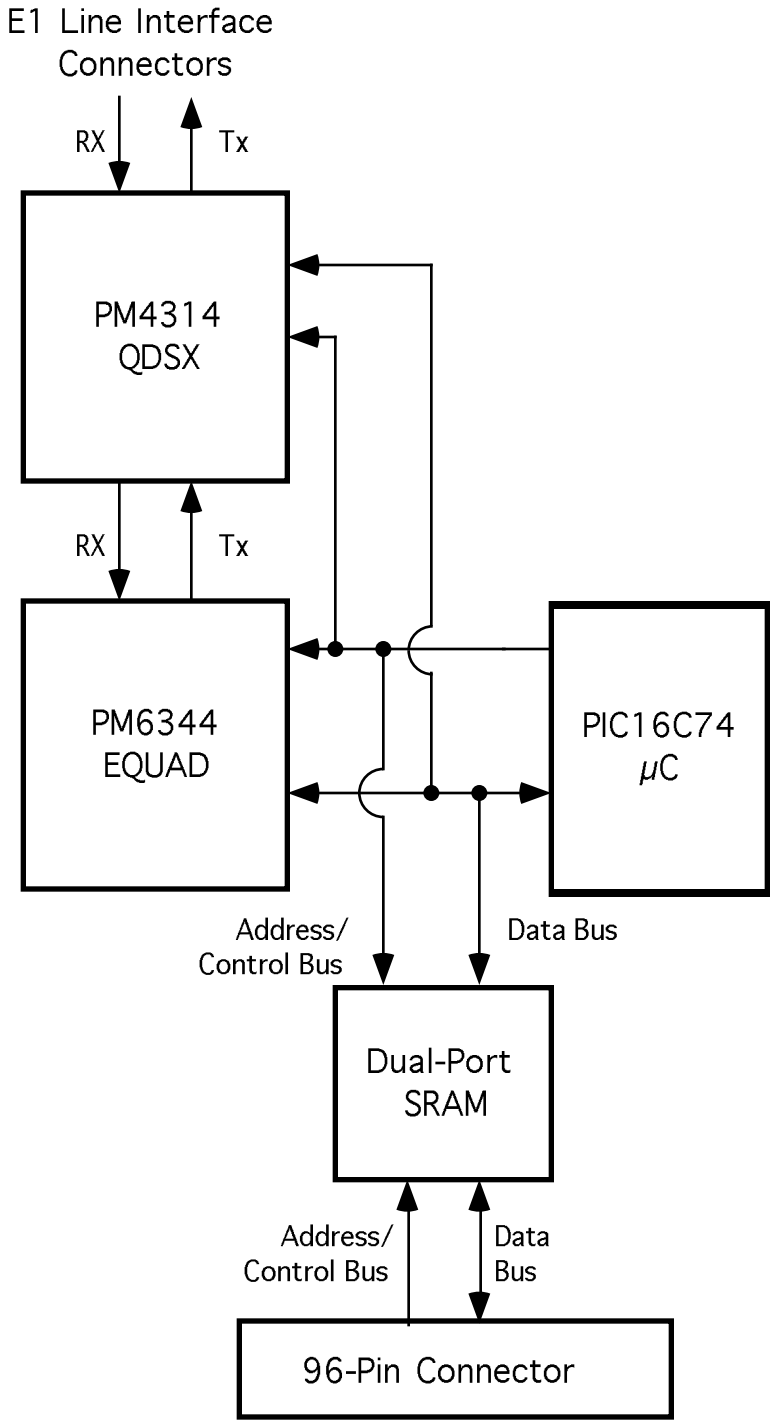
The EQUAD with QDSX Reference Design communicates with the host system using a 96-pin connector. The pin-out of this connector is compatible for connection with the PMC-Sierra's PM1501 Evaluation Motherboard, but is intended to be a generic 8-bit microprocessor interface to a multiplexed bus.

The host does not have a direct connection to the microprocessor port of the EQUAD or QDSX. Rather, a dual-port RAM, shared by the host and the local PIC16C74, is used to pass control and status information about the EQUAD and QDSX to and from the host — the actual register accesses to the EQUAD and QDSX are performed by the PIC16C74. The host system and PIC16C74 also communicate through the "mailbox" communication channels in the dual-port RAM.

The advantage to this architecture is that the host system is not burdened by the low-level monitoring and control functions related to the physical layer.

FUNCTIONAL DESCRIPTION

Block Diagram



PM6344 EQUAD

The PM6344 Quadruple E1 Framer (EQUAD) is a feature-rich device suitable for use in many E1 systems with a minimum of external circuitry. Each of the framers and transmitters is independently software configurable, allowing feature selection without changes to external wiring.

On the receive side, the EQUAD recovers clock and data and can be configured to frame to a basic G.704 2048 kbit/s signal or also frame to the signaling multiframe alignment signal and the CRC multiframe alignment signal.

The EQUAD also supports detection of various alarm conditions such as loss of signal, loss of frame, loss of signaling multiframe, loss of CRC multiframe, and reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and timeslot 16 alarm indication signal. The EQUAD detects and indicates the presence of remote alarm and AIS patterns and also integrates red and AIS alarms as per industry specifications.

Performance monitoring with accumulation of CRC-4 errors, far end block errors, framing bit errors, and line code violation is provided. The EQUAD also detects and terminates HDLC messages on a datalink. The datalink may be extracted from timeslot 16 and used for common channel signaling or may be extracted from the national bits.

An elastic store for slip buffering and adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis. Receive side data and signaling trunk conditioning is also provided.

On the transmit side, the EQUAD generates framing for a basic G.704 2048 kbit/s signal, or framing can be optionally disabled. The signaling multiframe alignment structure may be optionally inserted and the CRC multiframe structure may be optionally inserted.

Channel associated signaling insertion, idle code substitution, digital milliwatt tone substitution, and data inversion on a per-timeslot basis is also supported. Transmit side data and signaling trunk conditioning is provided.

HDLC messages on a datalink can be transmitted. The datalink may be inserted into timeslot 16 and used for common channel signaling or may be inserted into the national bits. The EQUAD can generate a low jitter transmit clock and provides a FIFO for transmit jitter attenuation. When not used for jitter attenuation, the full or empty status of this FIFO is made available to facilitate higher order multiplexing applications by controlling bit-stuffing logic.

The EQUAD provides a parallel microprocessor interface for controlling the operation of the EQUAD device. Serial PCM interfaces allow 2.048 Mbit/s backplanes to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic. Optional bit interleaved multiplexing of the individual serial streams supports 16.384 Mbit/s backplanes.

For a complete description of the EQUAD, please refer to PMC-Sierra's EQUAD databook (document number PMC-951013).

PM4314 QDSX

The PM4314 QDSX Quad T1/E1 Line Interface Device is a monolithic integrated circuit that supports DSX-1 and CEPT E1 compatible transmit and receive interfaces for four 1.544 Mbit/s or 2.048 Mbit/s data streams.

In the receive direction, clock and data are recovered from the received signal using a digital phase-locked loop that provides excellent high frequency jitter accommodation. The recovered data is decoded using B8ZS, HDB3, or AMI line code rules. Loss of signal and line code violations are detected. Line code violations are accumulated in internal counters.

In the transmit direction, each quadrant of the QDSX can transmit either a DSX-1/E1 stream encoded using B8ZS, HDB3, or AMI line code rules. The digital data is converted to high drive, dual rail RZ pulses that drive the DSX-1/E1 interface through a coupling transformer. The shape of the pulses is programmable to ensure that the DSX-1/E1 pulse template is met after the signal is passed through different cable lengths or types. Driver performance monitoring is provided and can generate interrupts upon driver failure.

A jitter attenuation function comprised of a digital phase-locked loop and data FIFO is available for use in either the transmit or receive path of each channel.

Diagnostic loopback is provided and the loopback may be invoked past the analog transmit outputs using the driver performance monitors or invoked prior to the conversion to analog. Line loopback with jitter attenuation is provided and may be enabled for automatic operation based on detected in-band loopback codes.

The QDSX detects framed or unframed in-band loopback code sequences from the received input pulses. Any arbitrary code from three to eight bits in length can be declared to be the activate and deactivate codes by writing to configuration registers. The in-band loopback code detector can optionally be moved to the transmit side where it detects in-band loopback codes in the unipolar input transmit data stream. For framed in-band loopback code sequences, it is expected that the framing bit overwrites the in-band loopback code bit.

The QDSX can insert unframed in-band loopback code sequences (programmable codes from three to eight bits in length) into the transmit or receive path of each channel. The QDSX detects framed or unframed in-band loopback code sequences in either the transmit or receive path of each channel. Two arbitrary codes can be searched for simultaneously, each programmable between three to eight bits in length.

The QDSX can insert an unframed 2^{15}-1 O.151 compatible pseudo-random bit sequence into the transmit or receive path of each channel. The QDSX can detect an unframed 2^{15}-1 O.151 compatible pseudo-random bit sequence in either the transmit or receive path of each channel.

The QDSX operates in conjunction with external line coupling transformers, resistors, and capacitors. An external crystal oscillator may be used for high speed timing generation. The QDSX is configured, controlled, and monitored using registers that are accessed via a generic microprocessor interface.

Internal high speed timing for all quadrants of the QDSX is provided by a common 37.056 MHz (for T1) or 49.152 MHz (for E1) master clock. This master clock rate is required for applications where QDSX provides jitter attenuation.

For a complete description of the QDSX, please refer to PMC-Sierra's QDSX Data Book (document number PMC-950857).

PIC16C74 Microcontroller

The Microchip PIC16C74 is a low-cost, high-performance, CMOS, fully-static EPROM-based 8-bit microcontroller. It employs a Harvard RISC-like architecture with 14-bit instruction words. Its two stage instruction pipeline allows most instructions to be executed in a single cycle. The PIC16C74 has enhanced core features, an eight-level deep stack, and multiple internal and external interrupt sources.

The PIC16C74 has 192 bytes of on-chip RAM and a 4k by 14-bit EPROM for program memory.

It has 33 I/O pins, each of which can source/sink 25mA.

The PIC16C74 also has a number of peripheral features (A/D converters, timer/counters, capture/compare/PWM modules, and two serial ports) which are not used in this reference design.

In the EQUAD with QDSX Reference Design, the PIC16C74 is devoted to the local maintenance functions for the E1 transmission.

Firmware for the PIC16C74 can be developed in Assembly language using Microchip's PC-hosted symbolic assembler, MPASM, available free from Microchip's bulletin board (MCHIPBBS on Compuserve). Also available free from Microchip is a C compiler and a simulator. The PIC16C74 can be programmed on universal programmers from Sprint and Data I/O. Additionally, Microchip sells programmers for this device.

Dual-Port RAM

This a high-speed 2K by 8-bit dual-port static RAM with internal interrupt logic for inter-processor communications. Many manufacturers (such as Integrated Device Technology, and Cypress Semiconductors) produce pin-compatible versions of this device.

The dual-port RAM has two independent ports with separate control, address and data pins that permit independent, asynchronous access for both reads and writes to any location in memory.

Depending on the functionality required, a memory map would be defined to pass status and control information between the host and the local PIC16C74.

IMPLEMENTATION DESCRIPTION

The schematic diagram of the EQUAD with QDSX Reference Design is contained in Appendix C. This section explains that schematic diagram.

The EQUAD with QDSX Reference Design schematic shows six main functional blocks: address decode/demultiplex logic, a PIC16C74 micro controller, dual-port RAM, a PM6344 EQUAD, a PM4314 QDSX, and line interface circuitry. Additionally, the schematic contains connectors, timing sources and miscellaneous "glue" circuitry. Each functional block is described below.

Address Decode/Demultiplex Logic

The DECODE_LOGIC functional block provides the chip select decoding of the address on the microprocessor bus. Additionally, this block de-multiplexes the AD[7:0] address/data lines from the 96-pin connector interface. The DECODE_LOGIC functional block buffers the remaining signals, and pulls up any that are tristatable.

The chip selects control access to the dual-port RAM. The outputs of the DECODE_LOGIC functional block go to the Left Port of the dual-port RAM.

The host cannot directly address the EQUAD or QDSX. Rather, the dual-port RAM mailbox register must be used to pass a command to the PIC16C74 to initiate a register access.

PIC16C74 Microcontroller

This subsection explains the connections and considerations concerning use of the PIC16C74 to provide the local maintenance functions on the EQUAD with QDSX Reference Design.

Interrupt Handling

The only efficient way of processing events that may have a low frequency of occurrence is to use interrupt-driven routines (instead of polling). The events (alarm conditions, timers, datalink servicing, and dual-port mailbox events) on the EQUAD, QDSX and the dual-port RAM will, on average, be low frequency.

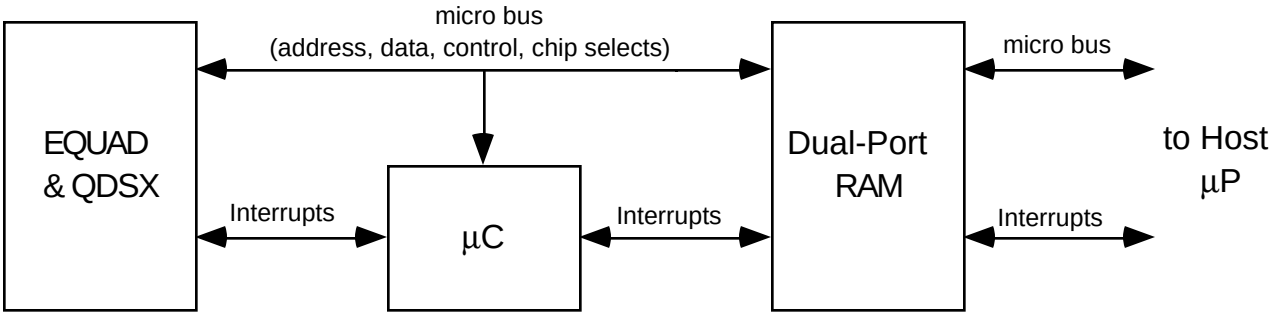
When the PIC16C74 detects an interrupt indication on its external interrupt input pins, it has to determine the source of the interrupt — first by polling its internal interrupt source register to determine if it was the EQUAD, QDSX or the dual-port RAM that interrupted. If it was the EQUAD or QDSX, then the appropriate device's registers need to be polled to determine what event caused the interrupt.

Once the PIC16C74 has determined the interrupt source, it can jump to a routine specific to that interrupt. Below, brief descriptions are given of service routines for each type of interrupt source.

External Memory Accesses

The PIC16C74 does not have a microprocessor bus suitable to access registers and memory within the EQUAD, QDSX and dual-port RAM. Therefore I/O pins on the PIC16C74 are defined to act as the address bus, data bus, chip selects, RDB, WRB and other signals necessary. Since the PIC16C74 is only accessing two external devices, it generates the chip selects instead of relying on external decode logic. Figure 1 shows a block diagram of the connections.

Figure 1. Block Diagram of PIC16C74 Connections



Subroutines are required to operate dedicated I/O pins as the micro bus during external accesses. Since the interrupt service routines will alternate between accessing the EQUAD, QDSX and the dual-port RAM, it saves instruction cycles to have separate subroutines dedicated to each, where the address would be taken from different pre-defined registers.

Initialization

The EQUAD and QDSX should be initialized to enable the appropriate interrupts, set the framing format, configure the interfaces, set the timing options.

The dual-port RAM should be initialized all necessary memory map status information is updated.

Maintenance Functions

There are a number of standardized maintenance functions. These include Remote Alarm Indication (RAI), Alarm Indication Signal, Loopbacks, and Performance Reports. All of these functions can be handled via interrupts from the EQUAD, as described in the following subsections.

Note: Each quadrant within the EQUAD has independent registers for maintenance functions. Below, where specific registers are referred to, the address is for the first quadrant; the other quadrants would be accessed via their equivalent registers.

REMOTE ALARM INDICATION (RAI)

A E1 RAI should be indicated to the remote E1 equipment in response to a out-of-frame condition, or receipt of an AIS defect. The Remote Alarm Indication consists of forcing Bit 3 of every NFAS frames to a logic 1.

The simplest implementation is to set the REMAIS bit in Register 045H (or equivalent) to logic one when an OOFI interrupt occurs with OOF=1 (in Register 024H and equivalent). The REMAIS bit should be cleared to logic zero when an OOFI interrupt occurs where OOF=0.

ALARM INDICATION SIGNAL (AIS)

The AIS should be sent upon loss of originating signal, or when any action is taken that would cause a service disruption (such as some loopbacks). If AIS transmission is desired, the AIS bit in Register 045H (or equivalent) should be set to logic one by the host (using the mailbox communication channel in the dual-port RAM).

LOOPBACKS

Loopbacks are used by carriers and customers as a maintenance tool to aid problem resolution. The carrier uses loopbacks for trouble isolation, and the customer uses them for CI-to-CI testing.

There are two standardized loopbacks: Line and Payload. Both Line and Payload loopbacks are supported in the EQUAD.

Note that the ETS 300 233 loopback commands are not detected or generated by the EQUAD. Therefore, if this functionality is needed, external circuitry which monitors and controls the Sa6 bit in TS0 in the BRPCM and BTPCM data streams (and using BTFP and BRFPI as multiframe pulsed to determine the sub-multiframe alignment) would be required.

Performance Monitoring

All the standardized performance monitoring parameters are available within registers of the EQUAD and QDSX. Therefore, with a timer interrupt setting the accumulation interval, the PIC16C74 can transfer all the performance monitoring indicators and parameters to known memory locations in the dual-port RAM. The host system could then process these parameters.

Dual-Port Mailboxes

The dual-port RAM contains two mailboxes, one in each direction, for passing data between the two ports. When the micro bus on one port writes a data byte to a specified location, the other port is interrupted. Using these mailboxes, a proprietary messaging scheme can be arranged for diagnostic operations. These interrupts from the dual-port RAM must be processed by the PIC16C74.

For example, a useful feature is to allow the host system to peek and poke registers within the EQUAD and QDSX devices (which is not in directly in the host address space). A simple protocol would be that the host would write a byte to the mailbox indicating that it wishes to perform a Read or Write, as well as putting the address and, if necessary, data within pre-defined locations within the dual-port RAM. Then, when the PIC16C74 services the mailbox interrupt, it would handle the operation, and send a message in the return mailbox indicating that the access has been completed.

Dual-Port RAM

The dual-port RAM is shared by the host system and the local PIC16C74 microcontroller. The PIC16C74 performs all the local maintenance functions (including termination of the facility datalink), while the dual-port RAM is used to pass information to and from the host system. This arrangement greatly reduces the real-time burden on the host system, allowing the host to interact with the EQUAD with QDSX Reference Design at a higher level than direct access to the individual physical layer devices.

The dual-port RAM holds, as a minimum, the following information:

- packets received by the EQUAD over the facility datalink
- packets to be transmitted by the EQUAD over the facility datalink
- status of the EQUAD and QDSX. This includes performance monitoring indications and parameters.

The EQUAD with QDSX Reference Design has been given 2 kbytes of space starting at 4000H.

The two ports on the dual-port RAM are denoted the "Left" and "Right" ports. In this design, the Left Port is connected to the 100-pin connector which carries the host microprocessor bus (which is decoded, de-multiplexed and buffered on the D3MX Module). The Right Port is connected to the PIC16C74's microprocessor bus (shared with the microprocessor port of the EQUAD and QDSX).

The two ports are entirely independent from each other and allow asynchronous Read and Write accesses from either port.

Each port also has an interrupt indication line used for processing a "mailbox" communications channel within the dual-port RAM. Each port has a memory location, which, when it is written to, alerts the other port via the interrupt indication signal. Therefore, a protocol can be used to pass information through these mailboxes. Uses of this communications channels include:

- allowing the host to "peek" and "poke" registers in the EQUAD and QDSX,
- initiating different configuration routines, and
- initiating different diagnostic routines.

EQUAD Functional Block

The EQUAD is a full-featured quadruple E1 framer which provides most standard E1 framing functions and performance monitoring.

The full register set of the EQUAD, including Test Mode registers are accessible to the PIC16C74 block. For a full description of these registers, refer to the EQUAD Data Book.

The backplane signals of the EQUAD are connected to header blocks. In a real application, these signals would be further processed. The header blocks are arranged to allow easy physical (payload) loopbacks on the EQUAD with QDSX Reference Design.

QDSX Functional Block

The QDSX is a full-featured quadruple T1/E1 line interface unit which provides a G.703-compliant interface for 1544 kbit/s and 2048 kbit/s rates.

The full register set of the QDSX, including Test Mode registers are accessible to the PIC16C74 block. For a full description of these registers, refer to the QDSX Data Book.

In this reference design, the QDSX is being used solely to provide a E-1 interface for the four duplex E-1 serial data streams.

Line Interface Circuitry

The line interface circuitry consists of the transformers, connectors and passive networks necessary to interface the QDSX device to cables carrying G.703-compliant 2048 kbit/s signals. This circuitry reflects recommendations in the QDSX data book.

The transformer shown is a new product, the T1008 from Pulse Engineering. Other manufacturers which produce suitable transformers are BH Electronics, Filtran, Midcom, and Schott. The characteristics of the transformer should match those recommended in the QDSX data book.

Timing Distribution

The high-speed timing to both the EQUAD and QDSX devices is sourced from a 49.152 MHz crystal oscillator.

The high-speed timing to the PIC16C74 is sourced from a 20.0 MHz crystal oscillator.

There are also two SMA connectors for providing two signals, BCLK_EXT and BFPI_EXT, to source the backplane timing signals to the EQUAD. The BCLK_EXT clock signal can be 2.048 MHz or 16.384 MHz depending on the backplane format chosen for the EQUAD. The BFPI_EXT frame pulse signal must be a valid frame pulse meeting the timing requirements of the BRFPI, BTFP, MRFP or MTFP (depending on the ones used) inputs of the EQUAD as specified in the EQUAD data book.

In this reference design, the BCLK_EXT and BFPI_EXT signals are shown going through MC100ELT21 PECL-to-TTL converters. This is done to provide an easy interface to frequency synthesizers in PMC-Sierra's in-house laboratories. In customer applications, the BCLK_EXT and BFPI_EXT signal could be sourced directly from a TTL-compatible clock source.

Additionally, there are header blocks available which can be jumpered to provide loop-timing of the backplane to the receive timing.

Header Blocks

To keep this reference design generic, the backplane signals of the EQUAD are not processed but rather brought out to headers for observation and as a point for interconnection. In a customer applications, these signals would be further processed as appropriate (e.g. timeslot interchange, frame relay, ATM, etc.).

The following signals are brought to headers:

- BRPCM[4:1] are the four Backplane Receive PCM serial data streams.
- BRSIG[4:1] are the four Backplane Receive Signaling serial data streams which indicate the extracted robbed-bit signaling information of each PCM timeslot on BRPCM.
- RFP[4:1] are the four Receive Frame Pulse Outputs which indicate the frame alignment found within the associated receive serial stream.
- BFPI_EXT is an external frame pulse for controlling the frame alignment of the EQUAD's synchronous backplane, provided via an SMA connector. BFPI_EXT is common to all of the quadrants within the EQUAD due to its connection to the BRFPI input.
- RCLKO[4:1] are the four Receive Clock Outputs. If an Elastic Store (ELST) within the EQUAD is bypassed, then the associated BRPCM and BRSIG signals are timed to this clock.
- BTCLK[4:1] are the four Backplane Transmit Clock inputs.

- BCLK_EXT is an external clock for controlling the timing of the EQUAD's synchronous backplane, provided via an SMA connector. BCLK_EXT is common to the receive backplane of all the quadrants within the EQUAD due to its connection to the BRCLK input.

For more detailed information on the use of these signals, refer to the EQUAD data book.

The headers are physically arranged to facilitate physical loopbacks. Each backplane receive PCM stream can be looped back by physically connecting the BRPCM[n] and BRSIG[n] signals to BTPCM[n] and BRSIG[n] respectively. Additionally, either the RCLKO[n] or the BRCLK_EXT signal should be connected to BTCLK[n] (depending whether the ELST is bypassed or not).

96-Pin Connector

The 96-pin connector interface carries all the signals required to connect the EQUAD with QDSX Reference Design to a host 8-bit multiplexed microprocessor bus.

The connector is a 96-pin female connector, with the pin defined as described in the table below (only 64 of the pins are used). This connector was chosen because it is compatible with the PMC-Sierra PM1501 Evaluation Motherboard (described in PMC-910501).

Signals are provided for a Motorola-type multiplexed microprocessor bus (including interrupts, and a hardware RESET signal). Additionally, power and ground are provided through this connector. TTL signal levels are assumed on this interface.

In the following table the signal type is one of: I (input), O (output), I/O (bi-directional), N/C (no-connect), PWR (power), or GND (ground). The direction of the signal is with reference to this design.

Signal Name	Type	Pin	Function
ALE	I	C1	Address latch enable. When high, identifies that address is valid on AD[7:0]. This signal is used for de-multiplexing the microprocessor bus.
E	I	C2	External data access indication. Active high.
RWB	I	C3	Active low write enable, active high read enable
RSTB	I	C4	Active low hardware RESET. This is connected to all devices providing a hardware RESET pin. After a hardware RESET, the D3MX Module should be re-initialized unless operating in stand-alone mode (no microprocessor).
A[15]	I	C5	Address bus bit 15
A[14]	I	C6	Address bus bit 14
A[13]	I	C7	Address bus bit 13
A[12]	I	C8	Address bus bit 12
A[11]	I	C9	Address bus bit 11
A[10]	I	C10	Address bus bit 10
A[9]	I	C11	Address bus bit 9
A[8]	I	C12	Address bus bit 8
AD[7]	I/O	C13	Multiplexed address/data bus bit 7
AD[6]	I/O	C14	Multiplexed address/data bus bit 6
AD[5]	I/O	C15	Multiplexed address/data bus bit 5
AD[4]	I/O	C16	Multiplexed address/data bus bit 4
AD[3]	I/O	C17	Multiplexed address/data bus bit 3
AD[2]	I/O	C18	Multiplexed address/data bus bit 2
AD[1]	I/O	C19	Multiplexed address/data bus bit 1
AD[0]	I/O	C20	Multiplexed address/data bus bit 0
PA3	I	C21	68HC11 Processor Port A bit 3
PA4	I	C22	68HC11 Processor Port A bit 4
PA5	I	C23	68HC11 Processor Port A bit 5
PA6	I	C24	68HC11 Processor Port A bit 6

PD2	O	C25	Master In Slave Out (MISO) of 68HC11 Port D bit 2 acting as SPI. Pulled up on motherboard.
PD3	I	C26	Master Out Slave In (MOSI) of 68HC11 Port D bit 3 acting as SPI. Pulled up on motherboard.
PD4	I	C27	Serial Clock (SCK) of 68HC11 Port D bit 4 acting as SPI. Pulled up on motherboard.
PD5	I	C28	Slave Select (SS) of 68HC11 Port D bit 5 acting as SPI active low. Pulled up on motherboard.
IRQB	O	C29	Maskable 68HC11 interrupt. Pulled up on motherboard.
BRB (XIRQB)	O	C30	Non Maskable 68HC11 interrupt. Pulled up on motherboard.
DISB	O	C31	EVMB memory disable. Pulling this signal low will disable MPU access to the EVMB's on-board RAM and EPROM. Pulled up on motherboard.
SP	I	C32	Spare
GND	GND	A1-A28	Ground
+5V	PWR	A29-A32	+5 Volts

APPENDIX A: DESIGN CONSIDERATIONS

Power Supply Voltage Transients

High currents drawn during IC switching causes power supply voltage transients due to the inductance of the power lines. The magnitude of the noise voltage can be reduced by minimizing the inductance of the power lines and by decreasing the magnitude of the transient currents. The power line inductance can be minimized by using a power plane. The transient currents on the power rails can be minimized by supplying the power from a local source such as a de-coupling capacitor near the circuit drawing the current.

The de-coupling capacitance and the inductance of the connection between the capacitor and the power pin determine the noise voltage at the power pin. The effectiveness of the de-coupling capacitor depends on the frequencies of the transients. Large "bulk" de-coupling capacitors are used to supply the low-frequency current variations and the small "noise-bypassing" capacitors are used to supply the high-frequency transient current that is required when the circuit is switching.

Ground Noise

Return currents and power supply transients during high current consumption produce most of the ground noise. Since ground noise cannot be controlled by de-coupling capacitors, the only way to minimizing the effect of ground noise is to minimize ground impedance. The best way to minimize ground impedance is to use a ground plane. It is not advisable to use ferrite beads in the ground path as this will inhibit the return currents from leaving and raise the ground noise level.

Noise-Bypassing at Power Pins

The EQUAD can generate a lot of simultaneous switching noise, especially if the line rate clocks are synchronous. It is important to provide a noise-bypassing capacitor at every power pin so that the switching currents can be supplied locally, thereby reducing the noise introduced into the power plane.

Values of Noise-Bypassing Capacitors

A rule of thumb is that the "bulk" noise-bypassing capacitor (placed where the power enters the circuit board) should have 10 times the value of all the noise-bypassing capacitors combined. Capacitors with low internal inductance should be used such as a tantalum electrolytic. Stay away from aluminum electrolytic as their inductances are an order of magnitude larger than tantalum capacitors.

The noise-bypassing capacitors (placed near the power pins) must be able to supply all the switching current. The minimum capacitance can be calculated by:

$$C = \frac{\Delta i \times \Delta t}{\Delta v}$$

The transient voltage drop ΔV in the supply voltage is caused by the transient current Δi occurring over time Δt across capacitance C. This equation shows that the voltage drop will be minimized as the capacitance is increased. However, using capacitors that are too large should be avoided due to their resonance characteristics.

Since all capacitors have some stray inductance in series with the capacitance, there will be a self-resonance at a certain frequency given by the equation:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Note that the larger the capacitance (for the same inductance) the lower the resonant frequency. If the capacitor is too large, the self-resonance will be too low to be an effective bypass but if the capacitor is not large enough, there will be insufficient current to supply the transient current during switching. The smallest value capacitor to satisfy the above equations should be used. It is rarely necessary that a capacitor larger than 0.01 µF be used.

Placement of Noise-Bypassing Capacitors

The de-coupling capacitor should be placed as close to the IC power pin as possible to reduce the wiring inductance. There are five sources of inductance: the parasitic inductance of the capacitor, the inductance of the wiring between the capacitor and the IC power pin, the power pin lead inductance inside the IC, the ground pin lead inductance inside the IC, and the ground inductance between the IC pin and ground. The capacitor inductance is negligible if the correct capacitor is used. There is no control over the lead frame inductance. To keep the inductance low, both the power lead and the ground lead should be keep as short as possible (less than 1.5 inches). The inductance for a trace is given by:

$$L = 0.005 \log^{-1}\left(2\pi\frac{h}{w}\right) \ \mu\text{H/inch}$$

where **h** is the height between the power or ground lead and the ground plane and **w** is the width of the power or ground lead. Note that doubling the width of the trace or reducing **h** will only decrease **L** approximately by 20%, but decreasing the length by 50% will decrease the inductance by 50%. A typical PCB trace has about 15nH of inductance per inch.

Ferrite Beads

Ferrite beads are mainly used on power rails to pass DC current but to attenuate the higher frequency noise that is riding on the DC rail. The impedance of ferrite beads increases with frequency; at DC the ferrite bead is like a short but at higher frequency the impedance of a ferrite bead can increase to over 100 ohms (depending on the bead and frequency). Ferrite beads attenuate high frequency noise from the power supply from getting into a circuit, but they also stop high frequency switching currents required by digital ICs. It is important, therefore, to use proper noise bypass capacitors when using ferrite beads to provide a local source of switching current.

Ferrite beads should be avoided on CMOS I/O power pins as the high current switching of the CMOS circuits causes a $\Delta \mathbf{I}/\Delta \mathbf{t}$ noise to be introduced into the power rail. This noise is induced because the ferrite beads "starve" the digital circuitry, causing the voltage to fluctuate locally. Ferrite beads should also be avoided on the ground bus as this inhibits the return currents.

Unused CMOS Inputs

"Floating" CMOS inputs (those that are left unconnected) may switch unpredictably, causing unwanted noise and power consumption. Therefore, all unused inputs should be connected to their inactive state: to ground or to the power rail (Vcc). Unused bi-directionals should be "pulled" through a series resistor (4.7k or greater) to avoid short-circuits occurring if the bi-directionals are erroneously configured as outputs.

APPENDIX B: MATERIAL LIST

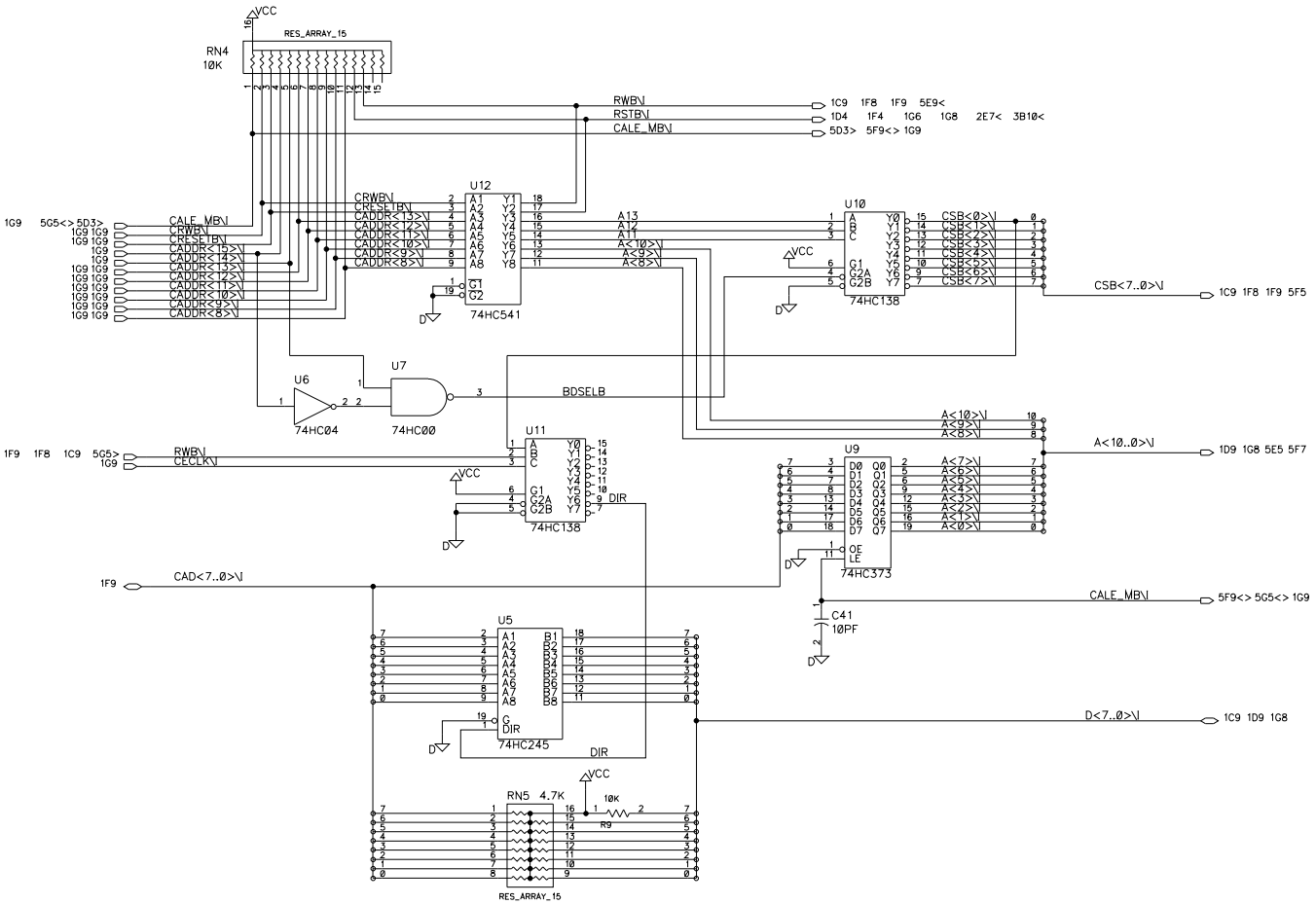
NO.	Part Name - Value	Jedec Type	Ref Des	Qty
1	74XXX00_SOIC-HCMOS	SOIC14	U7	1
2	74XXX04_SOIC-HCMOS	SOIC14	U6	1
3	74XXX138_SOIC-HCMOS	SOIC16	U10,U11	2
4	74XXX245_SOIC-HCMOS	SOIC20W	U5	1
5	74XXX373_SOIC-HCMOS	SOIC20W	U9	1
6	74XXX541_SOIC-HCMOS	SOIC20W	U12	1
7	BANTAM-BASE	BANTAM	J91-J98	8
8	CAP-.68UF,METAL POLY	CAP200	C37-C40	4
9	CAP-0.001UF	SMDCAP805	C6,C7,C9, C11-C13,C15, C17,C18,C21, C22,C25,C26, C30,C82	15
10	CAP-100000PF	SMDCAP1206	C1-C5,C8,C10, C14,C16,C19, C20,C23,C24, C27,C31, C45-C48, C74-C81,C84,C85	29
11	CAP-10000PF	SMDCAP805	C28,C33-C36, C58-C73	21
12	CAP-1000PF,NPO_805	SMDCAP805	C42-C44,C83	4
13	CAP-10PF,NPO_805	SMDCAP805	C41	1
14	CAP-47000PF	SMDCAP1206	C53-C56	4
15	CAPACITOR POL-0.47UF,25V, TANT A	SMDTANCAP_A	C49-C52	4
16	CAPACITOR POL-100UF, 16V,ELECTRO	CAP320	C32	1
17	CAPACITOR POL-10UF, 16V,TANT TEH	SMDTANCAP_C	C29,C57	2
18	CY7C136_-BASE	PLCC52	U3	1
19	DIN96_MALE-BASE	AMP_650473-5	P1	1
20	EQUAD-BASE	PQFP128	U8	1
21	HEADER8-BASE	SIP8	J2-J6,J9	6
22	INDUCTOR-FB,50,	INDUCTOR_FB	L1-L8	8

NO.	Part Name - Value FAIR RITE	Jedec Type	Ref Des	Qty
23	LED10-RED,25MA,2.1V	DIP20_LED	U2	1
24	MC100ELT21_SOIC-BASE	SOIC8	U4,U17	2
25	OSC_TTL_DIP-20.0000MHZ,100 PPM	CRYS14	Y2	1
26	OSC_TTL_DIP-49.152MHZ,32/50 PPM	CRYS14	Y1	1
27	PIC16C74-BASE	PIC16C74	U1	1
28	PWRBLOCK_2-BASE	CONN2END	J1	1
29	QDSX-BASE	PQFP128	U24	1
30	RESISTOR-10K,5%	SMDRES805	R1,R9,R12-R15,R60	7
31	RESISTOR-121,1%	SMDRES805	R20-R23	4
32	RESISTOR-196,1%	SMDRES805	R8,R11	2
33	RESISTOR-2.7,5%	SMDRES805	U13-U16	4
34	RESISTOR-316K,1%	SMDRES805	R36-R39	4
35	RESISTOR-357,1%	SMDRES805	R24-R27	4
36	RESISTOR-4.7K,5%	SMDRES805	R3-R7,R18,R19	7
37	RESISTOR-47,5%	SMDRES805	R16,R17,R28,R29	4
38	RESISTOR-68.1,1%	SMDRES805	R2,R10	2
39	RES_ARRAY_15_SMD-10K	SOIC16	RN1,RN3,RN4	3
40	RES_ARRAY_15_SMD-4.7K	SOIC16	RN5	1
41	RES_ARRAY_8_SMD-270	SOIC16	RN2	1
42	SMA-BASE	SMA	J7,J8	2
43	T1008-BASE	T1008	T1,T2	2
44	TST_PT-BASE	TST_PT_1	TP1-TP10	10

APPENDIX C: SCHEMATICS

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

DECODE LOGIC



DECOUPLING CAPS FOR DECODING LOGIC

PLACE DECOUPLING CAPS CLOSE TO THE POWER PINS

DRAWING

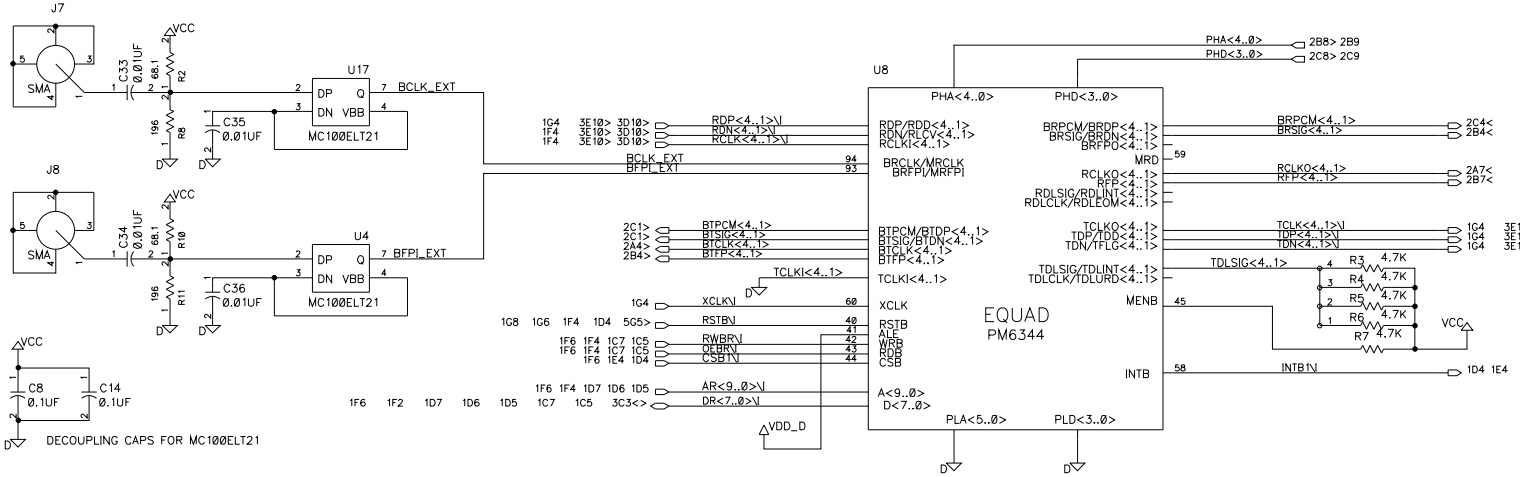
TITLE=DECODE LOGIC
ABBREV=DECODE
LAST_MODIFIED=Tue Oct 8 13:29:38 1996

PMC-Sierra, Inc.

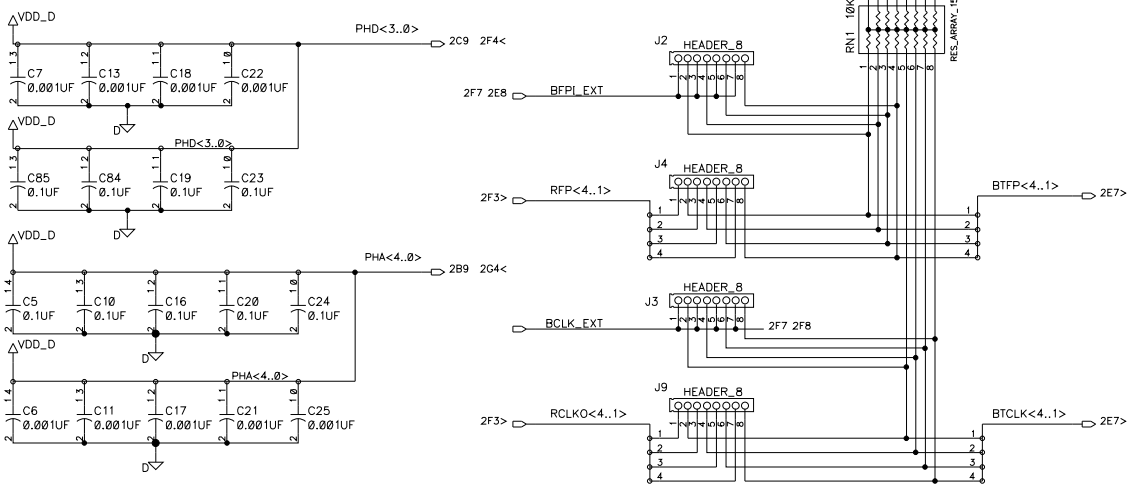
DOCUMENT NUMBER: PMC-960911	ISSUE: 1
TITLE: EQUAD WITH QDSX REFERENCE DESIGN DECODE LOGIC	DATE: SEP. 9, 1996
ENGINEER: AARON GILROY	PAGE: 5 OF 5

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

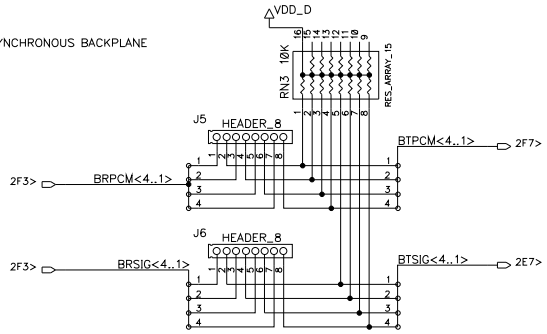
QUAD E1 FRAMER



NOTE: PLACE ALL DECOUPLING CAPS
NEAR POWER PINS



HEADER BLOCK FOR SYNCHRONOUS BACKPLANE



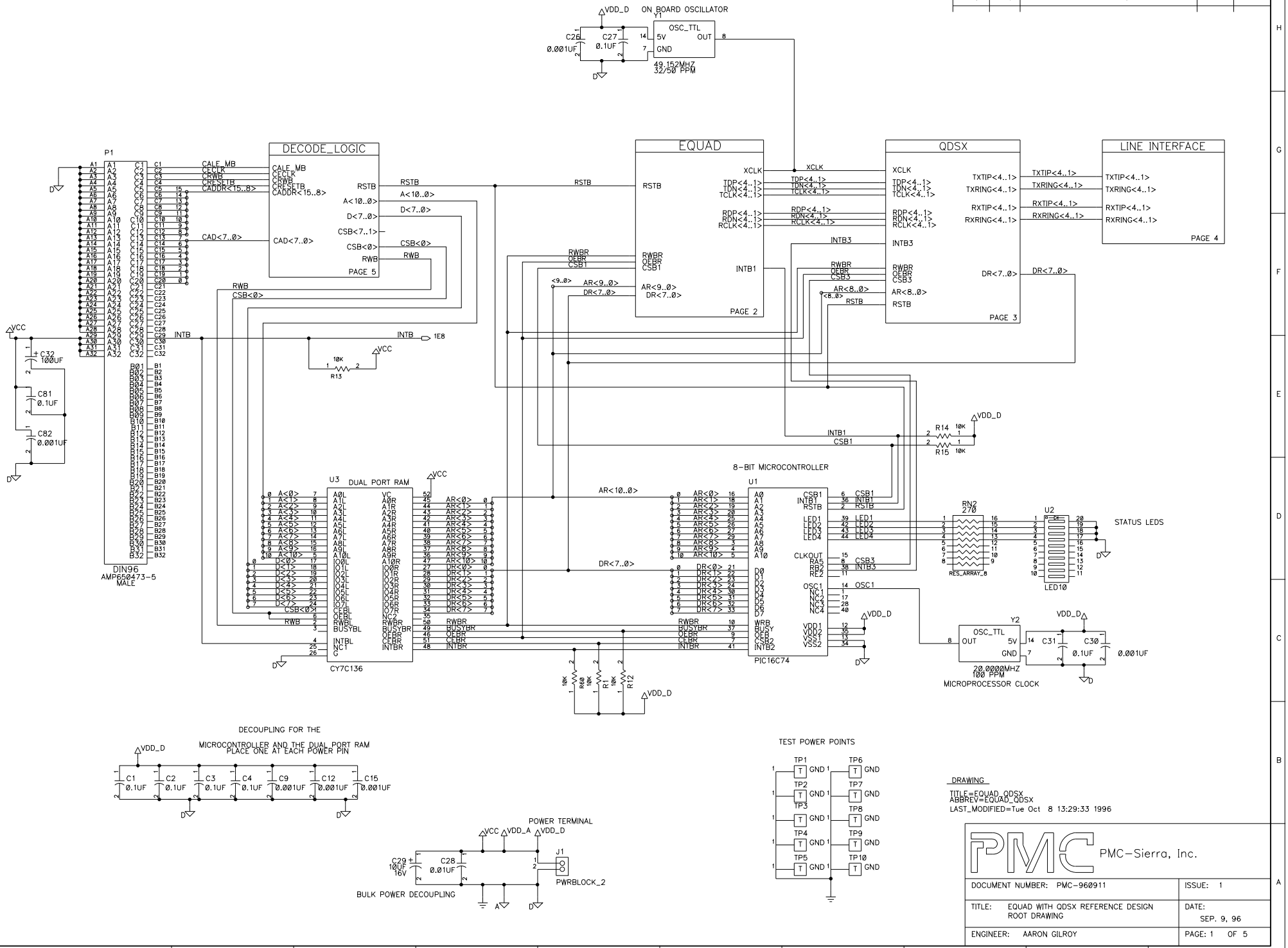
DRAWING

TITLE=EQUAD_BLOCK
ABBREV=EQUAD
LAST_MODIFIED=Tue Oct 8 13:29:47 1996

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-960911	ISSUE: 1
TITLE: EQUAD WITH QDSX REFERENCE DESIGN EQUAD	DATE: SEP. 9, 96
ENGINEER: AARON GILROY	PAGE: 2 OF 5

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING

TITLE=EQUAD_QDSX
ABBREV=EQUAD_QDSX
LAST_MODIFIED=Tue Oct 8 13:29:33 1996

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DOCUMENT NUMBER: PMC-960911	ISSUE: 1
TITLE: EQUAD WITH QDSX REFERENCE DESIGN ROOT DRAWING	DATE: SEP. 9, 96
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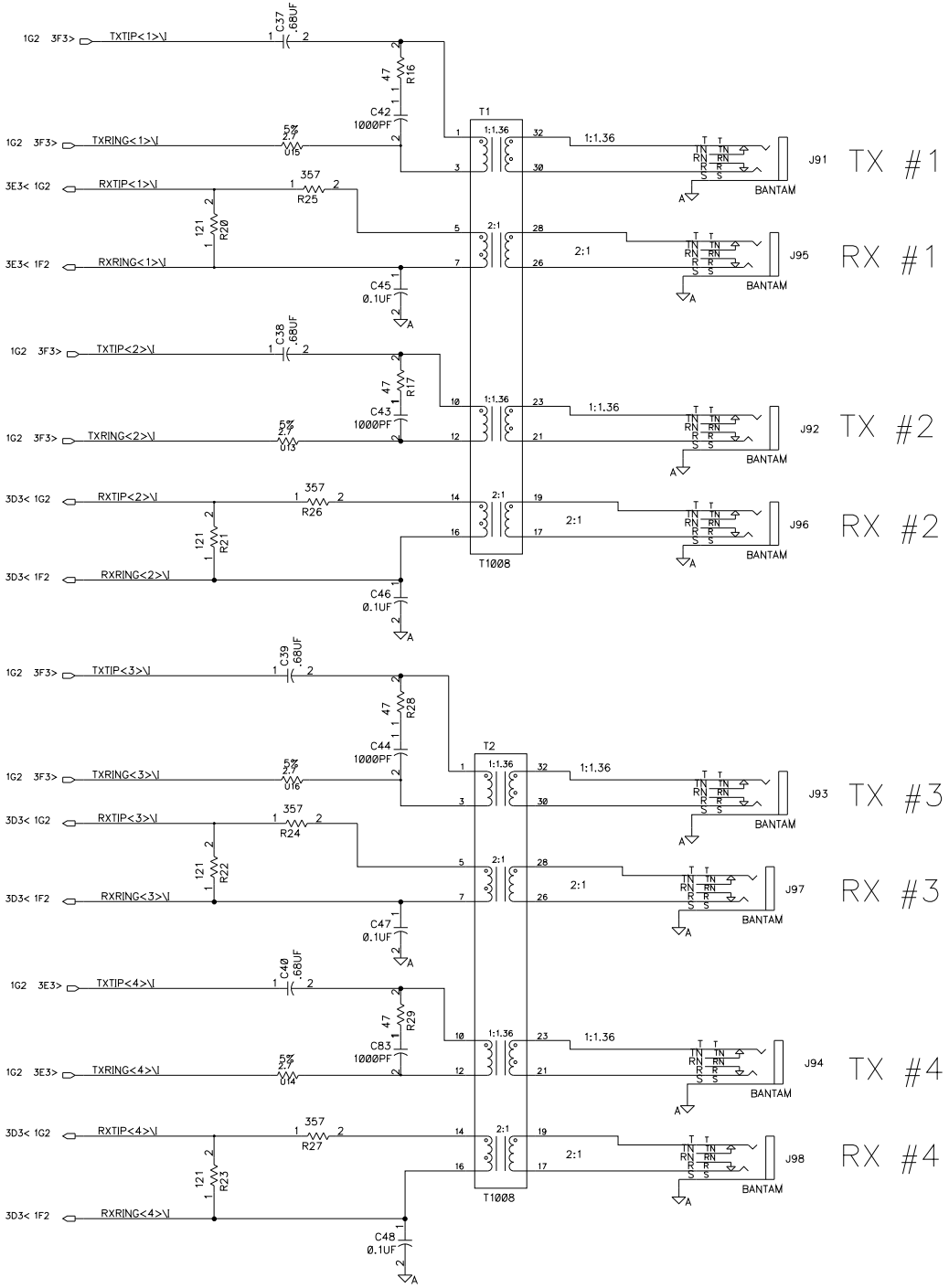

LINE INTERFACE TRANSMIT/RECEIVE

DRAWING
TITLE=LINE_INTERFACE
ABBREV=LIU

LAST_MODIFIED=Tue Oct 8 13:29:51 1996

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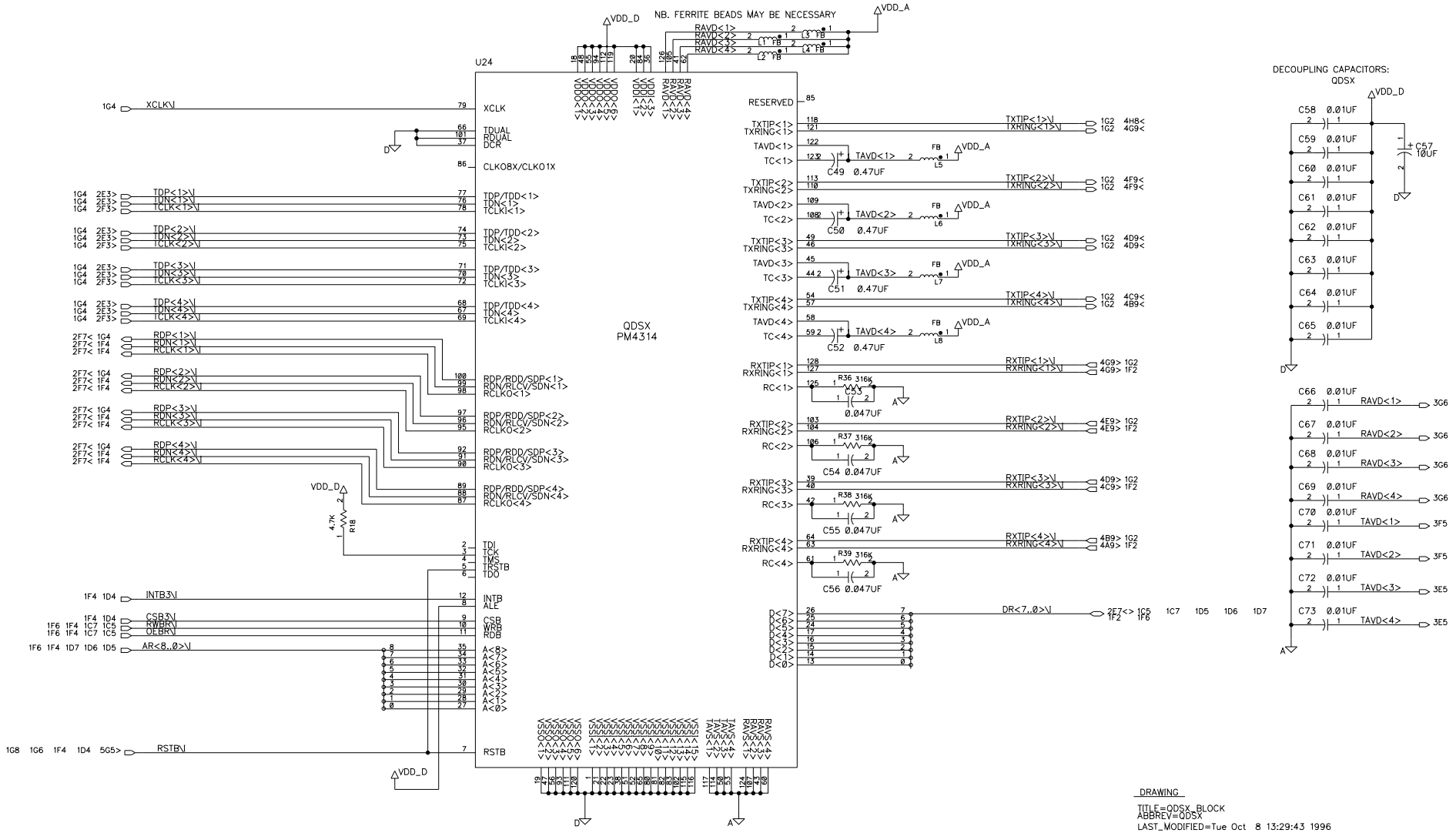
QDSX



DRAWING

TITLE=QDSX_BLOCK
ABBREV=QDSX
LAST_MODIFIED=Tue Oct 8 13:29:43 1996

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