# PM5312 & PM5344

## PATH OVERHEAD PROCESSING AND PAYLOAD ALIGNMENT OF AN STS-12C STREAM

# APPLICATION NOTE

## ISSUE 2: SEPTEMBER 1997

## CONTENTS

## LIST OF FIGURES

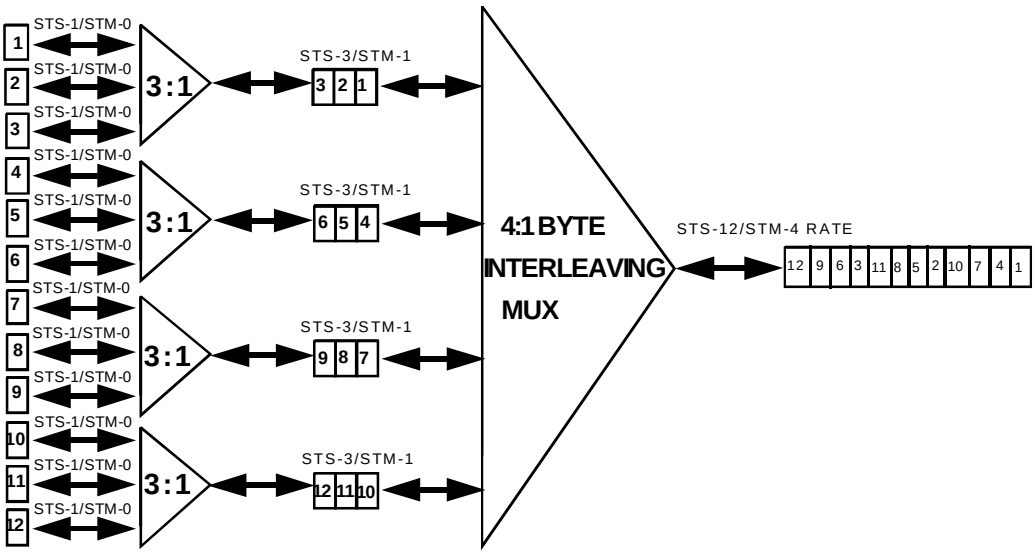
# 1 OVERVIEW

This application note describes the external circuitry required to adapt the PM5312 (STTX) and PM5344 (SPTX) standard products to allow processing of a byte serial STS-12c/STM-4c stream. In order to understand this circuitry it is worthwhile to understand the STS-12c/STM-4c multiplexing structure and terminology of the SONET/SDH signals.

In the rest of this application note, unless specifically referred, the reference to an STS-N/STM-N signal also includes STS-Nc/STM-Nc.

The multiplexing structure is shown below in figure 1. Each of the constituent STS-1/STM-0 streams are byte interleaved in a two stage process. In the first stage the STS-1/STM-0 streams (number 1 to 3, 4 to 6, etc.) are byte interleaved by sequentially interleaving a byte from one stream followed by a byte from the next stream working in a vertical manner. This yields four data streams at three times the byte rate as the 12 original STS-1/STM-0 streams. These are referred to as STS-3/STM-1. In the second stage the multiplexing is done in a very similar manner, again by sequentially interleaving a byte from one stream followed by a byte from the next stream while working in a vertical manner. This yields one data stream operating at four times the byte rate as the four original STS-3/STM-1 streams and is referred to as STS-12/STM-4.

**Figure 1 - Two Stage Interleaving Of STS-1 To STS-12**



In the reverse direction, the STS-12/STM-4 data rate can be converted back to the STS-1/STM-0 rate by a demultiplexing process that unwinds the byte interleaving process described above. The diagram of figure 1 depicts both directions.

The PM5312 (STTX) can be programmed to operate in full duplex as the first stage of the multiplexing architecture (operating as a STS-3:STS-1 mux/demux) or the second stage of the multiplexing architecture (operating as a STS-12:STS-3 mux/demux) as shown diagramatically in figure 1. The STTX has a third mode (operating as a STS-1:STS-1 mux/demux) of operation where it acts as a simple 1:1 multiplexer/demultiplexer with in-built transport overhead termination ability. This third mode is not the scope of this application note and will be ignored in the rest of this document.

When operating as the first stage of multiplexing/demultiplexing, the STTX interfaces to a single incoming byte serial STS-3/STM-1 stream and coverts it to three separate outgoing byte serial STS-1/STM-0 streams . In the reverse direction it converts the three incoming byte serial STS-1/STM-0 streams to a single byte serial STS-3/STM-1 outgoing stream.

When operating as the second stage of multiplexing/demultiplexing, the STTX interfaces to a single incoming byte serial STS-12/STM-4 stream and coverts it to four separate outgoing byte serial STS-3/STM-1 streams . In the reverse direction it converts the four incoming byte serial STS-3/STM-1 streams to a single byte serial STS-12/STM-4 outgoing stream.

Aside from the multiplexing/demultiplexing functionality of the STTX, there is also built-in processing for termination of Section (regenerator section) and Line (multiplex section) overheads. The appropriate transport overhead bytes are automatically terminated in each mode of operation and the overhead indications/alarms and serial ports must be utilized accordingly for each mode of operation as shown in the PM5312 data book.

The PM5344 (SPTX) standard product terminates the path overhead of the received SONET/SDH signal and also provides a decoded COMBUS interface on the output buses. The COMBUS interface multifunction control signal (e.g. DC1J1V1) and payload signal (e.g. DPL) totally defines the frame alignment, SPE alignment and tributary multiframe alignment on the outgoing SONET/SDH buses.

The rest of this application note describes two options that show how (by using the discussed functionality of the STTX and SPTX) to accomplish the Path Overhead processing, Transport Overhead processing and payload alignment of a byte serial STS-12c/STM-4c stream. The first option, (OPTION1), describes a

system where the line and the node are completely decoupled because the node has an independent timing source compared to the synchronization of the line clock. The second option, (OPTION2), describes a system where the line and the node are not decoupled and run off the same clock source. Option1 requires more complex external circuitry than option2.

# 2 OPTION 1:

Option 1 is covered by figure 2 and figure 3. Figure 2 shows the receive direction and utilizes the receive circuitry of an STTX (1/2 STTX block) and the receive circuitry of two separate SPTX's (1/2 SPTX #1 and 1/2 SPTX #2) plus some glue logic. The other half of the STTX, SPTX #1 and SPTX #2 are utilized in the transmit circuitry shown in figure 3.

## 2.1 Receive Operation With Decoupled Timing

In this architecture, the receive circuitry of the STTX (1/2 STTX) and the "Alignment" section runs synchronous to the line clock rate, at a frequency f1. The magnitude of f1 is a divide by 32 of the line rate and is nominally 19.44MHz. The "Parity Check" section runs synchronous to a system clock of frequency f2, varying by no more than 20ppm relative to the line clock rate. The "Decoupling" section runs sychronous to both f1 and f2 and uses a FIFO to transfer data from the f1 domain to the f2 domain.

The STTX interfaces to an STS-12c byte serial input stream and demultiplexes this stream to four STS-3c rate outputs. The STS-3c on output ROUT1[7:0] contains a complete STS-3c with valid pointers in the H1 and H2 locations. The remaining outputs on ROUT2[7:0], ROUT3[7:0] and ROUT4[7:0] contain the demultiplexed bytes of the original STS-12c and contain concatenation indicator values in the H1 and H2 locations. The remaining circuitry consists of three main stages, consisting of an "Alignment" stage, a "Decoupling" stage and a "Parity Check" stage. These three stages are described in more detail below.

### 2.1.1 Alignment:

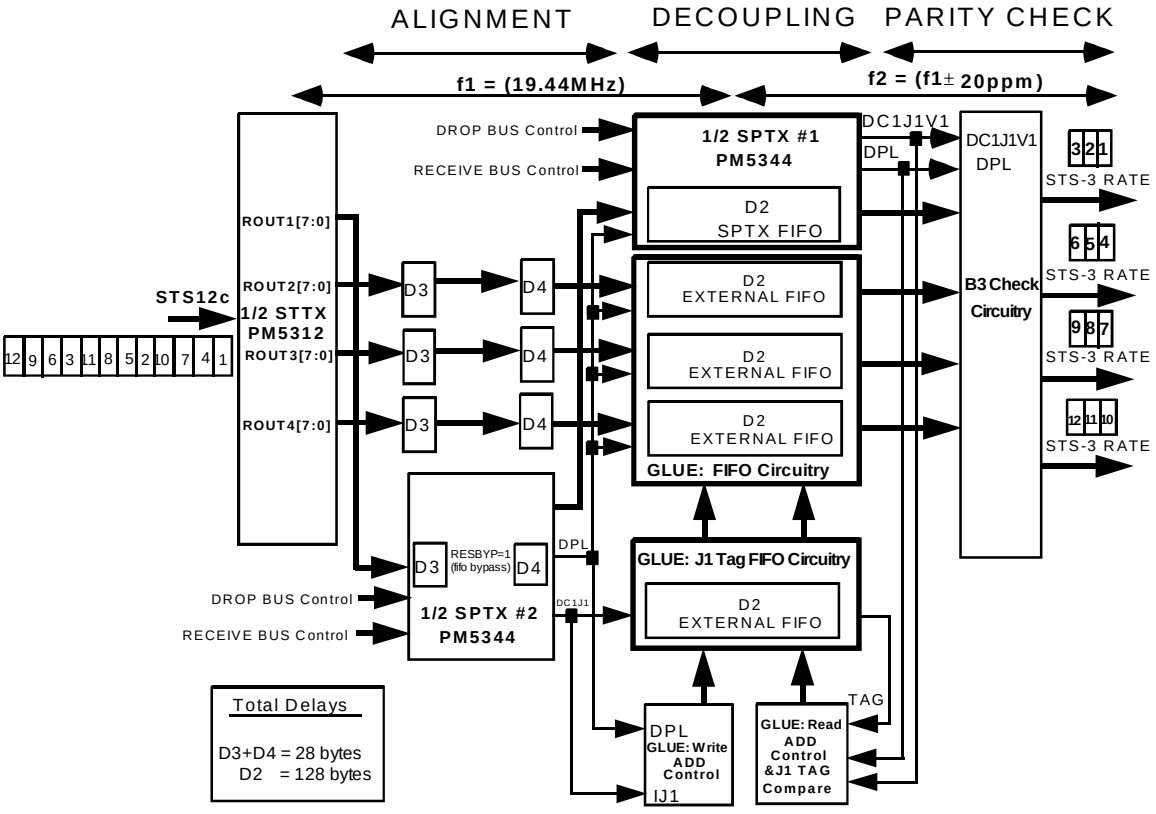
At the input of this stage the STTX outputs contain all the STS-12c data but do not have any known output alignment to distinguish payload bytes from overhead bytes. The "1/2 SPTX #2" block interfaces to the STS-3c output on ROUT1[7:0] and decodes the alignment of the payload bytes with respect to the overhead bytes by decoding the IFP input of the SPTX and the H1 and H2 bytes within the SONET signal. The decoded DPL and DC1J1V1 outputs completely define the location of the SPE and transport overhead bytes on the four STS-3c rate outputs. Since the "1/2 SPTX #2" block is in FIFO bypass, the total inherent delay through this block is D3+D4 (28 PICLK clock cycles as indicated in figure 32 of the SPTX's data book). To compensate for this delay the delay elements D3 and D4 must be placed on the ROUTn[7:0] (n = 2, 3 and 4) data outputs of the "1/2 STTX" block.

Besides determining the SPE alignment, SPTX #2 also terminates the path overhead.

The "RECEIVE BUS Control" interface refers to the PICLK and IFP inputs of the SPTX. The PICLK and IFP "RECEIVE BUS Control" inputs of SPTX #2 should be connected to the ROCLK and ROFP outputs of the STTX respectively.

The "DROP BUS Control" interface consists of the DCK and DFP inputs of SPTX #2. The DCK input of this SPTX should be connected to the line clock (frequency f1) and the DFP input of SPTX #2 should be pulled down to a logic 0.

**Figure 2 - STS-12c Receive Direction With Independent System & Line Timing**




## 2.1.2 Decoupling:

This stage of the circuitry decouples the line synchronous clocks and the system synchronous clocks by utilizing external FIFO's and a second SPTX. The "1/2

SPTX #1" block accomplishes the rate decoupling and path overhead termination on the STS-3c byte serial stream of the ROUT1[7:0] outputs. SPTX #1 is programmed in external path termination mode since it is only used as a decoupling element. The other three STS-3c streams are rate decoupled by the "External FIFO" sub block of the "FIFO Circuitry" block. There is no path overhead to terminate on the byte serial streams of the ROUT2[7:0], ROUT3[7:0] and ROUT4[7:0] outputs. The "External FIFO" block is a simple 128 byte deep FIFO and is necessary to mimic the FIFO and fixed intrinsic delays (which amount to a total sum equal to D2) of the SPTX.

The "write" addresses to the external FIFO'S are generated by a simple sequencer generated from a 4 bit count value. This sequencer has the added ability to set the bit in the "J1 TAG FIFO circuitry" at the address being addressed when the J1 indication is detected on its DPL and DC1J1V1 inputs. The J1 indication is simply the logical AND of the DPL and DC1J1V1 signals (when the DISV1 bit of register 00H in the SPTX is set to logic 1).

The "read" address generator is primed to the address at which the J1 TAG exists (in the "J1 TAG FIFO Circuitry") when the J1 indication is detected on the DC1J1V1 and DPL outputs of the "1/2 SPTX #1" block. Again, the J1 indication is simply the logical AND of the DPL and DC1J1V1 signals (when the DISV1 bit of register 00H in the SPTX is set to logic 1).

The "RECEIVE BUS Control" interface refers to the PICLK, RC1J1V1 and RPL inputs of SPTX #1. The PICLK, RC1J1V1 and RPL "RECEIVE BUS Control" inputs of SPTX #1 should be connected to the ROCLK (from STTX), DC1J1V1 (from SPTX #2) and DPL (from SPTX #2) respectively.

The "DROP BUS Control" interface consists of the DCK and DFP inputs of SPTX #1. The DCK input of this SPTX should be connected to the system clock (frequency f2) and the DFP input of SPTX #1 should be pulled down to logic low.

### 2.1.3 Parity Check:

This stage of the circuitry checks the BIP-8 B3 parity errors over the complete STS-12c SPE. The B3 BIP-8 calculation is performed over the entire SPE bytes (identified by DPL) and is compared to the B3 byte received in the following frame. The B3 byte within the frame can be identified by using the DC1J1V1 and DPL outputs of the SPTX; the B3 byte location is 270 bytes after the AND operation of the DC1J1V1 and DPL yields a logic 1.

## 2.2 Transmit Direction With Decoupled Timing

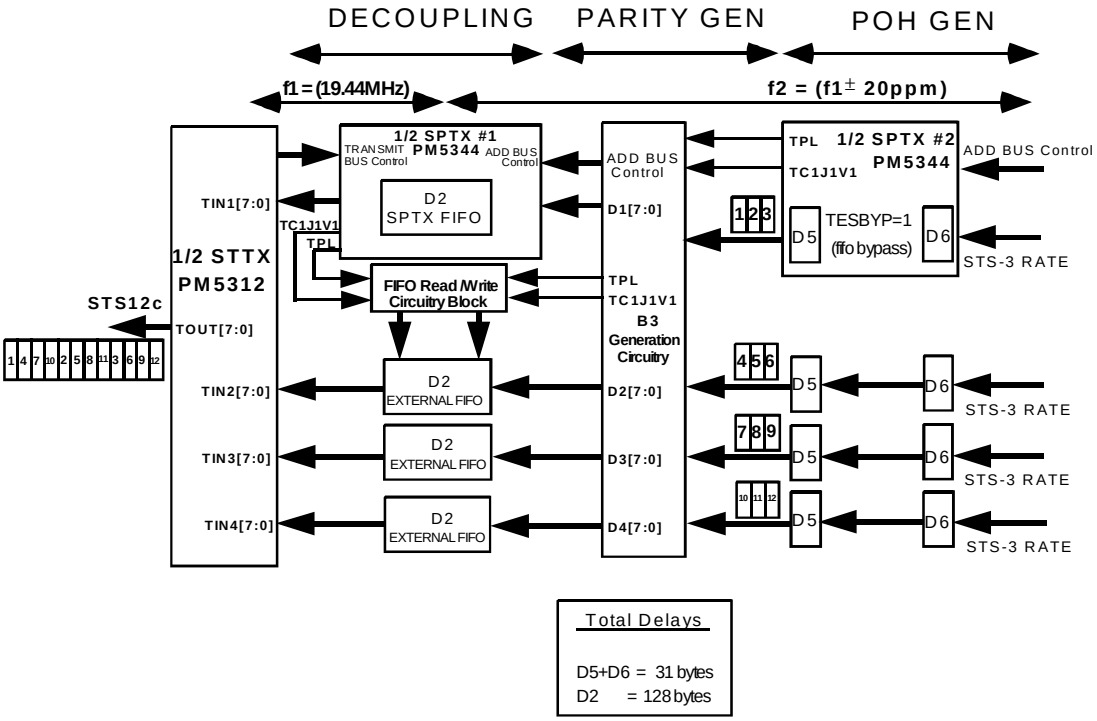
In this architecture the transmit circuitry of the STTX (1/2 STTX) runs synchronous to the line clock rate at a frequency f1. The magnitude of f1 is derived from the line interface and is nominally 19.44MHz. The "Parity Gen" and "POH Gen" sections runs synchronous to a system clock of frequency f2, varying by no more than 20ppm relative to the line clock rate. The "Decoupling" section runs sychronous to both f1 and f2 and uses a FIFO to transfer data from the f2 domain to the f1 domain.

The STTX interfaces to four byte serial STS-3c input streams and multiplexes them to a single byte serial STS-12c stream. The STS-3c on input TIN1[7:0] contains a complete STS-3c with valid pointers in the H1 and H2 locations. The remaining inputs on TIN2[7:0], TIN3[7:0] and TIN4[7:0] contain the bytes that make up the rest of the STS-12c and contain no valid pointers. The remaining circuitry consists of three main stages, a "POH GEN" stage, a "Parity Generation" stage and a "Decoupling" stage. These three stages are described in more detail below.

### 2.2.1 POH Gen:

This stage of the circuitry generates the path overhead (with the exception of the B3 byte) and provides alignment indications DC1J1V1 and DPL to the B3 generation circuitry. At this point all four STS-3 rate signals are assumed to be aligned such that the STTX can perform the multiplexing function. The SPTX (1/2 SPTX #2) has its V1 pulse on the DC1J1V1 inhibited by writing the DISV1 bit in register 00H. This is done to make the decoding of the J1 pulse simpler downstream. The "ADD BUS Control" interface includes the ACK, AC1J1V1 and the APL inputs.

**Figure 3 - STS-12c Transmit Direction With Independent System & Line Timing**




These inputs must be appropriately asserted in reference to the AD[7:0] data input on the STS-3c stream. Since the "1/2 SPTX #2" block is in FIFO bypass, the total inherent delay through this block is D5+D6 (31 ACK clock cycles as indicated in figure 35 of the SPTX's data book). To compensate for this delay the delay elements D5 and D6 must be placed on the other three STS-3 rate inputs.

It is assumed that the H1 and H2 byte locations on the STS-3 rate inputs to the "POH GEN" stage contain valid pointer and concatenation indicator bytes.

### 2.2.2 Parity Gen:

This stage of the circuitry generates BIP-8 B3 byte over the entire SPE payload of an STS-12c that is contained in the four byte serial STS-3 rate streams. The SPE bytes are identified by the DPL output of the SPTX. The calculated BIP-8 code is inserted into the B3 byte of the following SONET frame. The B3 byte within the frame can be identified by using the DC1J1V1 and DPL outputs of the SPTX; where the B3 byte location is 270 bytes after the AND operation of the DC1J1V1 and DPL yields a logic 1. For correct alignment at the inputs of the "decoupling" block, the DPL, DC1J1V1, ADD BUS Control and Dn[7:0] outputs

must all go through the same inherent delay through the "B3 Generation Circuitry".

### 2.2.3 Decoupling:

This stage of the circuitry acts exactly as the "Decoupling" stage of the receive side circuitry. The "FIFO Read Write" block is identical to the "Write ADD Control", "Read ADD Control & J1 TAG Compare" and "J1 TAG FIFO Circuitry" blocks on the receive side.

# 3 OPTION 2:

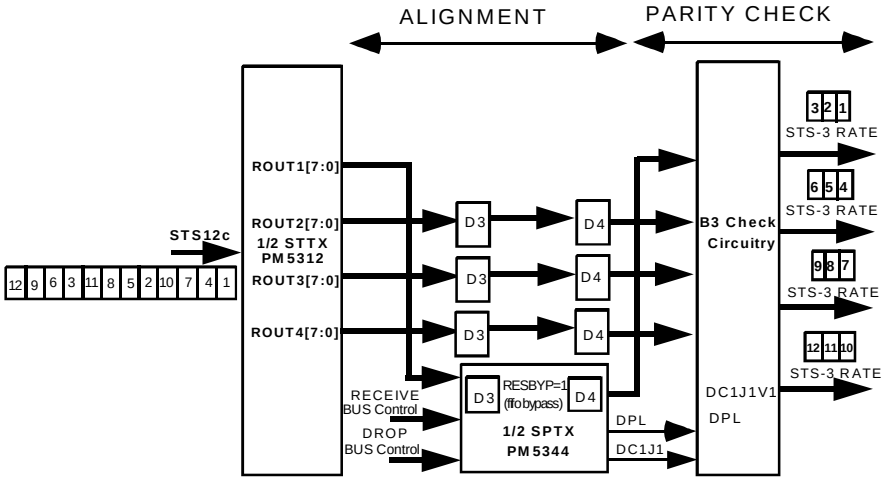
Option 2 is covered by figure 4 and figure 5. Figure 4 shows the receive direction and utilizes the receive circuitry of an STTX (1/2 STTX block) and the receive circuitry of an SPTX (1/2 SPTX) plus some glue logic. The other half of the STTX, SPTX are utilized in the transmit circuitry shown in figure 5.

Except for the "Decoupling" stage, which has been deleted for this option, all circuitry is identical to the circuitry used in option 1. Description of the "Alignment", "Parity Check", "Parity Gen" and "POH Gen" blocks in option 1 apply identically to option 2.

## 3.1 Receive Operation Without Decoupled Timing

See description of "Alignment" and "Parity Check" blocks in the "Receive Operation With Decoupled Timing" section.

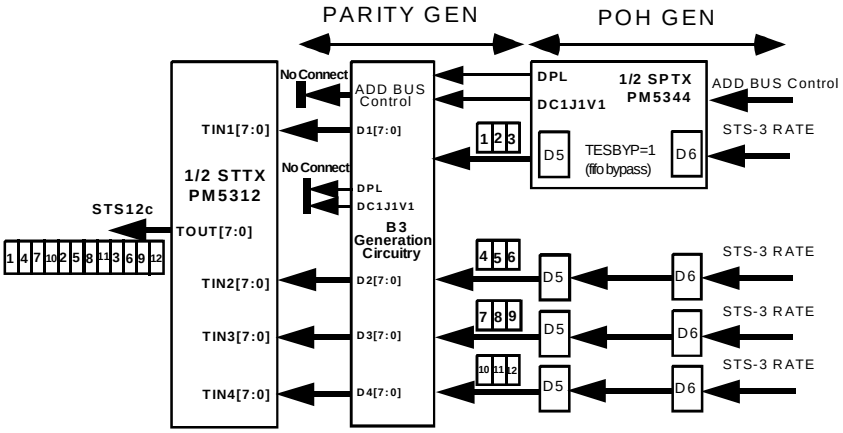
**Figure 4 - STS-12c Receive Direction With System & Line Both Coupled To The Same Clock**




## 3.2 Transmit Operation Without Decoupled Timing

See description of "Parity Gen" and "POH Gen" blocks in the "Transmit Operation With Decoupled Timing" section.

## Figure 5 - STS-12c Receive Direction With System & Line Both Coupled To The Same Clock



# 4 REFERENCES

1. PMC-Sierra data book PM5344 (SPTX), May 1995.
2. PMC-Sierra data book PM5312 (STTX), November 1993.

## NOTES

## CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com



PMC-950737 (R2) Issue date: September 1997