PM5345

S/UNI-155™

PECL OUTPUT TERMINATIONS

APPLICATION NOTE

ISSUE 3: SEPTEMBER 1997

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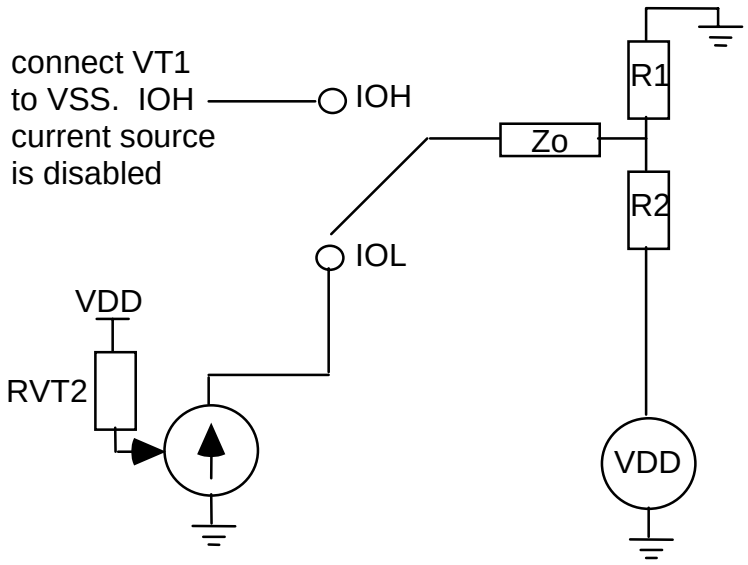
1 WHAT TERMINATION IS RECOMMENDED FOR THE PECL OUTPUTS ?

In a typical application, only the PECL data outputs (TXD+, and TXD-) are used. The TXCO+ and TXCO- outputs are left open. For this case, two termination schemes are possible. The first scheme is described in the PM5345 datasheet (see the application examples section), and involves calculating RVT1 and RVT2 values based on the required PECL output levels and the termination impedance. We have observed that the signal waveform shapes associated with this termination can be improved by the following modification:

Figure 1 -



The IOH current source is disabled by tying VT1 to VSS. R1 and R2 provide two functions:

1. the voltage divider set up by R1 and R2 sets the PECL output high voltage (nominally 4.2V for VDD = 5V).

2. the Thevenin equivalent impedance of R1 and R2 terminates the transmission line.

In addition, the equation used to calculate RVT2 is changed from the equation in the datasheet. The new equation becomes:

RVT2 = 12.564*Zo where Zo is the characteristic impedance in Ω

For a 100 Ω characteristic impedance transmission line, recommended resistor values are:

Table 1 -

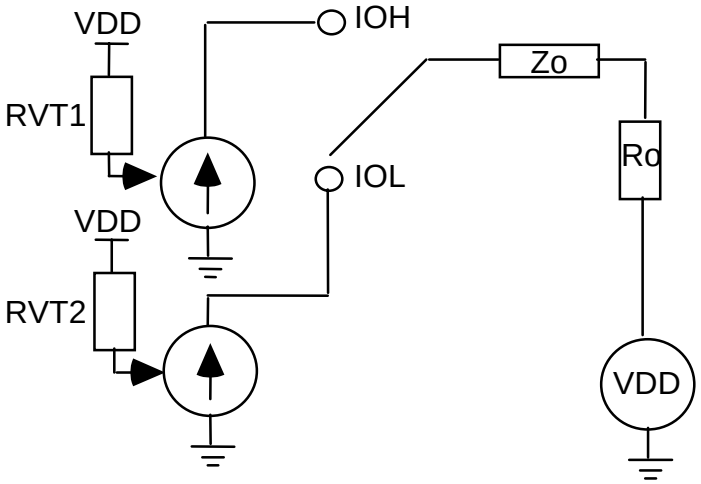
R1	626 Ω
R2	120 Ω
RVT2	1260 Ω

This termination is recommended for all new designs, and must be used if both PECL output pairs (clock and data) are used in an application.

How do the PM5345 PECL outputs operate?

The PECL outputs, TXD+, TXD-, TXCO+, and TXCO-, are implemented using CMOS technology, and can be modeled as ideal current sources. This is the dual of a traditional ECL output which is typically modeled as a voltage source. The output high and low currents (IOH and IOL) are set using resistors RVT1, and RVT2. IOH and IOL generate the output high and low voltages across the termination resistor, RO.

Figure 2 -



The advantage of this method is that the PECL output levels (VOH and VOL) are independent of variations in the VDD supply rail, and true PECL output levels are achieved across the complete VDD voltage range (4.75 to 5.25 V). The output

levels will of course be affected by variations in RVT1 and RVT2, as well as the terminating resistor, Ro.

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CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place,
Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

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