

## FEATURES

- **16-Bit Monotonic Over Temperature**
- **Low Glitch Impulse: 2nV-s**
- **Low Noise: 30nV/√Hz**
- **Buffered Rail-to-Rail Voltage Output**
- Low Power: 50mW from ±5V Supplies
- Unipolar or Bipolar Output
- 4-Quadrant Multiplying Capability
- Asynchronous Clear to User-Defined Voltage
- Power-On Reset
- Three-Wire SPI and MICROWIRE™ Compatible Serial Interface
- Schmitt Trigger On CLK Input Allows Direct Optocoupler Interface
- 16-Pin Narrow SO Package

## APPLICATIONS

- Industrial Process Control
- Precision Industrial Equipment
- Waveform Generation
- Automatic Test Equipment
- High Resolution Offset and Gain Adjustment

## DESCRIPTION

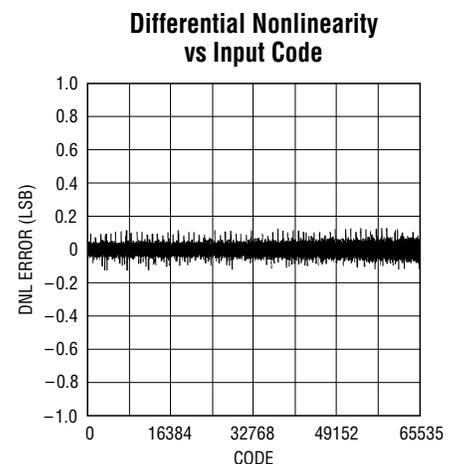
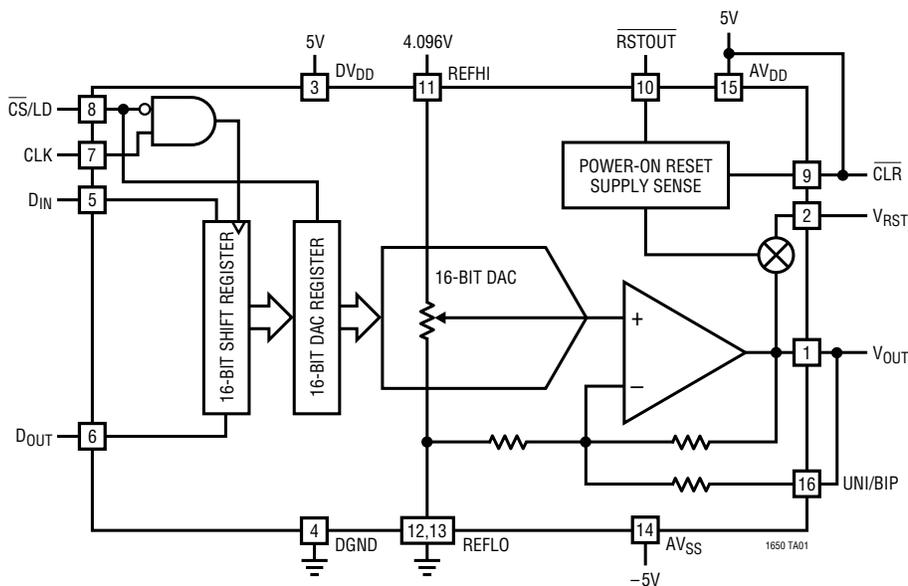
The LTC1650 is a deglitched rail-to-rail voltage output 16-bit digital-to-analog converter (DAC) available in a 16-pin narrow SO package. It has 16-bit monotonicity over temperature and includes a rail-to-rail output buffer amplifier and an easy to use three-wire cascadable serial interface. The LTC1650 operates with dual ±5V supplies.

The LTC1650 has excellent accuracy over its full operating temperature range along with very low power dissipation of 50mW with dual ±5V supplies. This, along with the small outline package, makes it the most flexible high resolution digital-to-analog converter available today.

The LTC1650 has a fast settling time of 4μs to 16 bits and a low midscale glitch of under 2nV-s. This makes the LTC1650 ideal for waveform generation or other applications where output dynamic performance is important.

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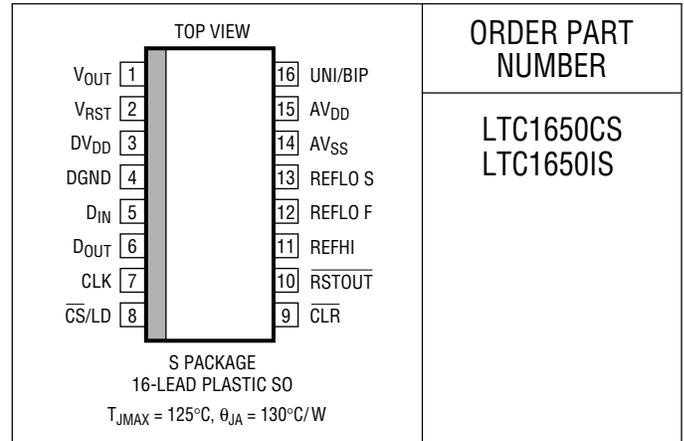
## TYPICAL APPLICATION



## ABSOLUTE MAXIMUM RATINGS

|  |                           |
|--|---------------------------|
| $AV_{DD}$ , $DV_{DD}$ to DGND .....        | -0.5V to 7.5V             |
| TTL Input Voltage .....                    | -0.5V to 7.5V             |
| $V_{OUT}$ , $V_{RST}$ .....                | -0.5V to $AV_{DD} + 0.5V$ |
| $AV_{SS}$ .....                            | 0.5V to -7.5V             |
| Operating Temperature Range                |                           |
| LTC1650C .....                             | 0°C to 70°C               |
| LTC1650I .....                             | -40°C to 85°C             |
| Maximum Junction Temperature .....         | 125°C                     |
| Storage Temperature Range .....            | -65°C to 150°C            |
| Lead Temperature (Soldering, 10 sec) ..... | 300°C                     |

## PACKAGE/ORDER INFORMATION



Consult factory for PDIP, A grade and Military grade parts.

## ELECTRICAL CHARACTERISTICS

$AV_{DD} = 4.75V$  to  $5.25V$ ,  $AV_{SS} = -4.75V$  to  $-5.25V$ ,  $DV_{DD} = 4.75V$  to  $5.25V$ ,  $REFLO = 0V$ ,  $REFHI = 4.096V$ ,  $V_{OUT}$  unloaded,  $T_A = T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.

| SYMBOL   | PARAMETER                                | CONDITIONS                                  | MIN | TYP   | MAX  | UNITS             |       |
|--|--|---|-----|-------|------|-------------------|-------|
| <b>DAC Characteristics, Unipolar/Bipolar Output Unless Otherwise Noted</b> |  |   |     |       |      |                   |       |
|  | Resolution                               |   | ●   | 16    |      | Bits              |       |
|  | Monotonicity                             |   | ●   | 16    |      | Bits              |       |
| DNL  | Differential Nonlinearity                | Guaranteed Monotonic (Note 1)               | ●   | ±0.15 | ±0.9 | LSB               |       |
| INL  | Integral Nonlinearity                    | Integral Nonlinearity (Note 1)              | ●   | ±4    | ±16  | LSB               |       |
|  | Bipolar Zero Error                       | $T_A = 25^{\circ}C$                         |     | ±5    | ±12  | LSB               |       |
|  | Bipolar Zero Error                       | $T_A = T_{MIN}$ to $T_{MAX}$                | ●   |       | ±18  | LSB               |       |
| $V_{OS}$   | Unipolar Offset Error                    | $T_A = T_{MIN}$ to $T_{MAX}$                | ●   | ±0.5  | ±12  | LSB               |       |
| $V_{OS}TC$   | Offset Error Temperature Coefficient     |   |     | ±10   |      | $\mu V/^{\circ}C$ |       |
|  | Gain Error                               | $T_A = 25^{\circ}C$                         |     | ±4    | ±12  | LSB               |       |
|  | Gain Error                               | $T_A = T_{MIN}$ to $T_{MAX}$                | ●   |       | ±18  | LSB               |       |
|  | Gain Error Temperature Coefficient       |   |     | ±0.05 |      | LSB/ $^{\circ}C$  |       |
|  | Bipolar Negative Full-Scale Error        | $T_A = 25^{\circ}C$                         |     | ±1    | ±12  | LSB               |       |
|  | Bipolar Negative Full-Scale Error        | $T_A = T_{MIN}$ to $T_{MAX}$                | ●   |       | ±16  | LSB               |       |
|  | Bipolar Negative Full-Scale Error Tempco |   |     | ±10   |      | $\mu V/^{\circ}C$ |       |
| <b>Power Supply Characteristics</b>  |  |   |     |       |      |                   |       |
| $AV_{DD}$  | Positive Supply Voltage                  |   | ●   | 4.75  | 5.0  | 5.25              | V     |
| $DV_{DD}$  | Positive Supply Voltage                  |   | ●   | 4.75  | 5.0  | 5.25              | V     |
| $AV_{SS}$  | Negative Supply Voltage                  |   | ●   | -4.75 | -5.0 | -5.25             | V     |
| $I_{AVDD}$   | $AV_{DD}$ Supply Current                 | $4.75V \leq AV_{DD} \leq 5.25V$ (Note 4)    | ●   |       | 5    | 7.5               | mA    |
| $I_{AVSS}$   | $AV_{SS}$ Supply Current                 | $-5.25V \leq AV_{SS} \leq -4.75V$ (Note 4)  | ●   | -7.5  | -5   |                   | mA    |
| $I_{DVDD}$   | $DV_{DD}$ Supply Current                 | $4.75V \leq DV_{DD} \leq 5.25V$ (Note 4)    | ●   |       | 0.02 | 0.1               | mA    |
| PSRR   | $AV_{DD}$ , $DV_{DD}$ Supply Rejection   | $4.75V \leq AV_{DD}$ , $DV_{DD} \leq 5.25V$ | ●   |       | 0.5  | 1.5               | LSB/V |
|  | $AV_{SS}$ Supply Rejection               | $-5.25V \leq AV_{SS} \leq -4.75V$           | ●   |       | 0.5  | 1.5               | LSB/V |

## ELECTRICAL CHARACTERISTICS

$AV_{DD} = 4.75V$  to  $5.25V$ ,  $AV_{SS} = -4.75V$  to  $-5.25V$ ,  $DV_{DD} = 4.75V$  to  $5.25V$ ,  $REFLO = 0V$ ,  $REFHI = 4.096V$ ,  $V_{OUT}$  unloaded,  $T_A = T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.

| SYMBOL                             | PARAMETER                                 | CONDITIONS                        |   | MIN            | TYP  | MAX      | UNITS           |
|------------------------------------|---|-----------------------------------|---|----------------|------|----------|-----------------|
| <b>Reference Input</b>             |   |                                   |   |                |      |          |                 |
| $R_{IN}$                           | Reference Input Resistance                |                                   | ● | 2.5            | 5    | 7.5      | k $\Omega$      |
|                                    | REFHI Range                               |                                   | ● | -4.0           | 4.0  | 4.5      | V               |
|                                    | REFLO Range                               |                                   | ● | -1.0           | 0    | 1.0      | V               |
| <b>Op Amp DC Performance</b>       |   |                                   |   |                |      |          |                 |
|                                    | Short-Circuit Current Low                 | $V_{OUT}$ Shorted to GND          | ● |                | 25   | 50       | mA              |
|                                    | Short-Circuit Current High                | $V_{OUT}$ Shorted to $V_{CC}$     | ● |                | 25   | 50       | mA              |
|                                    | Output Impedance                          | Measured at Midscale              |   |                | 0.15 |          | $\Omega$        |
| <b>AC Performance</b>              |   |                                   |   |                |      |          |                 |
|                                    | Voltage Output Slew Rate                  |                                   | ● | 0.8            | 2.0  |          | V/ $\mu$ s      |
|                                    | Voltage Output Settling Time              | (Note 3)                          |   |                | 4    |          | $\mu$ s         |
|                                    | Midscale Glitch Impulse                   |                                   |   |                | 1.8  |          | nV-s            |
|                                    | Digital Feedthrough                       |                                   |   |                | 0.05 |          | nV-s            |
|                                    | Output Noise Voltage Density              | 1kHz to 100kHz (Note 5)           |   |                | 30   |          | nV/ $\sqrt{Hz}$ |
| SINAD                              | Signal-to-Noise + Distortion Ratio        | REFHI = 1kHz 4V <sub>p-p</sub>    |   |                | 96   |          | dB              |
| <b>Digital I/O Characteristics</b> |   |                                   |   |                |      |          |                 |
| $V_{IH}$                           | Digital Input High Voltage                |                                   | ● | 2.4            |      |          | V               |
| $V_{IL}$                           | Digital Input Low Voltage                 |                                   | ● |                |      | 0.8      | V               |
| $V_{OH}$                           | Digital Output High Voltage               | $I_{OUT} = -1mA$ , $D_{OUT}$ Only | ● | $V_{CC} - 1.0$ |      |          | V               |
| $V_{OL}$                           | Digital Output Low Voltage                | $I_{OUT} = 1mA$ , $D_{OUT}$ Only  | ● |                |      | 0.4      | V               |
| $I_{LK}$                           | Digital Input Leakage                     | $V_{IN} = GND$ to $V_{CC}$        | ● |                |      | $\pm 10$ | $\mu A$         |
| $C_{IN}$                           | Digital Input Capacitance                 | (Note 2)                          |   |                |      | 10       | pF              |
| <b>Reset Characteristics</b>       |   |                                   |   |                |      |          |                 |
| $R_{ON}$                           | $V_{OUT}$ and $V_{RST}$ Switch Resistance | $V_{RST} = 0.5V$ (Note 6)         | ● |                | 200  | 500      | $\Omega$        |
|                                    | Threshold Voltage for Reset               | $AV_{DD}$ or $DV_{DD}$ (Note 7)   | ● | 1.5            | 2.5  | 3.2      | V               |
|                                    |   | $ AV_{SS} $ (Note 7)              | ● | 1.5            | 2.5  | 3.2      | V               |

## ELECTRICAL CHARACTERISTICS

$V_{DD} = 4.75V$  to  $5.25V$ ,  $V_{SS} = -4.75V$  to  $-5.25V$ ,  $DV_{DD} = 4.75V$  to  $5.25V$ ,  $REFLO = 0V$ ,  $REFHI = 4.096V$ ,  $V_{OUT}$  unloaded,  $T_A = T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.

| SYMBOL                           | PARAMETER                         | CONDITIONS         | MIN | TYP | MAX | UNITS |    |
|----------------------------------|-----------------------------------|--------------------|-----|-----|-----|-------|----|
| <b>Switching Characteristics</b> |                                   |                    |     |     |     |       |    |
| $t_1$                            | $D_{IN}$ Valid to CLK Setup       |                    | ●   | 40  |     | ns    |    |
| $t_2$                            | $D_{IN}$ Valid to CLK Hold        |                    | ●   | 0   |     | ns    |    |
| $t_3$                            | CLK High Time                     | (Note 2)           | ●   | 40  |     | ns    |    |
| $t_4$                            | CLK Low Time                      | (Note 2)           | ●   | 40  |     | ns    |    |
| $t_5$                            | $\overline{CS/LD}$ Pulse Width    | (Note 2)           | ●   | 50  |     | ns    |    |
| $t_6$                            | LSB CLK to $\overline{CS/LD}$     | (Note 2)           | ●   | 40  |     | ns    |    |
| $t_7$                            | $\overline{CS/LD}$ Low to CLK     | (Note 2)           | ●   | 20  |     | ns    |    |
| $t_8$                            | $D_{OUT}$ Output Delay            | $C_{LOAD} = 100pF$ | ●   | 5   | 45  | 150   | ns |
| $t_9$                            | CLK Low to $\overline{CS/LD}$ Low | (Note 2)           | ●   | 20  |     | ns    |    |
| $t_{10}$                         | CLR Pulse Width                   |                    | ●   | 50  |     | ns    |    |

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:** Nonlinearity is defined from code 0 to code 65535 (full scale) (end point INL, see Definitions section).

**Note 2:** Guaranteed by design. Not subject to test.

**Note 3:** To  $\pm 1$ LSB. Unipolar mode. DAC switched between all 1s and all 0s.

**Note 4:** Digital Inputs at 0V or  $DV_{DD}$ .

**Note 5:** Measured at  $V_{OUT}$ .  $REFHI = REFLO = 0V$ , unipolar mode.

**Note 6:** When part powers up or when it is reset, the output is connected to  $V_{RST}$  through this switch.

**Note 7:** Reset is active when any supply goes below this threshold.

## PIN FUNCTIONS

**$V_{OUT}$  (Pin 1):** The Rail-to-Rail Deglitched DAC Output.

**$V_{RST}$  (Pin 2):** The user-defined voltage to which the output gets reset when  $\overline{CLR}$  is active or when any of the supplies drop below 2.5V. The output will stay at this voltage until a new code is loaded into the DAC register.

**$DV_{DD}$  (Pin 3):** The Digital Positive Supply Input.  $4.75V \leq DV_{DD} \leq 5.25V$ . Requires a bypass capacitor to ground.

**DGND (Pin 4):** Digital Ground.

**$D_{IN}$  (Pin 5):** The TTL Level Input for the Serial Interface Data. Data on the  $D_{IN}$  pin is latched into the shift register on the rising edge of the serial clock. Data is loaded as one 16-bit word, MSB first.

**$D_{OUT}$  (Pin 6):** The output of the shift register that becomes valid on the rising edge of the serial clock.

**CLK (Pin 7):** The TTL Level Input for the Serial Interface Clock.

**$\overline{CS/LD}$  (Pin 8):** The TTL Level Input for the Serial Interface Enable and Load Control. When  $\overline{CS/LD}$  is low, the CLK signal is enabled so the data can be clocked in. When  $\overline{CS/LD}$  is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

**CLR (Pin 9):** The DAC is cleared to  $V_{RST}$  when this pin is pulled low. It should be logic high for normal operation.

**RSTOUT (Pin 10):** The logic output pin that goes active when any of the supplies drop below 2.5V. This pin is active low.

**REFHI (Pin 11):** The Reference Input Pin. The DAC is capable of 4-quadrant multiplying; this pin can swing from 4.5V to  $-4V$ .

**REFLO F/REFLO S (Pins 12, 13):** The Force and Sense Pin for the Lower Reference Input. This should nominally be tied to ground. This pin can swing from  $-1V$  to  $1V$ .

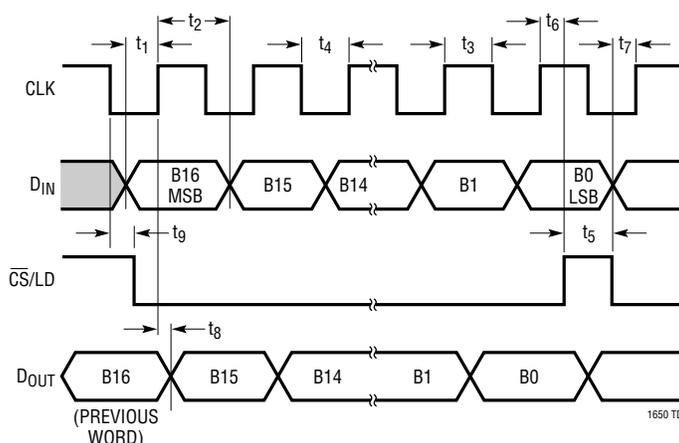
## PIN FUNCTIONS

**AV<sub>SS</sub> (Pin 14):** The Analog Negative Supply Input.  $-5.25V \leq AV_{SS} \leq -4.75V$ . Requires a bypass capacitor to ground.

**AV<sub>DD</sub> (Pin 15):** The Analog Positive Supply Input.  $4.75V \leq AV_{DD} \leq 5.25V$ . Requires a bypass capacitor to ground.

**UNI/BIP (Pin 16):** The Unipolar/Bipolar Selection Pin. For unipolar operation, tie this pin to V<sub>OUT</sub> and for bipolar operation, tie this pin the REFHI.

## TIMING DIAGRAM



## DEFINITIONS

### Resolution (n)

Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states ( $2^n$ ) that divide the full-scale range. The resolution does not imply linearity.

### Full-Scale Voltage (V<sub>FS</sub>)

This is the output of the DAC when all bits are set to 1. The output will swing from REFLO to REFHI in unipolar mode and from  $-REFHI$  to REFHI when in bipolar mode.

### Voltage Offset Error (V<sub>OS</sub>)

This is the voltage at the output when the DAC is loaded with all zeros.

### Least Significant Bit (LSB)

One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/2^n - 1 = (V_{FS} - V_{OS})/65535$$

### Integral Nonlinearity (INL)

Endpoint INL is the maximum deviation from a straight line passing through the endpoints of the DAC transfer curve. It is measured after adjusting out gain and offset error for the DAC.

### Differential Nonlinearity (DNL)

DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

$\Delta V_{OUT}$  = The measured voltage difference between two adjacent codes.

### Gain Error (GE)

Gain error is the difference between the full-scale output of a DAC from its ideal full-scale value after offset error has been adjusted for.

## OPERATION

### Serial Interface

The data on the  $D_{IN}$  input is loaded into the shift register on the rising edge of the clock. Data is loaded as one 16-bit word, MSB first. The DAC register loads the data from the shift register when  $\overline{CS/LD}$  is pulled high. The clock is disabled internally when  $\overline{CS/LD}$  is high. Note: CLK must be low before  $\overline{CS/LD}$  is pulled low to avoid an extra internal clock pulse.

The buffered output of the 16-bit shift register is available on the  $D_{OUT}$  pin which swings from DGND to  $DV_{DD}$ .

Multiple LTC1650s may be daisy-chained together by connecting the  $D_{OUT}$  pin to the  $D_{IN}$  pin of the next chip while the clock and  $\overline{CS/LD}$  signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the  $\overline{CS/LD}$  signal is pulled high to update all of them simultaneously.

When  $\overline{CLR}$  is pulled low or when the part powers up, the output connects through an internal pass gate to  $V_{RST}$  and will go to whatever voltage is on  $V_{RST}$ . When any of three supplies ( $DV_{DD}$ ,  $AV_{DD}$ ,  $IAV_{SS}$ ) goes below 2.5V, the  $\overline{RSTOUT}$  pin goes low and stays low as long as the supply is below 2.5V. The power-on reset is also activated when one of the supplies drops below 2.5V and the output is

then connected to  $V_{RST}$ . The output connects to  $V_{RST}$  when any of three conditions occur:  $\overline{CLR}$  goes low, the part powers up or one of the supplies drops below 2.5V. This condition exists as long as  $\overline{CS/LD}$  is low. As soon as  $\overline{CS/LD}$  goes high, the DAC register is loaded with the data in the shift register and the output will settle to its new value.

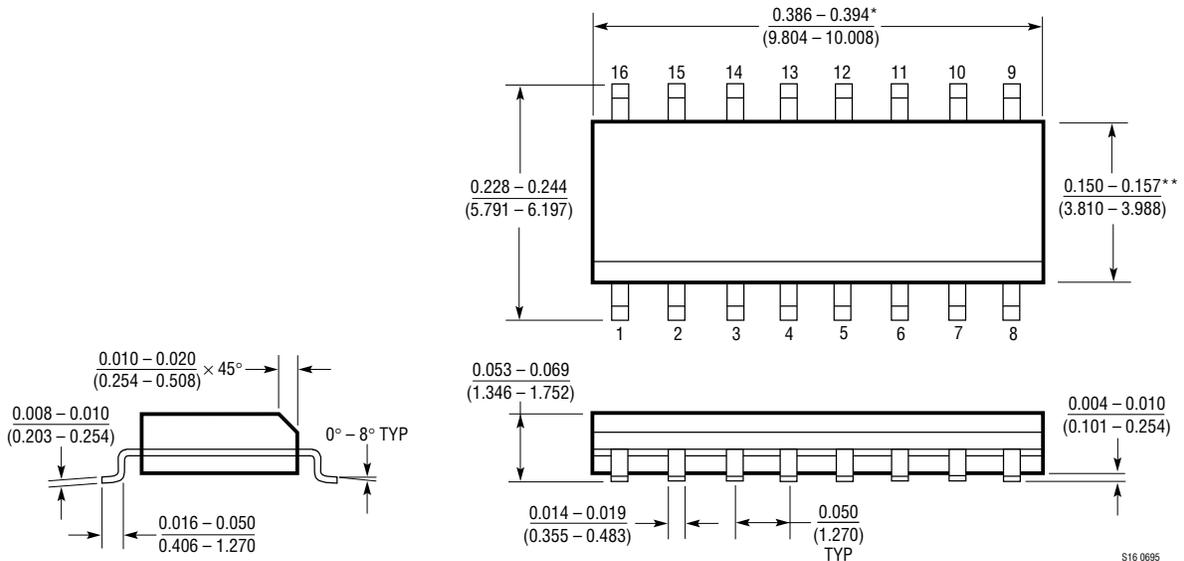
### Voltage Output

The LTC1650 rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range. The outputs swing to within a few millivolts of either supply rail when unloaded and have an equivalent output resistance of 50 $\Omega$  when driving a load to the rails. The buffer amplifier can drive 1000pF without going into oscillation. The LTC1650 has a deglitched voltage output. The midscale glitch is less than 2nV-s. The digital feedthrough is about 0.05nV-s.

The LTC1650 is capable of unipolar or bipolar output swing. When the UNI/BIP pin is connected to  $V_{OUT}$  the part is configured for unipolar operation and the output will swing from REFLO to REFHI. When connected to REFHI the part is configured in bipolar mode and the output will swing from ( $-REFHI - REFLO$ ) to ( $REFHI - REFLO$ ) and will be at  $-REFLO$  at midscale.

**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**S Package**  
**16-Lead Plastic Small Outline (Narrow 0.150)**  
 (LTC DWG # 05-08-1610)



\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

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**RELATED PARTS**

| PART NUMBER      | DESCRIPTION  | COMMENTS  |
|------------------|--|---|
| LTC1257          | Single 12-Bit $V_{OUT}$ DAC, Full Scale: 2.048V, $V_{CC}$ : 4.75V to 15.75V, Reference Can Be Overdriven Up to 12V, i.e., $FS_{MAX} = 12V$ | 5V to 15V Single Supply, Complete $V_{OUT}$ DAC in SO-8 Package   |
| LTC1446/LTC1446L | Dual 12-Bit $V_{OUT}$ DACs in SO-8 Package   | LTC1446: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V<br>LTC1446L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V |
| LTC1448          | Dual 12-Bit $V_{OUT}$ DAC, $V_{CC}$ : 2.7V to 5.5V   | Output Swings from GND to REF. REF Input Can Be Tied to $V_{CC}$  |
| LTC1450/LTC1450L | Single 12-Bit $V_{OUT}$ DACs with Parallel Interface   | LTC1450: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V<br>LTC1450L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V |
| LTC1451          | Single Rail-to-Rail 12-Bit DAC, Full Scale: 4.095V, $V_{CC}$ : 4.5V to 5.5V, Internal 2.048V Reference Brought Out to Pin                  | 5V, Low Power Complete $V_{OUT}$ DAC in SO-8 Package  |
| LTC1452          | Single Rail-to-Rail 12-Bit $V_{OUT}$ Multiplying DAC, $V_{CC}$ : 2.7V to 5.5V  | Low Power, Multiplying $V_{OUT}$ DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package                                 |
| LTC1453          | Single Rail-to-Rail 12-Bit $V_{OUT}$ DAC, Full Scale: 2.5V, $V_{CC}$ : 2.7V to 5.5V  | 3V, Low Power, Complete $V_{OUT}$ DAC in SO-8 Package   |
| LTC1454/LTC1454L | Dual 12-Bit $V_{OUT}$ DACs in SO-16 Package with Added Functionality   | LTC1454: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V<br>LTC1454L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V |
| LTC1456          | Single Rail-to-Rail Output 12-Bit DAC with Clear Pin, Full Scale: 4.095V, $V_{CC}$ : 4.5V to 5.5V  | Low Power, Complete $V_{OUT}$ DAC in SO-8 Package with Clear Pin  |
| LTC1458/LTC1458L | Quad 12 Bit Rail-to-Rail Output DACs with Added Functionality  | LTC1458: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V<br>LTC1458L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V |
| LTC1595          | 16-Bit Multiplying $I_{OUT}$ DAC in SO-8   | $\pm 1LSB$ Max INL/DNL, Low Glitch, DAC8043<br>16-Bit Upgrade   |
| LTC1596          | 16-Bit Multiplying $I_{OUT}$ DAC   | $\pm 1LSB$ Max INL/DNL, Low Glitch, AD7543/DAC8143<br>16-Bit Upgrade  |
| LTC1659          | Single Rail-to-Rail 12-Bit $V_{OUT}$ DAC in MSOP-8 Package, $V_{CC}$ : 2.7V TO 5.5V  | Low Power Multiplying $V_{OUT}$ DAC in MSOP-8 Package. Output Swings from GND to REF. REF Input Can be Tied to $V_{CC}$ |
| LTC7541A         | Parallel I/O Multiplying 12-Bit DAC  | 12-Bit Wide Input   |
| LTC7543/LTC8143  | Serial I/O Multiplying $I_{OUT}$ 12-Bit DACs   | Clear Pin, Serial Data Output (LTC8143)   |
| LTC8043          | Serial I/O Multiplying $I_{OUT}$ 12-Bit DAC  | 8-Pin SO and PDIP   |