

**W81282F**  
**USB Keyboard Controller**  
**with**  
**4 Ports Hub**

## W81282F Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	n.a.	08/27/99	0.50	n.a.	First published.
2					
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# W81282F

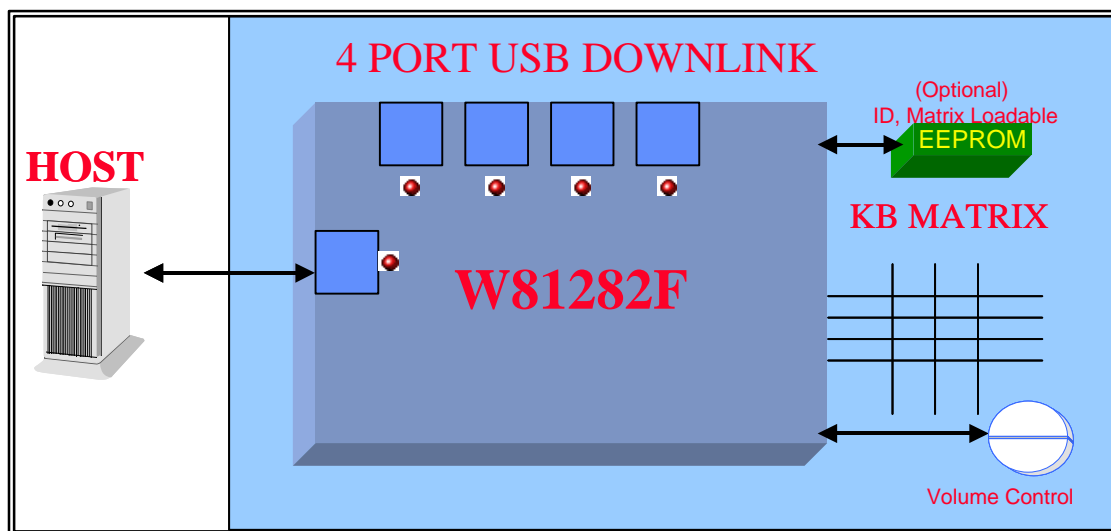


## USB HUB CONTROLLER

### 1. GENERAL DESCRIPTION

The W81282F is a highly integrated USB keyboard with 4 port hub controller chip. The W81282F has a built-in 21X8 default keyboard matrix, so that it can be directly connected to keyboard with multi-media function matrix. The keyboard matrix, vendor ID, and device ID can be easily customized from an optional EEPROM or modify firmware to meet any customers' requirement. The 4 USB down-stream port can be used to connect various USB peripheral devices, such as printer, modem, speaker, camera, mice, and joystick, to system without any external glue logics. The W81282F use 12MHz clock input with internal PLL to eliminate EMI effect. The W81282F also built-in ESD/EFT protection circuit so it can pass ESD/EFT test without any external glue logics.

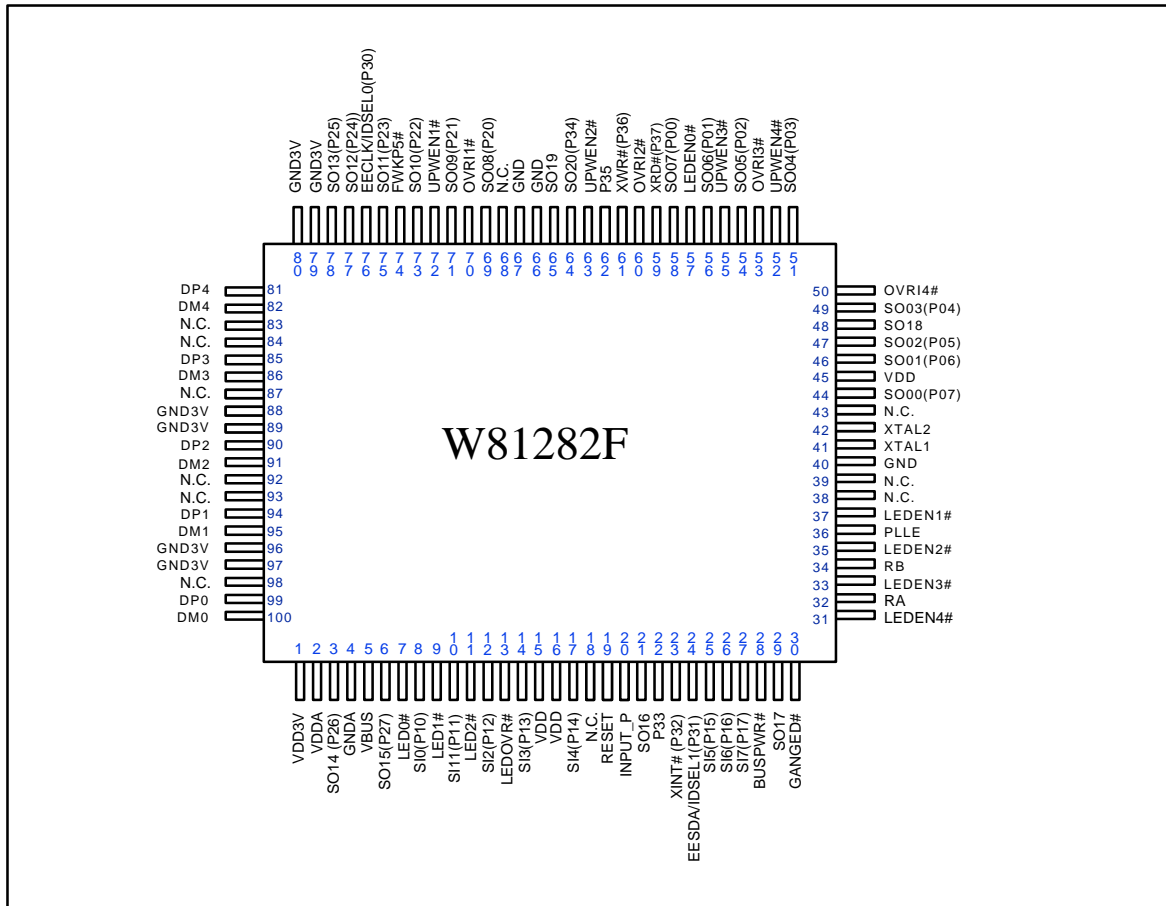
### 2. APPLICATION BLOCK DIAGRAM



### **3. FEATURES**

- Full compliance with USB spec Rev 1.1 and HID Class Definition Rev 1.0
- Embedded microprocessor--8052 ( 6K ROM + 256 Byte RAM)
- Support auto-detected two power source mode between bus power mode and self power mode.
- 12-Mhz crystal/oscillator input to lower EMI
- Support Suspend and Resume operation
- Support ACPI features
- Four downstream ports with per port over-current protection
- Single 5V supplied with embedded 5V-3.3V regulator
- Provides the external pull-up resistor control for the up-stream connection.
- Per-port/Global power control optional
- Built-in ESD/EFT protection circuit
- Support 21 X 8 keyboard matrix
- Support consumer control function for multi-media
- Support optional EEPROM for vendor ID, device ID, and KB matrix down load
- Support encoder input for audio volume control
- Provide the external pull-up resistor control for the up-stream connect
- 100-pin PQFP
- 5V CMOS device

## 4. PIN CONFIGURATION



**5. PIN DESCRIPTION**

Pin Number	Pin Name	I/O Type	Pin Function	Pull Up/Down
1	VDD3V	Power1	3.3V Regulator Output. Supplying voltage for all transceivers	-
2	VDDA	Power1	Analog power.	-
3	SO14 (P26)	IOUD2	Port 2.6 and function of Scan Out line 14.	U
4	GNDA	Power0	Analog ground.	-
5	VBUS	IUD2T	Input of upstream power status. On self-power mode, connection should be controlled by VBUS status.	-
6	SO15 (P27)	IOUD2	Port 2.7 and function of Scan Out line 15.	U
7	LED0#	IOU2P	Keyboard NumLock LED driver. To drive LED directly.	O
8	SI0 (P10)	IOUD2	Port 1.0 and function of Scan In line 0.	U
9	LED1#	IOU2P	Keyboard CapLock LED driver. To drive LED directly.	O
10	SI1 (P11)	IOUD2	Port 1.1 and function of Scan In line 1.	U
11	LED2#	IOU2P	Keyboard ScrollLock LED driver. To drive LED directly	O
12	SI2 (P12)	IOUD2	Port 1.2 and function of Scan In line 2.	U
13	LEDOVR#	IOU2P	Flag of any downstream port1 over-current. To drive LED directly	O
14	SI3 (P13)	IOUD2	Port 1.3 and function of Scan In line 3.	U
15,16	VDD	Power1	Digital supply voltage.	-
17	SI4 (P14)	IOUD2	Port 1.4 and function of Scan In line 4.	U
18	N.C.	IOUD2	No connection. This pin should be floated.	U
19	RESET	IUD2T	Master reset input. Active high.	-
20	INPUT_P	IOUD2	A programmable port and reverse for input application.	U
21	SO16	O2	This pin is function of Scan Out line 16.	-
22	P33	IOUD2	Port 3.3 and reverse for input or output application.	U
23	XINT# (P32)	IOUD2	Port 3.2. This pin is dedicated for internal use.	U
24	EESDA/IDSEL1 (P31)	IOUD2	Port 3.1 and function of serial data line interfacing with external EEPROM. If no serial EEPROM present, this pin is used to scan ID selection and named IDSEL1	U
25	SI5 (P15)	IOUD2	Port 1.5 and function of Scan In line 5.	U
26	SI6 (P16)	IOUD2	Port 1.6 and function of Scan In line 6.	U
27	SI7 (P17)	IOUD2	Port 1.7 and function of Scan In line 7.	U

28	<b>BUSPWR#</b>	<b>IUD2</b>	Buspower/Selfpower control setting. This pin should be floated or tied to VDD.	<b>D</b>
29	<b>SO17</b>	<b>IOU2P</b>	This pin is function of Scan Out line 17.	<b>O</b>
30	<b>GANGED#</b>	<b>IUD2</b>	Ganged/Individual downstream power switch control setting. Default is Individual mode.	<b>U</b>
31	<b>LEDEN4#</b>	<b>IOU2P</b>	Downstream port4 LED. Active low when port4 enable.	<b>O</b>
32	<b>RA</b>	<b>IUD2</b>	<b>This pin is a Rotation A input for consumer HID application.</b>	<b>U</b>
33	<b>LEDEN3#</b>	<b>IOU2P</b>	Downstream port3 LED. Active low when port3 enable.	<b>O</b>
34	<b>RB</b>	<b>IUD2</b>	<b>This pin is a Rotation B input for consumer HID application.</b>	<b>U</b>
35	<b>LEDEN2#</b>	<b>IOU2P</b>	Downstream port2 LED. Active low when port2 enable.	<b>O</b>
<b>36</b>	<b>PLLE</b>	<b>IUD2</b>	PLL clock generator enable/disable control. It should be tied to VDD. (PLLE=1, clock=12MHz ; PLLE=0, clock=48MHz)	<b>U</b>
37	<b>LEDEN1#</b>	<b>IOU2P</b>	Downstream port1 LED. Active low when port1 enable.	<b>O</b>
<b>38</b>	<b>N.C.</b>	<b>IUD2</b>	No connection. This pin should be floated.	<b>U</b>
<b>39</b>	<b>N.C.</b>	<b>IUD2</b>	No connection. This pin should be floated.	<b>U</b>
40	<b>GND</b>	<b>Power0</b>	Digital ground	-
41	<b>XTAL1</b>	<b>OSCM</b>	Clock In. (12MHz when PLLE=1, 48MHz when PLLE=0)	-
42	<b>XTAL2</b>	<b>OSCM</b>	Clock Out.	-
<b>43</b>	<b>N.C.</b>	<b>IUD2</b>	No connection. This pin should be floated.	<b>D</b>
<b>44</b>	<b>SO00 (P07)</b>	<b>IOUD2</b>	Port 0.7 and function of Scan Out line 0.	<b>U</b>
45	<b>VDD</b>	<b>Power1</b>	Digital supply voltage.	-
<b>46</b>	<b>SO01 (P06)</b>	<b>IOUD2</b>	Port 0.6 and function of Scan Out line 1.	<b>U</b>
<b>47</b>	<b>SO02 (P05)</b>	<b>IOUD2</b>	Port 0.5 and function of Scan Out line 2.	<b>U</b>
48	<b>SO18</b>	<b>O2</b>	<b>This pin is function of Scan Out line 18.</b>	-
<b>49</b>	<b>SO03 (P04)</b>	<b>IOUD2</b>	Port 0.4 and function of Scan Out line 3.	<b>U</b>
50	<b>OVRI4#</b>	<b>IUD2T</b>	Downstream port4 over-current status input. Active low.	-
<b>51</b>	<b>SO04 (P03)</b>	<b>IOUD2</b>	Port 0.3 and function of Scan Out line 4.	<b>U</b>
52	<b>UPWEN4#</b>	<b>O2</b>	Downstream port4 power control. Active low.	-
53	<b>OVRI3#</b>	<b>IUD2T</b>	Downstream port3 over-current status input. Active low.	-
<b>54</b>	<b>SO05 (P02)</b>	<b>IOUD2</b>	Port 0.2 and function of Scan Out line 5.	<b>U</b>
55	<b>UPWEN3#</b>	<b>O2</b>	Downstream port3 power control. Active low.	-
<b>56</b>	<b>SO06 (P01)</b>	<b>IOUD2</b>	Port 0.1 and function of Scan Out line 6.	<b>U</b>
57	<b>LEDEN0#</b>	<b>IOU2P</b>	Up_stream port LED. Active low when up_stream port enable.	<b>O</b>
<b>58</b>	<b>SO07 (P00)</b>	<b>IOUD2</b>	Port 0.0 and function of Scan Out line 7.	<b>U</b>



59	<b>XRD# (P37)</b>	<b>IOUD2</b>	Port 3.7. <b>This pin is dedicated for internal use.</b>	<b>U</b>
60	<b>OVRI2#</b>	<b>IUD2T</b>	Downstream port2 over-current status input. Active low.	-
61	<b>XWR# (P36)</b>	<b>IOUD2</b>	Port 3.6. <b>This pin is dedicated for internal use.</b>	<b>U</b>
62	<b>P35</b>	<b>IOUD2</b>	Port 3.5 and reverse for input or output application.	<b>U</b>
63	<b>UPWEN2#</b>	<b>O2</b>	Downstream port2 power control. Active low.	-
64	<b>SO20 (P34)</b>	<b>IOUD2</b>	Port 3.4 and function of <b>Scan Out line 20.</b>	<b>U</b>
65	<b>SO19</b>	<b>O2</b>	This pin is function of Scan Out line 19.	-
66,67	<b>GND</b>	<b>Power0</b>	Digital ground.	-
68	<b>N.C.</b>	<b>IOUD2</b>	No connection. This pin should be floated.	<b>U</b>
69	<b>SO08 (P20)</b>	<b>IOUD2</b>	Port 2.0 and function of Scan Out line 8.	<b>U</b>
70	<b>OVRI1#</b>	<b>IUD2T</b>	Downstream port1 over-current status input. Active low.	-
71	<b>SO09 (P21)</b>	<b>IOUD2</b>	Port 2.1 and function of Scan Out line 9.	<b>U</b>
72	<b>UPWEN1#</b>	<b>O2</b>	Downstream port1 power control. Active low.	-
73	<b>SO10 (P22)</b>	<b>IOUD2</b>	Port 2.2 and function of Scan Out line 10.	<b>U</b>
74	<b>FWKP5#</b>	<b>IUD2</b>	Embedded function wake-up input. <b>Can be used for Wake-up hot key.</b>	<b>D</b>
75	<b>SO11 (P23)</b>	<b>IOUD2</b>	Port 2.3 and function of Scan Out line 11.	<b>U</b>
76	<b>EECLK&gt;IDSEL0 (P30)</b>	<b>IOUD2</b>	<b>This pin is Port 3.0 and function of serial clock line interfacing with external EEPROM. If no serial EEPROM present, this pin is used to scan ID selection and named IDSEL0.</b>	<b>U</b>
77	<b>SO12 (P24)</b>	<b>IOUD2</b>	Port 2.4 and function of Scan Out line 12.	<b>U</b>
78	<b>SO13 (P25)</b>	<b>IOUD2</b>	Port 2.5 and function of Scan Out line 13.	<b>U</b>
79,80	<b>GND3V</b>	<b>Power0</b>	Ground of port3 and port4 transceivers.	-
81	<b>DP4</b>	<b>AIO</b>	USB D+ for downstream port4.	-
82	<b>DM4</b>	<b>AIO</b>	USB D- for downstream port4.	-
83,84	<b>N.C.</b>	-	No connection.	
85	<b>DP3</b>	<b>AIO</b>	USB D+ for downstream port3.	-
86	<b>DM3</b>	<b>AIO</b>	USB D- for downstream port3.	-
87	<b>N.C.</b>	-	No connection.	
88,89	<b>GND3V</b>	<b>Power0</b>	Ground of port1 and port2 transceivers.	-
90	<b>DP2</b>	<b>AIO</b>	USB D+ for downstream port2.	-
91	<b>DM2</b>	<b>AIO</b>	USB D- for downstream port2.	-

92,93	<b>N.C.</b>	-	No connection.	
94	<b>DP1</b>	<b>AIO</b>	USB D+ for downstream port1.	-
95	<b>DM1</b>	<b>AIO</b>	USB D- for downstream port1.	-
96,97	<b>GND3V</b>	<b>Power0</b>	Ground of port0 transceivers.	-
98	<b>N.C.</b>	-	No connection.	
99	<b>DP0</b>	<b>AIO</b>	USB D+ for upstream port0.	-
100	<b>DM0</b>	<b>AIO</b>	USB D- for upstream port0.	-

**6. ABSOLUTE MAXIMUM RATINGS**

PARAMETER	LIMIT
Supply Voltage (Vcc to Vss)	5.5V
Analog Input Voltage	Vss-0.5V to Vcc+0.5V
Digital Input Voltage	Vss-0.5V to Vcc+0.5V
Power Dissipation	TBD
Ambient Operating Temperature	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	250°C

**7. ELECTRICAL CHARACTERISTICS**

 Operating conditions:  $V_{CC} = 5V \pm 5\%$ ,  $T_a = 0^\circ$  to  $70^\circ\text{C}$ 

PARAMETER	Symbol	Conditions	Min	Max	Unit
VCC Supply Current	I <sub>cc</sub>			TBD	mA
Logic Output High	VOH	I <sub>o</sub> ≥ 24ma	2.5	V <sub>CC</sub>	V
Logic Output Low	VOL	I <sub>o</sub> ≥ 6ma		0.4	V
Logic Input Leakage Current		T <sub>a</sub> = 70°C		10	uA
<b>USB CHARACTERISTICS</b>		Note 8			
Leakage Current:					
Hi-Z State Output Leakage	ILO	V < V <sub>IN</sub> < 3.3 V	-10	+10	uA
Input Levels:					
Differential Input Sensitivity	VDI	(D+) - (D-)	0.2		V
Single Ended Signal "0"	VSE0		0.8	2.0	V
Differential Common Mode Range	V <sub>CM</sub>	Includes VDI range	0.8	2.5	
Output Levels:					
Driver Output Low	VOLU	R <sub>L</sub> of 1.5 kΩ to 3.6 V		0.3	V
Driver Output High	VOHU	R <sub>L</sub> of 15 kΩ to GND	2.8	3.6	V
Output Signal Crossover Voltage	V <sub>CRS</sub>		1.3	2.0	V
Capacitance:					
Transceiver Capacitance	CIN	Pin to GND		20	pF
Full Speed Timings:					
Output Rise/Fall Times	t <sub>R</sub> / t <sub>F</sub>	Note 1, 4 (C <sub>L</sub> = 50 pF)	4	20	ns
Source Differential Driver Jitter to Next Transition	t <sub>DJ1</sub>	Note 2, 3	-3.5	3.5	ns
/ to Paired Transition	/t <sub>DJ2</sub>		/-4	/4	ns
Differential to EOP transition Skew	t <sub>DEOP</sub>	Note 3	-2	5	ns
Hub Differential Data Delay (without cable)	t <sub>HDD2</sub>	Note 2,3,5		44	ns
Hub Differential Driver Jitter to Next Transition	t <sub>HDJ1</sub>	Note 2,3,5	-3	3	ns
/ to Paired Transition (including cable)	/ t		/-1	/1	
Data bit width distortion after SOP	t <sub>SOP</sub>	Note 3,5	-5	5	ns
Hub SE0 Delay Relative to t <sub>HDD</sub>	t <sub>EOPD</sub>	Note 3,5	0	15	ns
Hub EOP Output Width Skew	t <sub>HESK</sub>	Note 3,5	-15	15	ns
Low Speed Timings:					
Output Rise/Fall Times	t <sub>R</sub> / t <sub>F</sub>	Note 1, 4 (C <sub>L</sub> = 50 pF)	75	300	ns

## 7. ELECTRICAL CHARACTERISTICS, continued

PARAMETER	Symbol	Conditions	Min	Max	Unit
Source Differential Driver Jitter to Next Transition / to Paired Transition	t DJ1 /tDJ2	Note 2, 3	-25 /-14	25 /14	ns ns
Differential to EOP transition Skew	t <sub>DEOP</sub>	Note 3	-40	100	ns
Hub Differential Data Delay(without cable)	t <sub>HDD2</sub>	Note 2,3,5		300	ns
Hub Differential Driver Jitter to Next Transition / to Paired Transition (including cable)	t <sub>HDJ1</sub> / t <sub>HDJ2</sub>	Note 2,3,5	-45 / -45	45 /45	ns ns
Data bit width distortion after SOP	t <sub>SOP</sub>	Note 3,5	-60	60	ns
Hub SE0 Delay Relative to t <sub>HDD</sub>	t <sub>EOPD</sub>	Note 3,5	0	200	ns
Hub EOP Output Width Skew	t <sub>HESK</sub>	Note 3,5	-300	300	ns

Note 1: Measured from 10% to 90% of the data signal.

Note 2: Timing difference between the differential signals.

Note 3: Measured at crossover point of differential data signals.

Note 4: The rising and falling edges should be smoothly transiting(monotonic)

Note 5: Full Speed timing have a 1.5 kΩ pull-up to 2.8 V on the D+ (DP) data line.

Note 6: Low Speed timing have a 1.5 kΩ pull-up to 2.8 V on the D- (DM) data line.

Note 7: The maximum load specification is the maximum effective capacitive load allowed that meets the target hub VBUS droop of 330 mV.

Note 8: All other USB Electrical Characteristics refer to USB spec Rev 1.1 7.3.2 and 7.3.3.

## 8. TYPICAL APPLICATION



## 9. HOW TO READ THE TOP MARKING

Example: The top marking of W81282F-05



1st line: Winbond logo

2nd line: the type number: W81282F-05

3rd line: the tracking code: 732 A C 2 7242968

732: packages made in '97, week 19 \_\_\_\_\_

A: assembly house ID; A means ASE, S means SPIL ... etc

C: IC revision; B means version B, C means version C

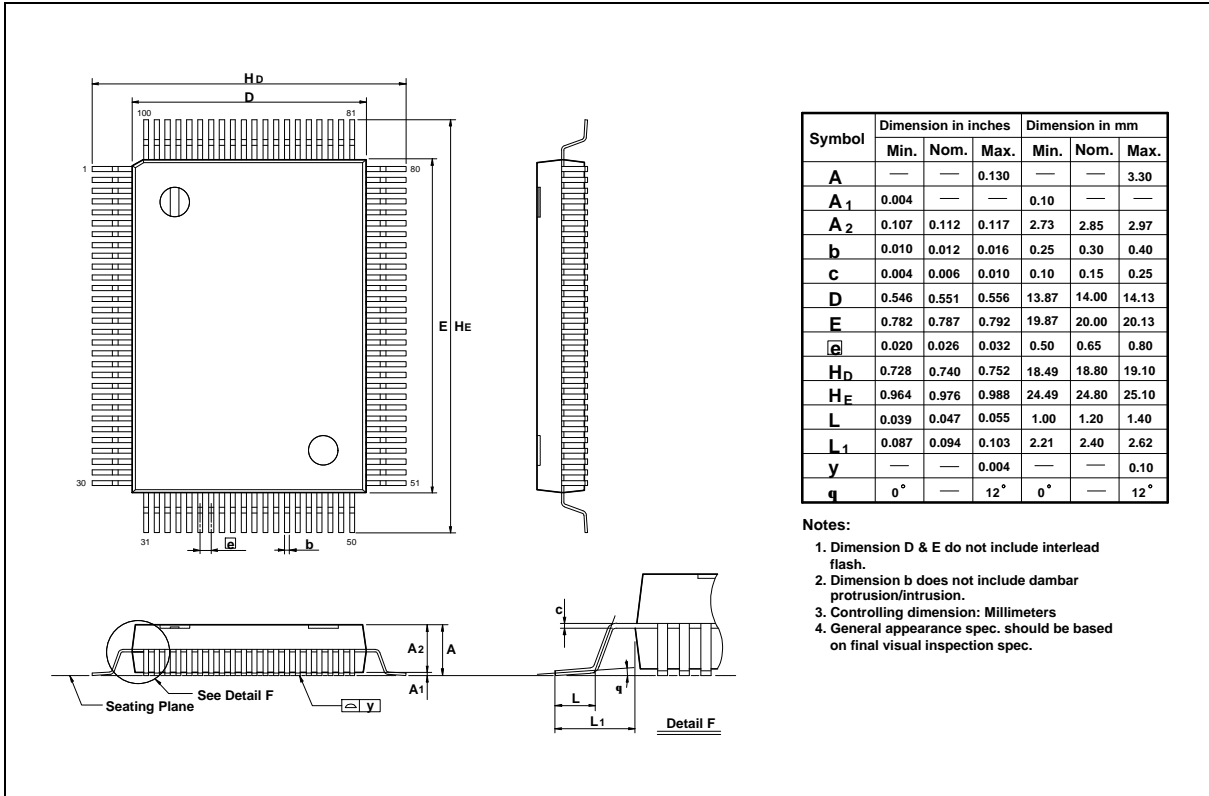
2: wafers manufactured in Winbond FAB 2

7242968: wafer production series lot number



### 10. PACKAGE DIMENSIONS

(100-pin QFP)





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