

45MHz, 45V/ μ s, Dual/Quad Rail-to-Rail Input and Output Precision Op Amps

February 1998

FEATURES

- **Gain-Bandwidth Product: 45MHz**
- **Slew Rate: 45V/ μ s**
- **Low Supply Current per Amplifier: 4.3mA**
- Input Common Mode Range Includes Both Rails
- Output Swings Rail-to-Rail
- Input Offset Voltage, Rail-to-Rail: 1350 μ V Max
- Input Offset Current: 440nA Max
- Input Bias Current: 2.2 μ A Max
- Open-Loop Gain: 800V/mV Min
- Low Input Noise Voltage: 12nV/ $\sqrt{\text{Hz}}$ Typ
- Wide Supply Range: 2.7V to ± 15 V
- Large Output Drive Current: 70mA
- Dual in 8-Pin PDIP and SO Packages

APPLICATIONS

- Active Filters
- Rail-to-Rail Buffer Amplifiers
- Driving A/D Converters
- Low Voltage Signal Processing
- Battery-Powered Systems

DESCRIPTION

The LT[®]1632/LT1633 are dual/quad, rail-to-rail input and output op amps with a 45MHz gain-bandwidth product and a 45V/ μ s slew rate.

The LT1632/LT1633 have excellent DC precision over the full range of operation. Input offset voltage is typically less than 400 μ V and the minimum open-loop gain of 0.8 million into a 10k load virtually eliminates all gain error. Common mode rejection is typically 83dB over the full rail-to-rail input range of 5V supply for excellent noninverting performance.

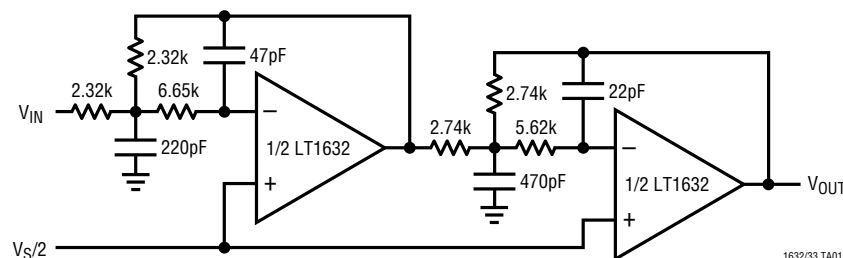
The LT1632/LT1633 maintain their performance for supplies from 2.7V to 36V and are specified at 3V, 5V and ± 15 V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output. The output delivers load currents in excess of 50mA.

The LT1632 is available in 8-pin PDIP and SO packages with the standard dual op amp pinout. The LT1633 features the standard quad op amp configuration and is available in a 14-pin plastic SO package. These devices can be used as plug-in replacements for many standard op amps to improve input/output range and performance.

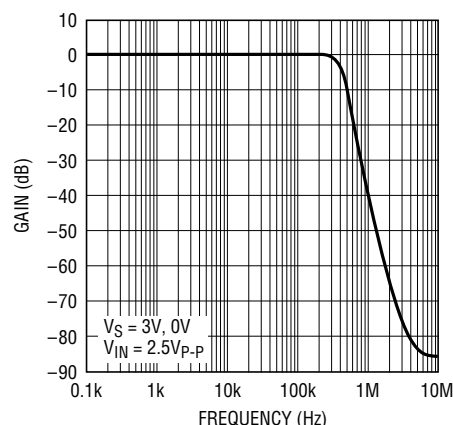
LT, LTC and LT are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

Single Supply, 400kHz, 4th Order Butterworth Filter



Frequency Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
 Input Current $\pm 10\text{mA}$
 Output Short-Circuit Duration (Note 1) Continuous
 Operating Temperature Range (Note 3) ... -40°C to 85°C

Specified Temperature Range 0°C to 70°C
 Junction Temperature 150°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 130^\circ\text{C/W}$ (N8) $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 190^\circ\text{C/W}$ (S8)	ORDER PART NUMBER LT1632CN8 LT1632CS8 S8 PART MARKING 1632	TOP VIEW S PACKAGE 14-LEAD PLASTIC SO $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 150^\circ\text{C/W}$	ORDER PART NUMBER LT1633CS
---	--	--	--

Consult factory for Military and Industrial grade parts.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, 0V ; $V_S = 3\text{V}$, 0V ; $V_{CM} = V_{OUT} = \text{half supply}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$		400	1350	μV
		$V_{CM} = V^-$		400	1350	μV
ΔV_{OS}	Input Offset Shift	$V_{CM} = V^-$ to V^+		350	1500	μV
		Input Offset Voltage Match (Channel-to-Channel) $V_{CM} = V^-$, V^+ (Note 4)		500	2300	μV
I_B	Input Bias Current	$V_{CM} = V^+$	0	1.15	2.2	μA
		$V_{CM} = V^-$	-2.2	-1.15	0	μA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+		2.3	4.4	μA
		Input Bias Current Match (Channel-to-Channel) $V_{CM} = V^+$ (Note 4) $V_{CM} = V^-$ (Note 4)		50	880	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$		40	440	nA
		$V_{CM} = V^-$		40	440	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+		80	880	nA
		Input Noise Voltage		400		nV _{p-p}
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		12		nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		1.6		pA/ $\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance			5		pF
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5\text{V}$, $V_O = 300\text{mV}$ to 4.7V , $R_L = 10\text{k}$	450	2000		V/mV
		$V_S = 3\text{V}$, $V_O = 300\text{mV}$ to 2.7V , $R_L = 10\text{k}$	350	1500		V/mV

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, 0V ; $V_S = 3\text{V}$, 0V ; $V_{CM} = V_{OUT} = \text{half supply}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}$, $V_{CM} = V^- \text{ to } V^+$	70	83		dB
		$V_S = 3\text{V}$, $V_{CM} = V^- \text{ to } V^+$	66	81		dB
	CMRR Match (Channel-to-Channel) (Note 4)	$V_S = 5\text{V}$, $V_{CM} = V^- \text{ to } V^+$ $V_S = 3\text{V}$, $V_{CM} = V^- \text{ to } V^+$	65 61	85 82		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.7\text{V to } 12\text{V}$, $V_{CM} = V_O = 0.5\text{V}$	82	100		dB
	PSRR Match (Channel-to-Channel) (Note 4)	$V_S = 2.7\text{V to } 12\text{V}$, $V_{CM} = V_O = 0.5\text{V}$	79	101		dB
	Minimum Supply Voltage (Note 8)	$V_{CM} = V_O = 0.5\text{V}$		2.6	2.7	V
V_{OL}	Output Voltage Swing Low (Note 5)	No Load		15	30	mV
		$I_{SINK} = 0.5\text{mA}$		32	60	mV
		$I_{SINK} = 25\text{mA}$, $V_S = 5\text{V}$		600	1200	mV
		$I_{SINK} = 20\text{mA}$, $V_S = 3\text{V}$		500	1000	mV
V_{OH}	Output Voltage Swing High (Note 5)	No Load		16	40	mV
		$I_{SOURCE} = 0.5\text{mA}$		42	80	mV
		$I_{SOURCE} = 20\text{mA}$, $V_S = 5\text{V}$		910	1800	mV
		$I_{SOURCE} = 15\text{mA}$, $V_S = 3\text{V}$		680	1400	mV
I_{SC}	Short-Circuit Current	$V_S = 5\text{V}$	± 20	± 40		mA
		$V_S = 3\text{V}$	± 15	± 30		mA
I_S	Supply Current per Amplifier			4.3	5.2	mA
GBW	Gain-Bandwidth Product (Note 6)	$f = 100\text{kHz}$	22	45		MHz
SR	Slew Rate (Note 7)	$V_S = 5\text{V}$, $A_V = -1$, $R_L = \text{Open}$, $V_O = 4\text{V}$	13	27		V/ μs
		$V_S = 3\text{V}$, $A_V = -1$, $R_L = \text{Open}$	11	22		V/ μs

$0^\circ\text{C} < T_A < 70^\circ\text{C}$, $V_S = 5\text{V}$, 0V ; $V_S = 3\text{V}$, 0V ; $V_{CM} = V_{OUT} = \text{half supply}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+ - 0.1\text{V}$	●	600	2000	μV
		$V_{CM} = V^- + 0.2\text{V}$	●	600	2000	μV
$V_{OS\ TC}$	Input Offset Voltage Drift (Note 2)	$V_{CM} = V^+ - 0.1\text{V}$	●	6		$\mu\text{V}/^\circ\text{C}$
			●	6		$\mu\text{V}/^\circ\text{C}$
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^- + 0.2\text{V to } V^+ - 0.1\text{V}$	●	400	2300	μV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.2\text{V}$, $V^+ - 0.1\text{V}$ (Note 4)	●	700	3750	μV
I_B	Input Bias Current	$V_{CM} = V^+ - 0.1\text{V}$	●	0	1.3	μA
		$V_{CM} = V^- + 0.2\text{V}$	●	-2.6	-1.3	μA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.2\text{V to } V^+ - 0.1\text{V}$	●	2.6	5.2	μA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+ - 0.1\text{V}$ (Note 4)	●	50	1040	nA
		$V_{CM} = V^- + 0.2\text{V}$ (Note 4)	●	50	1040	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+ - 0.1\text{V}$	●	40	520	nA
		$V_{CM} = V^- + 0.2\text{V}$	●	40	520	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.2\text{V to } V^+ - 0.1\text{V}$	●	80	1040	nA
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5\text{V}$, $V_O = 300\text{mV to } 4.7\text{V}$, $R_L = 10\text{k}$	●	300	1100	V/mV
		$V_S = 3\text{V}$, $V_O = 300\text{mV to } 2.7\text{V}$, $R_L = 10\text{k}$	●	200	1000	V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}$, $V_{CM} = V^- + 0.2\text{V to } V^+ - 0.1\text{V}$	●	67	81	dB
		$V_S = 3\text{V}$, $V_{CM} = V^- + 0.2\text{V to } V^+ - 0.1\text{V}$	●	61	77	dB
	CMRR Match (Channel-to-Channel) (Note 4)	$V_S = 5\text{V}$, $V_{CM} = V^- + 0.2\text{V to } V^+ - 0.1\text{V}$ $V_S = 3\text{V}$, $V_{CM} = V^- + 0.2\text{V to } V^+ - 0.1\text{V}$	● ●	62 57	78 73	dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V to } 12\text{V}$, $V_{CM} = V_O = 0.5\text{V}$	●	81	94	dB
	PSRR Match (Channel-to-Channel) (Note 4)	$V_S = 3\text{V to } 12\text{V}$, $V_{CM} = V_O = 0.5\text{V}$	●	77	95	dB

ELECTRICAL CHARACTERISTICS

0°C < T_A < 70°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Minimum Supply Voltage (Note 8)	V _{CM} = V _O = 0.5V		2.6	2.7	V
V _{OL}	Output Voltage Swing Low (Note 5)	No Load		18	40	mV
		I _{SINK} = 0.5mA		37	80	mV
		I _{SINK} = 25mA, V _S = 5V		700	1400	mV
		I _{SINK} = 20mA, V _S = 3V		560	1200	mV
V _{OH}	Output Voltage Swing High (Note 5)	No Load		16	40	mV
		I _{SOURCE} = 0.5mA		50	100	mV
		I _{SOURCE} = 15mA, V _S = 5V		820	1600	mV
		I _{SOURCE} = 10mA, V _S = 3V		550	1100	mV
I _{SC}	Short-Circuit Current	V _S = 5V	±18	±37		mA
		V _S = 3V	±13	±26		mA
I _S	Supply Current per Amplifier			4.9	6.0	mA
GBW	Gain-Bandwidth Product (Note 6)	f = 100kHz	20	41		MHz
SR	Slew Rate (Note 7)	V _S = 5V, A _V = -1, R _L = Open, V _O = 4V	13	26		V/μs
		V _S = 3V, A _V = -1, R _L = Open	10	21		V/μs

-40°C < T_A < 85°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	V _{CM} = V ⁺ - 0.1V		700	2400	μV
		V _{CM} = V ⁻ + 0.2V		700	2400	μV
V _{OS} TC	Input Offset Voltage Drift (Note 2)	V _{CM} = V ⁺ - 0.1V		6		μV/°C
				6		μV/°C
ΔV _{OS}	Input Offset Voltage Shift	V _{CM} = V ⁻ + 0.2V to V ⁺ - 0.1V		475	2500	μV
	Input Offset Voltage Match (Channel-to-Channel)	V _{CM} = V ⁻ + 0.2V, V ⁺ (Note 4)		750	4000	μV
I _B	Input Bias Current	V _{CM} = V ⁺ - 0.1V	0	1.46	3.0	μA
		V _{CM} = V ⁻ + 0.2V	-3.0	-1.46	0	μA
ΔI _B	Input Bias Current Shift	V _{CM} = V ⁻ + 0.2V to V ⁺ - 0.1V		2.92	6.0	μA
	Input Bias Current Match (Channel-to-Channel)	V _{CM} = V ⁺ - 0.1V (Note 4)		70	1160	nA
		V _{CM} = V ⁻ + 0.2V (Note 4)		70	1160	nA
I _{OS}	Input Offset Current	V _{CM} = V ⁺ - 0.1V		75	580	nA
		V _{CM} = V ⁻ + 0.2V		75	580	nA
ΔI _{OS}	Input Offset Current Shift	V _{CM} = V ⁻ + 0.2V to V ⁺ - 0.1V		50	1160	nA
A _{VOL}	Large-Signal Voltage Gain	V _S = 5V, V _O = 300mV to 4.7V, R _L = 10k	250	1000		V/mV
		V _S = 3V, V _O = 300mV to 2.7V, R _L = 10k	200	800		V/mV
CMRR	Common Mode Rejection Ratio	V _S = 5V, V _{CM} = V ⁻ + 0.2V to V ⁺ - 0.1V	65	80		dB
		V _S = 3V, V _{CM} = V ⁻ + 0.2V to V ⁺ - 0.1V	60	75		dB
	CMRR Match (Channel-to-Channel) (Note 4)	V _S = 5V, V _{CM} = V ⁻ + 0.2V to V ⁺ - 0.1V	62	78		dB
		V _S = 3V, V _{CM} = V ⁻ + 0.2V to V ⁺ - 0.1V	57	73		dB
PSRR	Power Supply Rejection Ratio	V _S = 3V to 12V, V _{CM} = V _O = 0.5V	79	95		dB
		V _S = 3V to 12V, V _{CM} = V _O = 0.5V	75	95		dB
	Minimum Supply Voltage (Note 8)	V _{CM} = V _O = 0.5V		2.6	2.7	V
V _{OL}	Output Voltage Swing Low (Note 5)	No Load		19	40	mV
		I _{SINK} = 0.5mA		39	80	mV
		I _{SINK} = 25mA, V _S = 5V		730	1500	mV
		I _{SINK} = 20mA, V _S = 3V		580	1200	mV

ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$, $V_S = 5\text{V}$, 0V ; $V_S = 3\text{V}$, 0V ; $V_{CM} = V_{OUT} = \text{half supply}$, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	Output Voltage Swing High (Note 5)	No Load	●	16	40	mV
		$I_{SOURCE} = 0.5\text{mA}$	●	55	110	mV
		$I_{SOURCE} = 15\text{mA}$, $V_S = 5\text{V}$	●	860	1700	mV
		$I_{SOURCE} = 10\text{mA}$, $V_S = 3\text{V}$	●	580	1200	mV
I_{SC}	Short-Circuit Current	$V_S = 5\text{V}$	●	± 17	± 36	mA
		$V_S = 3\text{V}$	●	± 12	± 24	mA
I_S	Supply Current per Amplifier		●	4.95	6.2	mA
GBW	Gain-Bandwidth Product (Note 6)	$f = 100\text{kHz}$	●	20	40	MHz
SR	Slew Rate (Note 7)	$V_S = 5\text{V}$, $A_V = -1$, $R_L = \text{Open}$, $V_O = 4\text{V}$	●	11	22	V/ μs
		$V_S = 3\text{V}$, $A_V = -1$, $R_L = \text{Open}$	●	9	18	V/ μs

$T_A = 25^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$		500	2200	μV
		$V_{CM} = V^-$		500	2200	μV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^- \text{ to } V^+$		360	2200	μV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-, V^+$ (Note 4)		700	3500	μV
I_B	Input Bias Current	$V_{CM} = V^+$	0	1.15	2.2	μA
		$V_{CM} = V^-$	-2.2	-1.15	0	μA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- \text{ to } V^+$		2.3	4.4	μA
		Input Bias Current Match (Channel-to-Channel)		50	880	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$		50	440	nA
		$V_{CM} = V^-$		50	440	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- \text{ to } V^+$		36	880	nA
	Input Noise Voltage	0.1Hz to 10Hz		400		nV _{p-p}
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		12		nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		1.6		pA/ $\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance	$f = 100\text{kHz}$		5		pF
A_{VOL}	Large-Signal Voltage Gain	$V_O = -14.5\text{V to } 14.5\text{V}$, $R_L = 10\text{k}$	800	5000		V/mV
		$V_O = -10\text{V to } 10\text{V}$, $R_L = 2\text{k}$	400	2500		V/mV
	Channel Separation	$V_O = -10\text{V to } 10\text{V}$, $R_L = 2\text{k}$	110	127		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^- \text{ to } V^+$	82	98		dB
		CMRR Match (Channel-to-Channel) (Note 4)	80	101		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5\text{V to } \pm 15\text{V}$	82	96		dB
		PSRR Match (Channel-to-Channel) (Note 4)	80	101		dB
V_{OL}	Output Voltage Swing Low (Note 5)	No Load		16	35	mV
		$I_{SINK} = 5\text{mA}$		150	300	mV
		$I_{SINK} = 25\text{mA}$		600	1200	mV
V_{OH}	Output Voltage Swing High (Note 5)	No Load		16	40	mV
		$I_{SOURCE} = 5\text{mA}$		250	500	mV
		$I_{SOURCE} = 25\text{mA}$		1200	2400	mV

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{SC}	Short-Circuit Current		± 35	± 70		mA
I_S	Supply Current per Amplifier			4.6	6	mA
GBW	Gain-Bandwidth Product (Note 6)	$f = 100\text{kHz}$	22	45		MHz
SR	Slew Rate	$A_V = -1$, $R_L = \text{Open}$, $V_O = \pm 10\text{V}$, Measure at $V_O = \pm 5\text{V}$	22	45		V/ μs

$0^\circ\text{C} < T_A < 70^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	V _{CM} = V ⁺ − 0.1V V _{CM} = V [−] + 0.2V	● ●		800 800	2750 2750	μV μV
V _{OS} TC	Input Offset Voltage Drift (Note 2)	V _{CM} = V ⁺ − 0.1V	● ●		6 6		μV/°C μV/°C
ΔV _{OS}	Input Offset Voltage Shift	V _{CM} = V [−] + 0.2V to V ⁺ − 0.1V	●		500	2500	μV
	Input Offset Voltage Match (Channel-to-Channel)	V _{CM} = V [−] + 0.2V, V ⁺ − 0.1V (Note 4)	●		800	4000	μV
I _B	Input Bias Current	V _{CM} = V ⁺ − 0.1V V _{CM} = V [−] + 0.2V	● ●	0 −2.6	1.3 −1.3	2.6 0	μA μA
ΔI _B	Input Bias Current Shift	V _{CM} = V [−] + 0.2V to V ⁺ − 0.1V	●		2.6	5.2	μA
	Input Bias Current Match (Channel-to-Channel)	V _{CM} = V ⁺ − 0.1V (Note 4) V _{CM} = V [−] + 0.2V (Note 4)	● ●		70 70	1040 1040	nA nA
I _{OS}	Input Offset Current	V _{CM} = V ⁺ − 0.1V V _{CM} = V [−] + 0.2V	● ●		70 70	520 520	nA nA
ΔI _{OS}	Input Offset Current Shift	V _{CM} = V [−] + 0.2V to V ⁺ − 0.1V	●		140	1040	nA
A _{VOL}	Large-Signal Voltage Gain	V _O = −14.5V to 14.5V, R _L = 10k V _O = −10V to 10V, R _L = 2k	● ●	600 300	4000 2000		V/mV V/mV
	Channel Separation	V _O = −10V to 10V, R _L = 2k	●	110	125		dB
CMRR	Common Mode Rejection Ratio	V _{CM} = V [−] + 0.2V to V ⁺ − 0.1V	●	81	96		dB
	CMRR Match (Channel-to-Channel) (Note 4)	V _{CM} = V [−] + 0.2V to V ⁺ − 0.1V	●	77	95		dB
PSRR	Power Supply Rejection Ratio	V _S = ±5V to ±15V	●	80	94		dB
	PSRR Match (Channel-to-Channel) (Note 4)	V _S = ±5V to ±15V	●	74	95		dB
V _{OL}	Output Voltage Swing Low (Note 5)	No Load I _{SINK} = 5mA I _{SINK} = 25mA	● ● ●		21 180 680	45 350 1400	mV mV mV
V _{OH}	Output Voltage Swing High (Note 5)	No Load I _{SOURCE} = 5mA I _{SOURCE} = 25mA	● ● ●		15 300 1400	40 600 2800	mV mV mV
I _{SC}	Short-Circuit Current		●	±28	±57		mA
I _S	Supply Current per Amplifier		●		5.2	6.9	mA
GBW	Gain-Bandwidth Product (Note 6)	f = 100kHz	●	20	41		MHz
SR	Slew Rate	A _V = −1, R _L = Open, V _O = ±10V, Measured at V _O = ±5V	●	21	43		V/μs

ELECTRICAL CHARACTERISTICS

–40°C < T_A < 85°C, V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	V _{CM} = V ⁺ – 0.1V	●	1000	3000	μV
		V _{CM} = V [–] + 0.2V	●	1000	3000	μV
V _{OS} TC	Input Offset Voltage Drift (Note 2)	V _{CM} = V ⁺ – 0.1V	●	6		μV/°C
			●	6		μV/°C
ΔV _{OS}	Input Offset Voltage Shift	V _{CM} = V [–] + 0.2V to V ⁺ – 0.1V	●	500	2600	μV
	Input Offset Voltage Match (Channel-to-Channel)	V _{CM} = V [–] + 0.2V, V ⁺ – 0.1V (Note 4)	●	850	4000	μV
I _B	Input Bias Current	V _{CM} = V ⁺ – 0.1V	●	0	1.4	μA
		V _{CM} = V [–] + 0.2V	●	–2.8	–1.4	μA
ΔI _B	Input Bias Current Shift	V _{CM} = V [–] + 0.2V to V ⁺ – 0.1V	●	2.8	5.6	μA
	Input Bias Current Match (Channel-to-Channel)	V _{CM} = V ⁺ – 0.1V (Note 4)	●	75	1120	nA
		V _{CM} = V [–] + 0.2V (Note 4)	●	75	1120	nA
I _{OS}	Input Offset Current	V _{CM} = V ⁺ – 0.1V	●	60	560	nA
		V _{CM} = V [–] + 0.2V	●	60	560	nA
ΔI _{OS}	Input Offset Current Shift	V _{CM} = V [–] + 0.2V to V ⁺ – 0.1V	●	120	1120	nA
A _{VOL}	Large-Signal Voltage Gain	V _O = –14.5V to 14.5V, R _L = 10k	●	500	5000	V/mV
		V _O = –10V to 10V, R _L = 2k	●	250	1800	V/mV
	Channel Separation	V _O = –10V to 10V, R _L = 2k	●	110	124	dB
CMRR	Common Mode Rejection Ratio	V _{CM} = V [–] + 0.2V to V ⁺ – 0.1V	●	81	96	dB
	CMRR Match (Channel-to-Channel) (Note 4)	V _{CM} = V [–] + 0.2V to V ⁺ – 0.1V	●	77	95	dB
PSRR	Power Supply Rejection Ratio	V _S = ±5V to ±15V	●	80	93	dB
	PSRR Match (Channel-to-Channel) (Note 4)	V _S = ±5V to ±15V	●	74	95	dB
V _{OL}	Output Voltage Swing Low (Note 5)	No Load	●	23	50	mV
		I _{SINK} = 5mA	●	187	350	mV
		I _{SINK} = 25mA	●	700	1400	mV
V _{OH}	Output Voltage Swing High (Note 5)	No Load	●	16	40	mV
		I _{SOURCE} = 5mA	●	300	600	mV
		I _{SOURCE} = 25mA	●	1500	3000	mV
I _{SC}	Short-Circuit Current		●	±27	±54	mA
I _S	Supply Current per Amplifier		●	5.3	7	mA
GBW	Gain-Bandwidth Product (Note 6)	f = 100kHz	●	20	40	MHz
SR	Slew Rate	A _V = –1, R _L = Open, V _O = ±10V, Measure at V _O = ±5V	●	18	35	V/μs

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 2: This parameter is not 100% tested.

Note 3: The LT1632/LT1633 are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. Guaranteed I grade parts are available, consult factory.

Note 4: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1633; between the two amplifiers on the LT1632.

Note 5: Output voltage swings are measured between the output and power supply rails.

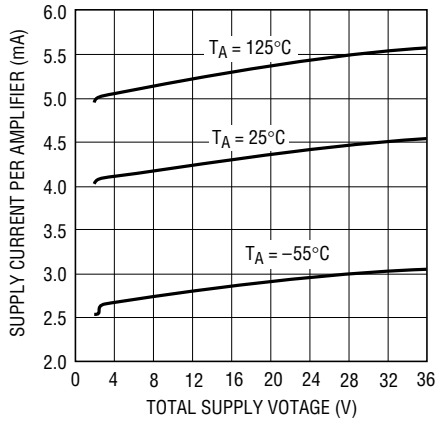
Note 6: V_S = 3V, V_S = ±15V GBW limit guaranteed by correlation to 5V tests.

Note 7: V_S = 3V, V_S = 5V slew rate limit guaranteed by correlation to ±15V tests.

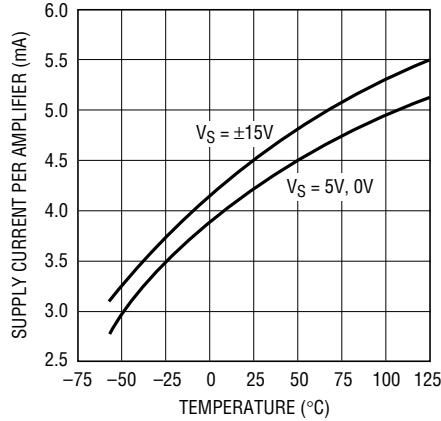
Note 8: Minimum supply voltage is guaranteed by testing the change of V_{OS} to be less than 250μV when the supply voltage is varied from 3V to 2.7V.

TYPICAL PERFORMANCE CHARACTERISTICS

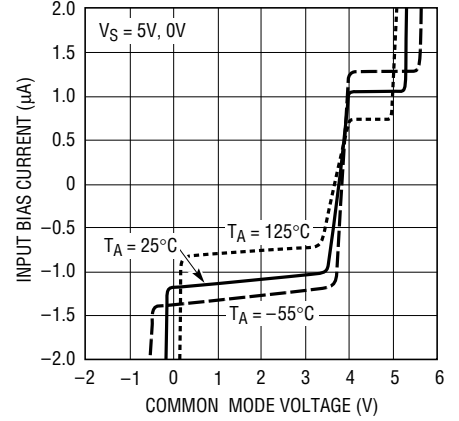
Supply Current vs Supply Voltage



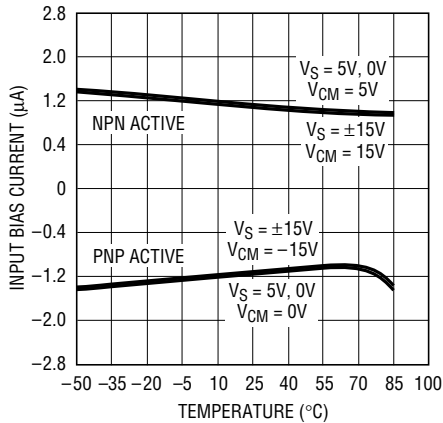
Supply Current vs Temperature



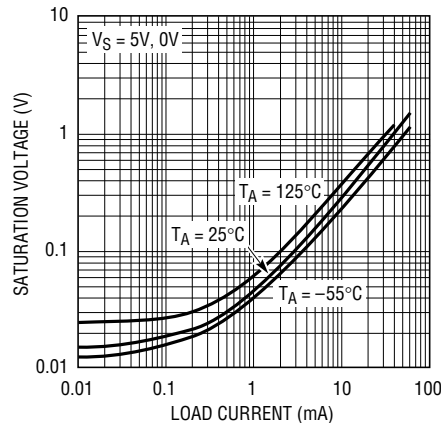
Input Bias Current vs Common Mode Voltage



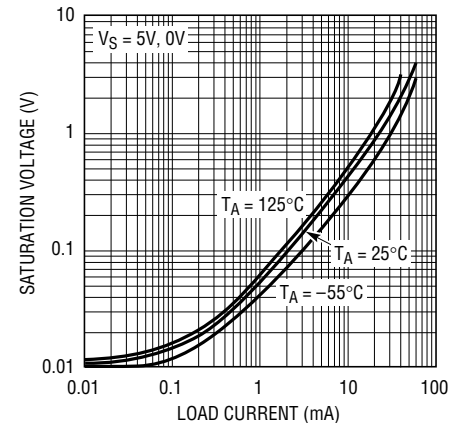
Input Bias Current vs Temperature



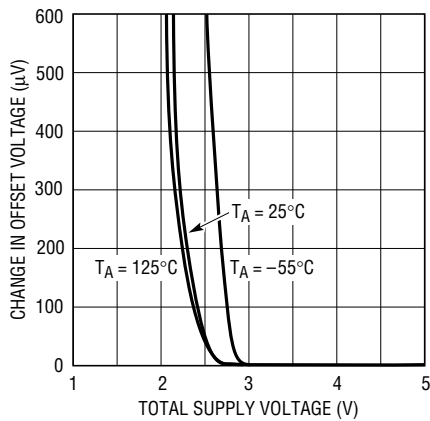
Output Saturation Voltage vs Load Current (Output Low)



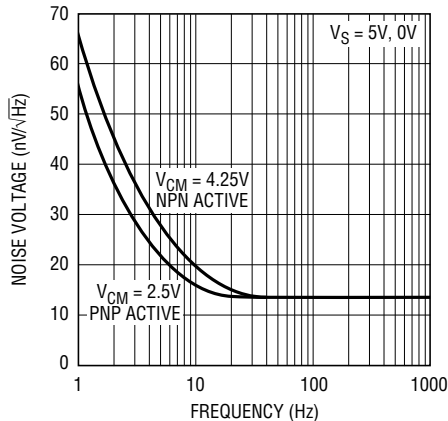
Output Saturation Voltage vs Load Current (Output High)



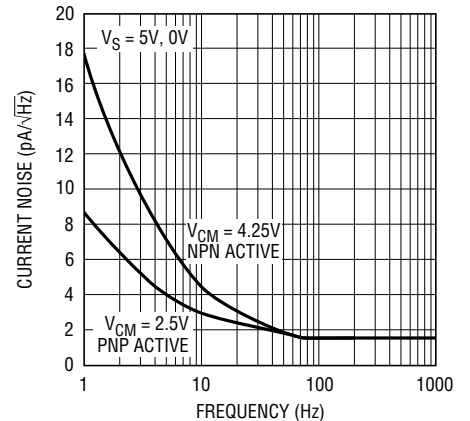
Minimum Supply Voltage



Noise Voltage Spectrum

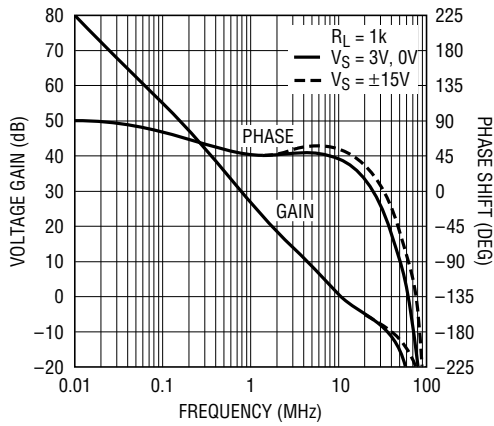


Noise Current Spectrum

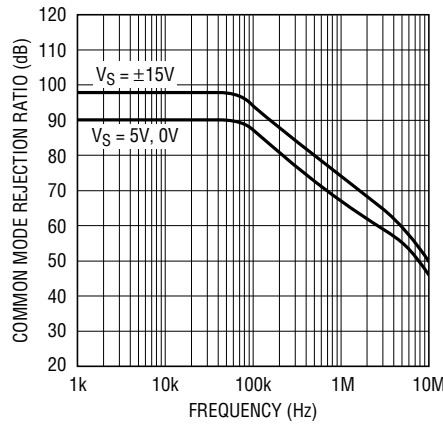


TYPICAL PERFORMANCE CHARACTERISTICS

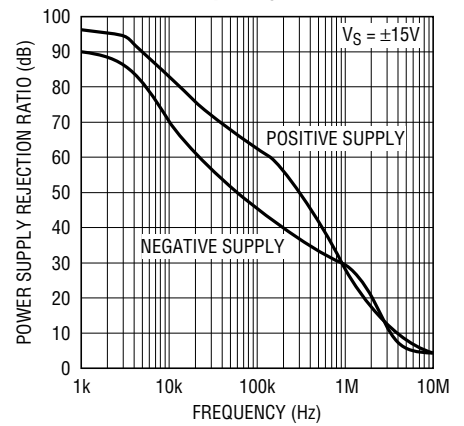
Gain and Phase vs Frequency



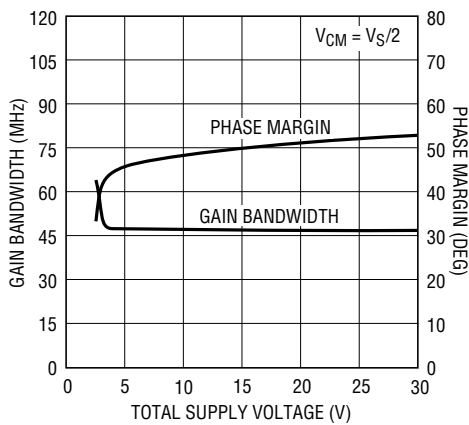
CMRR vs Frequency



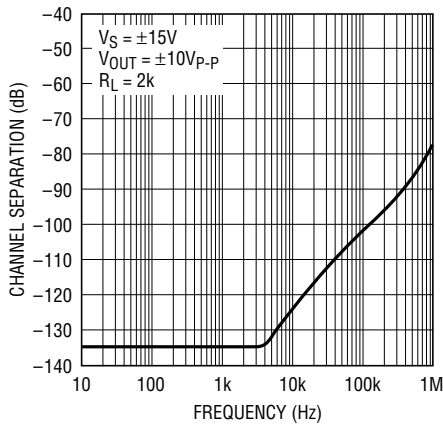
PSRR vs Frequency



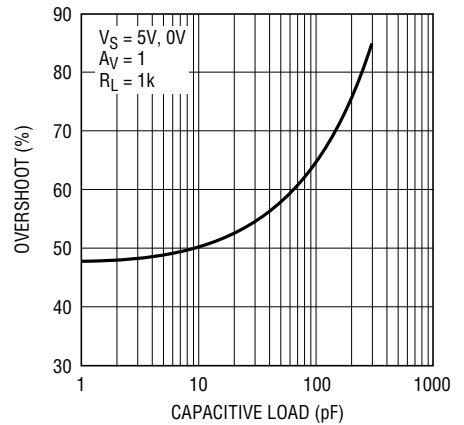
Gain Bandwidth and Phase Margin vs Supply Voltage



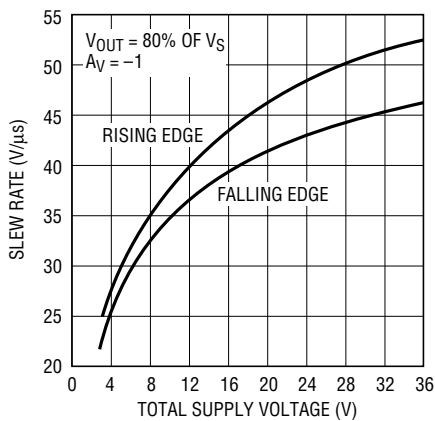
Channel Separation vs Frequency



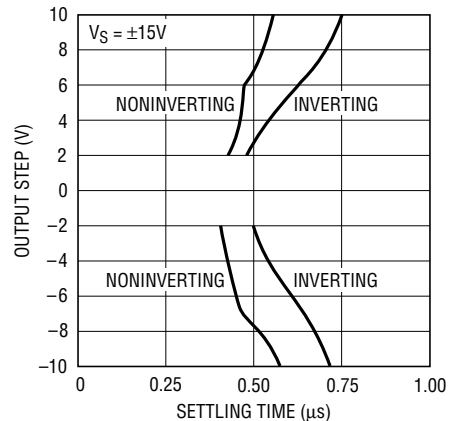
Capacitive Load Handling



Slew Rate vs Supply Voltage

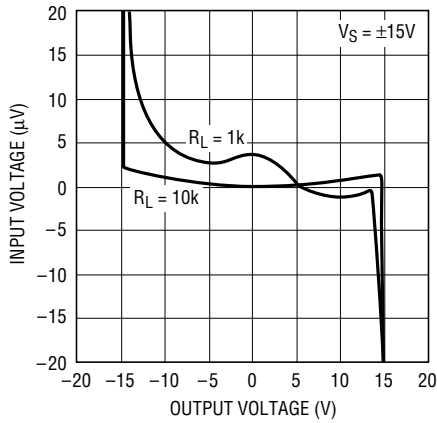


Output Step vs Settling Time to 0.01%

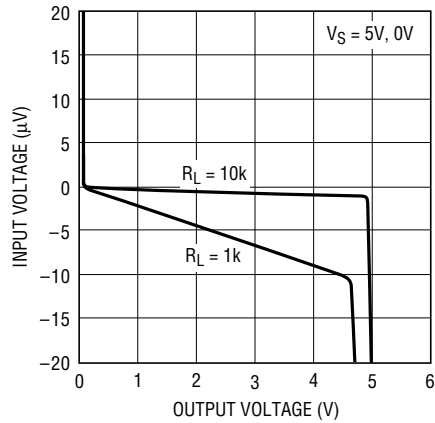


TYPICAL PERFORMANCE CHARACTERISTICS

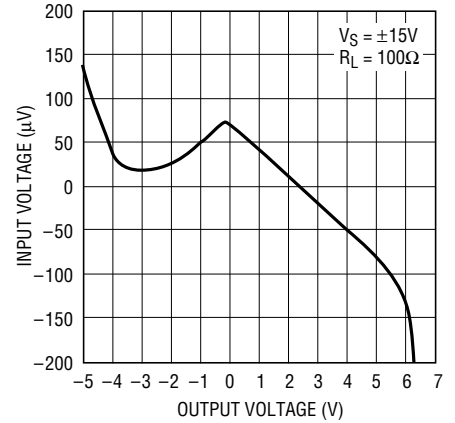
Open-Loop Gain



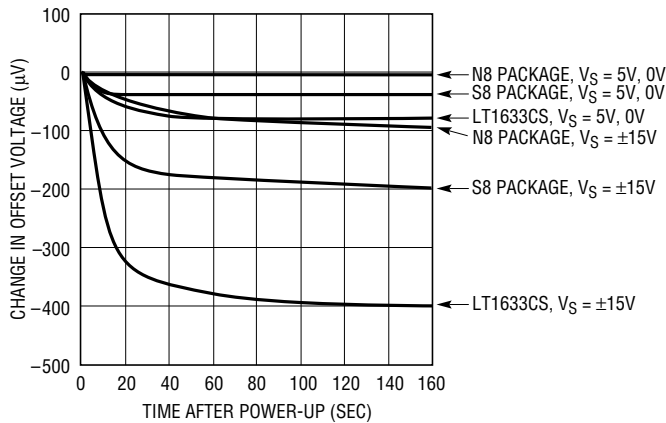
Open-Loop Gain



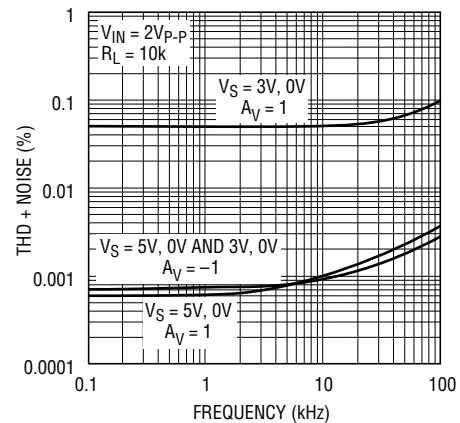
Open-Loop Gain



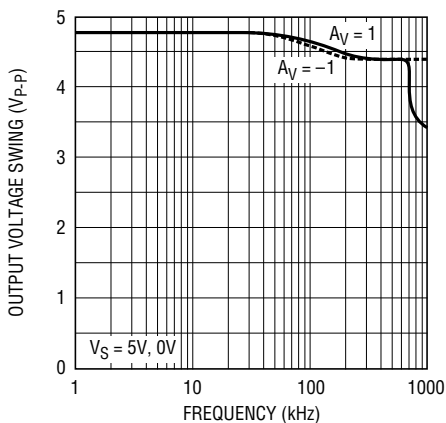
Warm-Up Drift vs Time



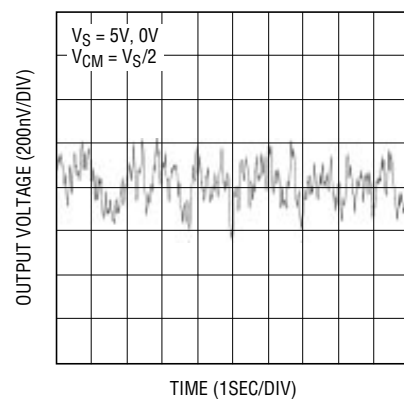
Total Harmonic Distortion + Noise vs Frequency



Maximum Undistorted Output Signal vs Frequency

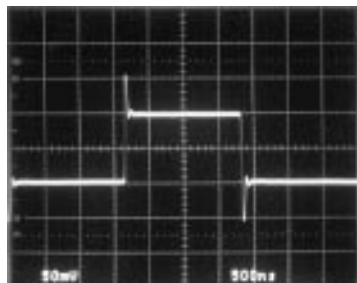


0.1Hz to 10Hz Output Voltage Noise



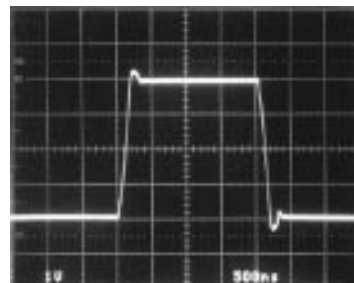
TYPICAL PERFORMANCE CHARACTERISTICS

5V Small-Signal Response



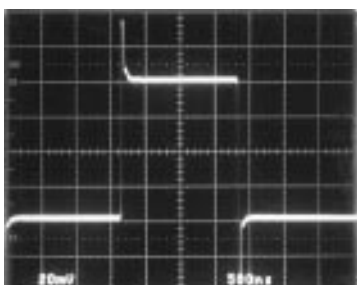
$V_S = 5V, 0V$
 $A_V = 1$
 $R_L = 1k$
 1632/33 G25

5V Large-Signal Response



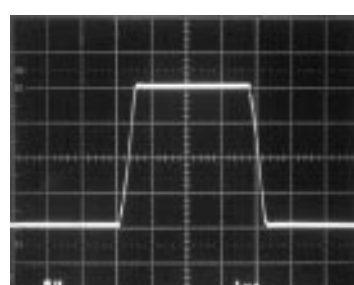
$V_S = 5V, 0V$
 $A_V = 1$
 $R_L = 1k$
 1632/33 G26

$\pm 15V$ Small-Signal Response



$V_S = \pm 15V$
 $A_V = 1$
 $R_L = 1k$
 1632/33 G27

$\pm 15V$ Large-Signal Response



$V_S = \pm 15V$
 $A_V = 1$
 $R_L = 1k$
 1632/33 G28

APPLICATIONS INFORMATION

Rail-to-Rail Input and Output

The LT1632/LT1633 are fully functional for an input and output signal range from the negative supply to the positive supply. Figure 1 shows a simplified schematic of the amplifier. The input stage consists of two differential amplifiers, a PNP stage Q1/Q2 and an NPN stage Q3/Q4 that are active over different ranges of input common mode voltage. The PNP differential input pair is active for input common mode voltages V_{CM} between the negative supply to approximately 1.5V below the positive supply. As V_{CM} moves closer toward the positive supply, the transistor Q5 will steer the tail current I_1 to the current mirror Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the rest of the input common mode range up to the positive supply.

The output is configured with a pair of complementary common emitter stages Q14/Q15 that enables the output to swing from rail to rail. These devices are fabricated on Linear Technology's proprietary complementary bipolar process to ensure similar DC and AC characteristics. Capacitors C1 and C2 form local feedback loops that lower the output impedance at high frequencies.

Power Dissipation

The LT1632/LT1633 amplifiers combine high speed and large output current drive in a small package. Because the amplifiers operate over a very wide supply range, it is possible to exceed the maximum junction temperature of 150°C in plastic packages under certain conditions. Junc-

APPLICATIONS INFORMATION

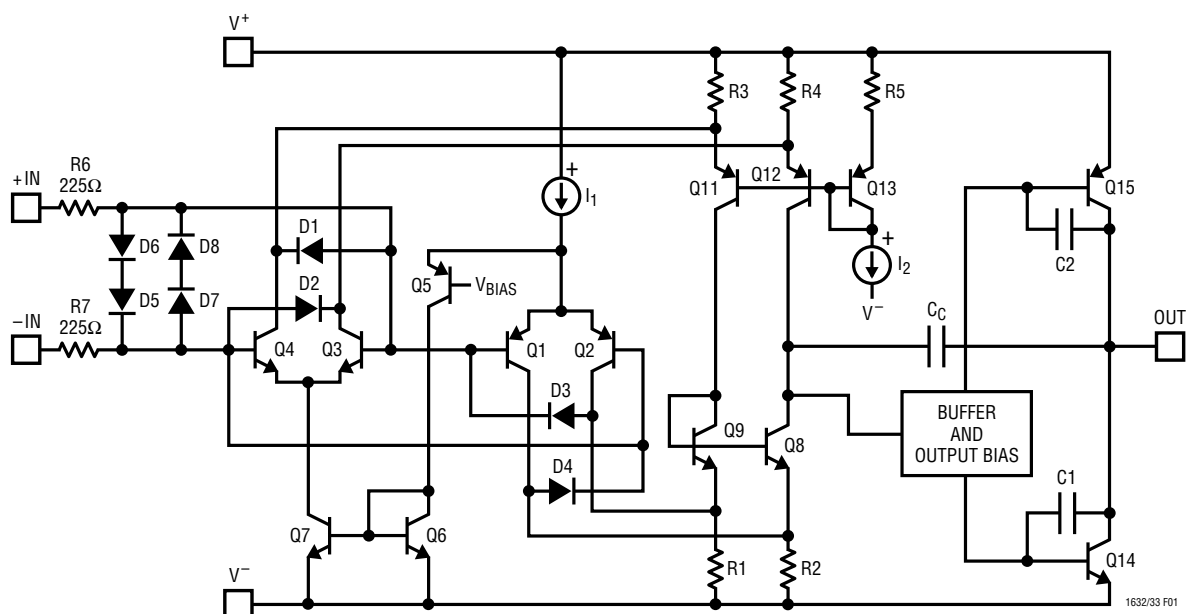


Figure 1. LT1632 Simplified Schematic Diagram

tion temperature T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

$$\text{LT1632CN8: } T_J = T_A + (P_D \cdot 130^\circ\text{C/W})$$

$$\text{LT1632CS8: } T_J = T_A + (P_D \cdot 190^\circ\text{C/W})$$

$$\text{LT1633CS: } T_J = T_A + (P_D \cdot 150^\circ\text{C/W})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and load resistance. For a given supply voltage, the worst-case power dissipation $P_{D\text{MAX}}$ occurs at the maximum supply current and when the output voltage is at half of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore $P_{D\text{MAX}}$ is given by:

$$P_{D\text{MAX}} = (V_S \cdot I_{S\text{MAX}}) + (V_S/2)^2/R_L$$

To ensure that the LT1632/LT1633 are used properly, calculate the worst-case power dissipation, use the thermal resistance for a chosen package and its maximum

junction temperature to derive the maximum ambient temperature.

Example: An LT1632CS8 operating on $\pm 15\text{V}$ supplies and driving a 500Ω , the worse-case power dissipation per amplifier is given by:

$$\begin{aligned} P_{D\text{MAX}} &= (30\text{V} \cdot 5.6\text{mA}) + (15\text{V} - 7.5\text{V})(7.5/500) \\ &= 0.168 + 0.113 = 0.281\text{W} \end{aligned}$$

If both amplifiers are loaded simultaneously, then the total power dissipation is 0.562W . The SO-8 package has a junction-to-ambient thermal resistance of 190°C/W in still air. Therefore, the maximum ambient temperature that the part is allowed to operate is:

$$\begin{aligned} T_A &= T_J - (P_{D\text{MAX}} \cdot 190^\circ\text{C/W}) \\ T_A &= 150^\circ\text{C} - (0.562\text{W} \cdot 190^\circ\text{C/W}) = 43^\circ\text{C} \end{aligned}$$

For a higher operating temperature, lower the supply voltage or use the DIP package part.

APPLICATIONS INFORMATION

Input Offset Voltage

The offset voltage changes depending upon which input stage is active, and the maximum offset voltages are trimmed to less than $1350\mu\text{V}$. To maintain the precision characteristics of the amplifier, the change of V_{OS} over the entire input common mode range (CMRR) is guaranteed to be less than $1500\mu\text{V}$ on a single 5V supply.

Input Bias Current

The input bias current polarity depends on the input common mode voltage. When the PNP differential pair is active, the input bias currents flow out of the input pins. They flow in the opposite direction when the NPN input stage is active. The offset voltage error due to input bias currents can be minimized by equalizing the noninverting and inverting input source impedance.

Output

The outputs of the LT1632/LT1633 can deliver large load currents; the short-circuit current limit is 70mA. Take care to keep the junction temperature of the IC below the absolute maximum rating of 150°C (refer to the Power Dissipation section). The output of these amplifiers have reverse-biased diodes to each supply. If the output is forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to several hundred mA, no damage to the part will occur.

Overdrive Protection

To prevent the output from reversing polarity when the input voltage exceeds the power supplies, two pairs of crossing diodes D1 to D4 are employed. When the input voltage exceeds either power supply by approximately 700mV, D1/D2 or D3/D4 will turn on, forcing the output to the proper polarity. For this phase reversal protection to work properly, the input current must be limited to less than 5mA. If the amplifier is to be severely overdriven, an external resistor should be used to limit the overdrive current.

The LT1632/LT1633's input stages are also protected against large differential input voltages by a pair of back-to-back diodes D5/D8. When a differential voltage of more than 1.4V is applied to the inputs, these diodes will turn on, preventing the emitter-base breakdown of the input transistors. The current in D5/D8 should be limited to less than 10mA. Internal 225Ω resistors R6 and R7 will limit the input current for differential input signals of 4.5V or less. For larger input levels, a resistor in series with either or both inputs should be used to limit the current. Worst-case differential input voltage usually occurs when the output is shorted to ground. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins.

Capacitive Load

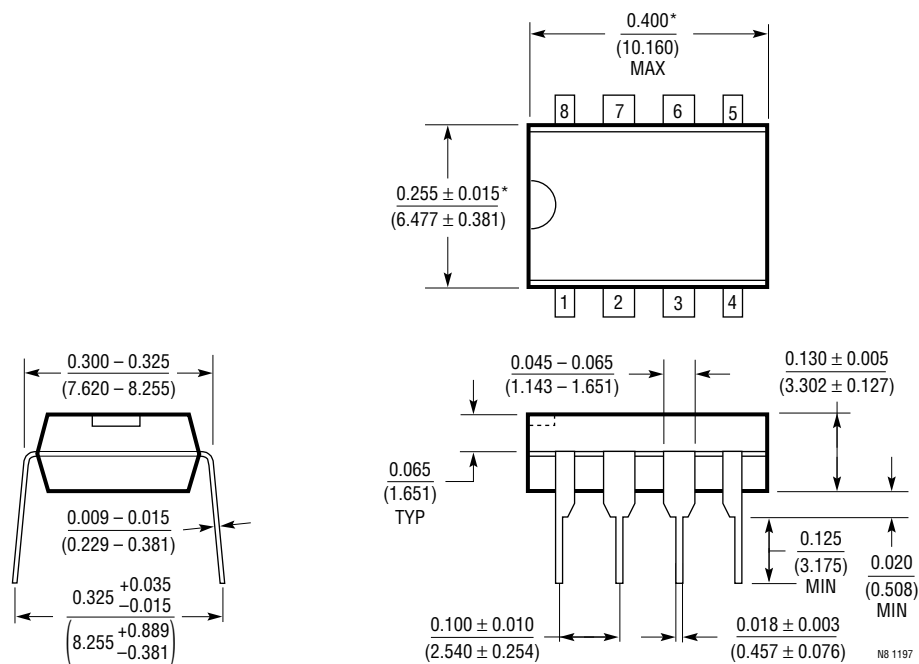
The LT1632/LT1633 are wideband amplifiers that can drive capacitive loads up to 200pF on $\pm 15\text{V}$ supplies in a unity-gain configuration. On a 3V supply, the capacitive load should be kept to less than 100pF. When there is a need to drive larger capacitive loads, a resistor of a couple hundred ohms should be connected between the output and the capacitive load. The feedback should still be taken from the output so that the resistor isolates the capacitive load to ensure stability.

Feedback Components

The low input bias currents of the LT1632/LT1633 make it possible to use the high value feedback resistors to set the gain. However, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT1632/LT1633 in a noninverting gain of 2, set with two 20k resistors, will probably oscillate with 10pF total input capacitance (5pF input capacitance and 5pF board capacitance). The amplifier has a 6MHz crossing frequency and a 55° phase margin at 6dB of gain. The feedback resistors and the total input capacitance form a pole at 1.6MHz that induces a phase shift of 75° at 5MHz! The solution is simple: either lower the value of the resistors or add a feedback capacitor of 10pF or more.

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

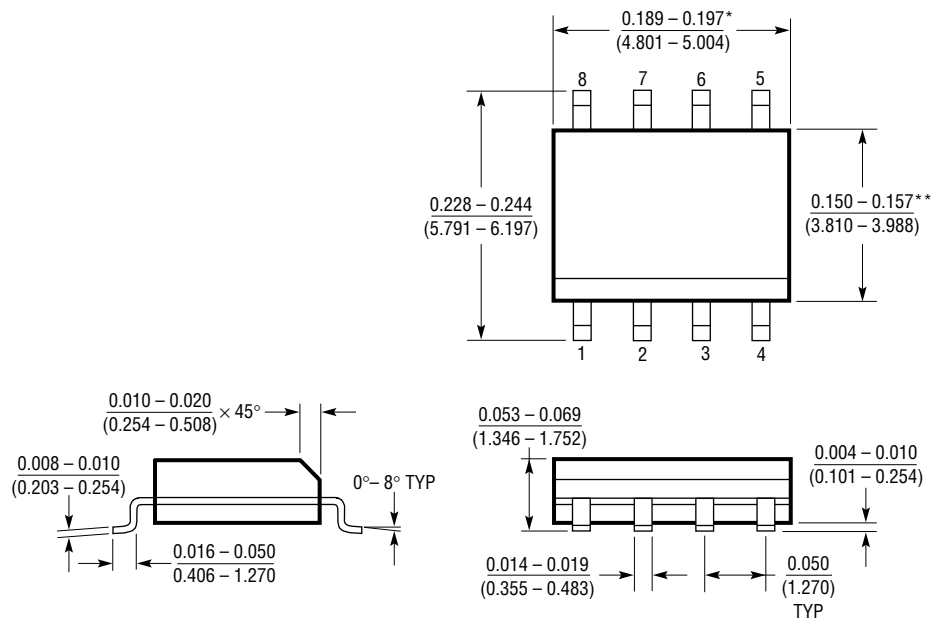
N8 Package **8-Lead PDIP (Narrow 0.300)** (LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

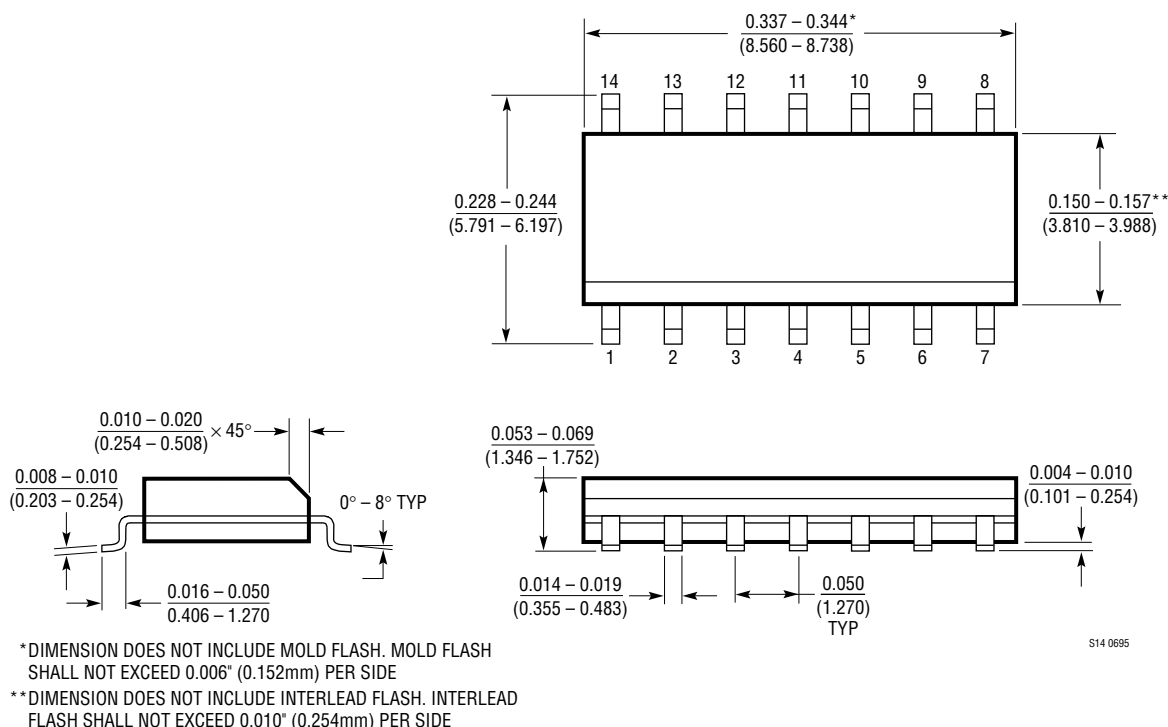
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package 14-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1211/LT1212	Dual/Quad 14MHz, 7V/μs, Single Supply Precision Op Amps	Input Common Mode Includes Ground, 275μV V _{OS(MAX)} , 6μV/°C Max Drift, Max Supply Current 1.8mA per Op Amp
LT1213/LT1214	Dual/Quad 28MHz, 12V/μs, Single Supply Precision Op Amps	Input Common Mode Includes Ground, 275μV V _{OS(MAX)} , 6μV/°C Max Drift, Max Supply Current 3.5mA per Op Amp
LT1215/LT1216	Dual/Quad 23MHz, 50V/μs, Single Supply Precision Op Amps	Input Common Mode Includes Ground, 450μV V _{OS(MAX)} , 6μV/°C Max Drift, Max Supply Current 6.6mA per Op Amp
LT1498/LT1499	Dual/Quad 10MHz, 6V/μs Rail-to-Rail Input and Output C-Load™ Op Amps	High DC Accuracy, 475μV V _{OS(MAX)} , 4μV/°C Max Drift, Max Supply Current 2.2mA per Amp
LT1630/LT1631	Dual/Quad 30MHz, 10V/μs Rail-to-Rail Input and Output Op Amps	High DC Accuracy, 525μV V _{OS(MAX)} , 70mA Output Current, Max Supply Current 4.4mA per Amp

C-Load is a trademark of Linear Technology Corporation.