LTC1552

# Digitally Controlled Synchronous Switching Regulator Controller for Pentium® Pro Processor

September 1996

## FEATURES

- Digitally Programmable 2.1V to 3.5V Fixed Output Voltage with 100mV Steps
- Provides All Features Required by the Intel Pentium® Pro Processor VRM 8.0 DC/DC Converter Specification
- Flags for Power Good, Over Temperature and Over Voltage Fault
- Output Current Exceeds 14A from a 5V or 12V Supply
- Dual N-Channel MOSFET Synchronous Drive
- Excellent Output Regulation: ±1% Over Line, Load and Temperature Variations
- High Efficiency: Over 95% Possible
- Adjustable Current Limit Without External Sense Resistors
- Fast Transient Response
- Available in SSOP-20 Package

## APPLICATIONS

- Power Supply for Pentium Pro, SPARC, ALPHA and PA-RISC Microprocessors
- High Power 5V or 12V/2.1V - 3.5V Regulators

## DESCRIPTION

The LTC®1552 is a high power, high efficiency switching regulator controller optimized for 5V or 12V input to 2.1V - 3.5V output applications. It features digitally programmable output voltage, a precision internal reference and an internal feedback system that can provide output regulation of ±1% over temperature, load current and line voltage shifts. The LTC1552 uses a synchronous switching architecture with two external N-channel output devices, eliminating the need for a high power, high cost P-channel device. Additionally, it senses the output current across the on resistance of the upper N-channel FET, providing an adjustable current limit without an external low value sense resistor.

The LTC1552 free runs at 300kHz, and can be synchronized to a faster external clock if desired. It includes all the inputs and outputs required to implement a power supply conforming to the Intel Pentium Pro Processor VRM 8.0 DC/DC Converter Specification.



## TYPICAL APPLICATION

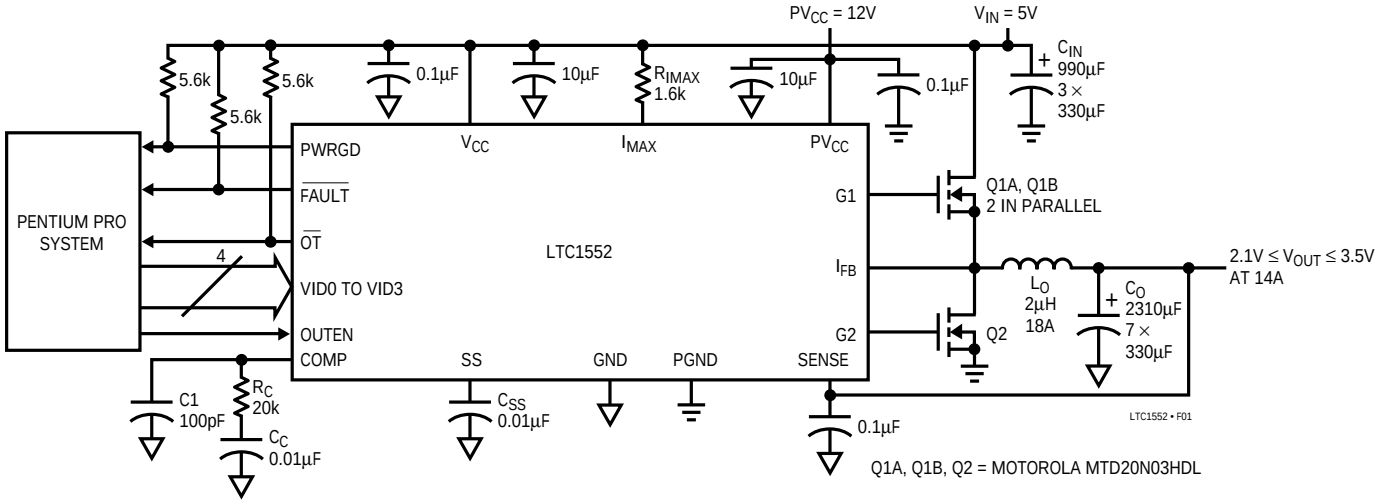



Figure 1. 5V to 2.1V - 3.5V Supply Application

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage

$V_{CC}$ ..... 7V

$PV_{CC}$ ..... 20V

Input Voltage

$I_{FB}$ ..... –0.3V to $PV_{CC}$ + 0.3V

$I_{MAX}$ ..... –0.3V to 13V

All Other Inputs ..... –0.3V to $V_{CC}$ + 0.3V

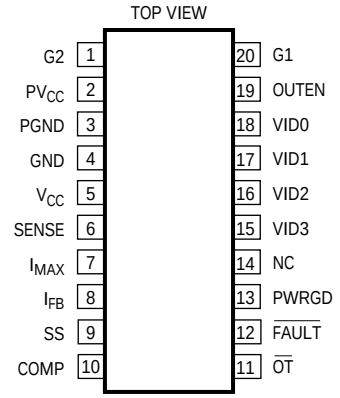
Digital Output Voltage ..... –0.3V to 13V

Operating Temperature Range ..... 0°C to 70°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION




G PACKAGE
20-LEAD PLASTIC SSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 96°C/W

| ORDER PART NUMBER |
|---|
| LTC1552CG |

Consult factory for Industrial and Military grade parts.

## ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5V, $PV_{CC}$ = 12V, $T_A$ = 25°C unless otherwise noted (Note 2).

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | ● | 4.5 | | 5.5 | V |
| $PV_{CC}$ | Supply Voltage for G1 and G2 | | ● | | | 18 | V |
| $V_{FB}$ | Internal Feedback Voltage | (Note 3) | | | 1.265 | | V |
| $V_{OUT}$ | Output Voltage | Figure 2, % Error wrt Rated Output Voltage | ● | –3 | | 3 | % |
| $\Delta V_{OUT}$ | Output Load Regulation<br>Output Line Regulation | Figure 2, $I_{OUT}$ = 0A to 12A (Note 3)<br>Figure 2, $V_{IN}$ = 4.75V to 5.25V (Note 3) | | | ±7<br>±5 | | mV<br>mV |
| $V_{PWRGD}$ | Positive Power Good Trip Point<br>Negative Power Good Trip Point | Figure 2, % Above Rated Output Voltage<br>Figure 2, % Below Rated Output Voltage | ●<br>● | 3<br>–7 | 5<br>–5 | 7<br>–3 | %<br>% |
| $V_{FAULT}$ | $\overline{FAULT}$ Trip Point | Figure 2, % Above Rated Output Voltage | ● | 12 | 15 | 18 | % |
| $I_{CC}$ | Normal Supply Current<br>Shutdown Supply Current | Figure 3, OUTEN = $V_{CC}$ (Note 4)<br>Figure 3, OUTEN = 0, VID0, VID1, VID2, VID3 Floating | ●<br>● | | 700<br>150 | 1500<br>300 | µA<br>µA |
| $I_{PVCC}$ | Supply Current | Figure 3, $PV_{CC}$ = 12V, OUTEN = $V_{CC}$ (Note 5)<br>$PV_{CC}$ = 12V, OUTEN = 0, VID0, VID1, VID2, VID3 Floating | | | 15<br>1 | | mA<br>µA |
| $f_{OSC}$ | Internal Oscillator Frequency | Figure 4 | ● | 270 | 300 | 330 | kHz |
| $G_{ERR}$ | Error Amplifier Open-Loop DC Gain | (Note 6) | | | 53 | | dB |
| $g_{mERR}$ | Error Amplifier Transconductance | (Note 6) | ● | 0.75 | 1.1 | 1.45 | mMho |
| $I_{IMAX}$ | $I_{MAX}$ Sink Current | $V_{IMAX}$ = $V_{CC}$ | | | 185 | | µA |
| $I_{SS}$ | Soft Start Source Current | $V_{SS}$ = 0V, $V_{IMAX}$ = 0V, $V_{IFB}$ = $V_{CC}$ | | | –14 | | µA |
| $I_{SSIL}$ | Maximum Soft Start Sink Current Under Current Limit | $V_{SENSE}$ = $V_{OUT}$, $V_{IMAX}$ = $V_{CC}$, $V_{IFB}$ = 0V (Notes 7, 8) | ● | 90 | 130 | 170 | µA |
| $I_{SSHIL}$ | Soft Start Sink Current Under Hard Current Limit | $V_{SENSE}$ = 0V, $V_{IMAX}$ = $V_{CC}$, $V_{IFB}$ = 0V | ● | 40 | 65 | 120 | mA |
| $t_{SSHIL}$ | Hard Current Limit Hold Time | $V_{SENSE}$ = 0V, $V_{IMAX}$ = 4V, $V_{IFB}$↓ from 5V | ● | 120 | 180 | 230 | µs |
| $t_{PWRGD}$<br>$t_{PWRBAD}$ | Power Good Response Time↑<br>Power Good Response Time↓ | $V_{SENSE}$↑ from 0V to Rated $V_{OUT}$<br>$V_{SENSE}$↓ from Rated $V_{OUT}$ to 0V | ●<br>● | 210<br>60 | 300<br>100 | 400<br>140 | µs<br>µs |
| $t_{FAULT}$ | $\overline{FAULT}$ Response Time | $V_{SENSE}$↑ from Rated $V_{OUT}$ to $V_{CC}$ | ● | 60 | 100 | 140 | µs |
| $t_{OT}$ | $\overline{OT}$ Response Time | Figure 3, OUTEN↓, VID0, VID1, VID2, VID3 = 0 (Note 9) | ● | 20 | 30 | 60 | µs |
| $V_{OT}$ | Over Temperature Trip Point | Figure 3, OUTEN↓, VID0, VID1, VID2, VID3 = 0 (Note 9) | ● | 1.9 | 2 | 2.1 | V |

## ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5V, $PV_{CC}$ = 12V, $T_A$ = 25°C unless otherwise noted (Note 2).

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OTDD}$ | Over Temperature Driver Disable | Figure 3, OUTEN↓, VID0, VID1, VID2, VID3 = 0 (Note 9) | ● | 1.6 | 1.7 | 1.8 | V |
| $V_{SHDN}$ | Shutdown | Figure 3, OUTEN↓, VID0, VID1, VID2, VID3 = 0 (Note 9) | ● | 0.8 | 1.2 | 1.55 | V |
| $t_R$, $t_F$ | Diver Rise and Fall Time | Figure 4 | ● | | 90 | 140 | ns |
| $t_{NOL}$ | Driver Nonoverlap Time | Figure 4 | ● | 30 | 100 | | ns |
| $DC_{MAX}$ | Maximum G1 Duty Cycle | Figure 4 | ● | 82 | 85 | 90 | % |
| $V_{IH}$ | VID0, VID1, VID2, VID3 Input High Voltage | | ● | 2 | | | V |
| $V_{IL}$ | VID0, VID1, VID2, VID3 Input Low Voltage | | ● | | | 0.8 | V |
| $R_{IN}$ | VID0, VID1, VID2, VID3 Internal Pull-Up | | | | 5.6 | | kΩ |
| $I_{SINK}$ | Digital Output Sink Current | | | | 10 | | mA |

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: This parameter is guaranteed by correlation and is not tested directly.

Note 4: OUTEN is internally pulled low if VID0, VID1, VID2, VID3 are floating. Due to the internal pull-up resistors, there will be an additional 1mA/pin if any of the VID0, VID1, VID2, VID3 pins are pulled low.

Note 5: Supply current in normal operation is dominated by the current needed to charge and discharge the external FET gates. This will vary with the LTC1552 operating frequency, supply voltage and the external FETs used.

Note 6: The open loop DC gain and transconductance from the SENSE pin to COMP pin will be $(G_{ERR})(1.265/3.3)$ and $(g_{mERR})(1.265/3.3)$ respectively.

Note 7: The current limiting amplifier can sink but cannot source current. Under normal (not current limited) operation, the output current will be zero.

Note 8: Under typical soft current limit, the net soft start discharge current will be $130\mu A\ I_{SSIL} + (-14\mu A)(I_{SS}) = 116\mu A$. The soft start sink-to-source current ratio is designed to be 13:1.

Note 9: When VID0, VID1, VID2, VID3 are all high, OUTEN will be forced low internally. The OUTEN trip voltages are guaranteed for all other input codes.

## PIN FUNCTIONS

G2 (Pin 1): Gate Drive for the Lower N-Channel MOSFET, Q2. This output will swing from $PV_{CC}$ to PGND. It will always be low when G1 is high or when the output is disabled. To prevent undershoot during a soft start cycle, G2 is held low until G1 first goes high.

$PV_{CC}$ (Pin 2): Power Supply for G1 and G2. $PV_{CC}$ must be connected to a potential of at least $V_{IN} + V_{GS(ON)Q1}$. If $V_{IN}$ = 5V, $PV_{CC}$ can be generated using a simple charge pump connected to the switching node between Q1 and Q2 (see Figure 7), or it can be connected to an auxiliary 12V supply if one exists. For applications where $V_{IN}$ = 12V, $PV_{CC}$ can be generated using a 5V + 12V charge pump (see Figure 9).

PGND (Pin 3): Power Ground. PGND should be connected to a low impedance ground plane in close proximity to the source of Q2.

GND (Pin 4): Signal Ground. GND is connected to the low power internal circuitry and should be connected to the negative terminal of the output capacitor where it returns to the ground plane. PGND and GND should form a star connection right at this pin.

$V_{CC}$ (Pin 5): Power Supply. Power for the internal low power circuitry. $V_{CC}$ should be wired separately from the drain of Q1 if they share the same supply. A 10µF bypass capacitor is recommended from this pin to GND.

SENSE (Pin 6): Output Voltage Pin. Connect to the positive terminal of the output capacitor. SENSE is a very sensitive pin; for optimum performance, it requires an external 0.1µF capacitor from this pin to GND.

$I_{MAX}$ (Pin 7): Current Limit Threshold. This is set by the voltage drop across an external resistor connected between the drain of Q1 and $I_{MAX}$. There is a 185µA internal pull-down at $I_{MAX}$.

## PIN FUNCTIONS

$I_{FB}$ (Pin 8): Current Limit Sense Pin. Connect to the switching node between the source of Q1 and the drain of Q2. If $I_{FB}$ drops below $I_{MAX}$ when G1 is on, the LTC1552 will go into current limit. The current limit circuit can be disabled by floating $I_{MAX}$ and shorting $I_{FB}$ to $V_{CC}$. For $V_{IN}$ = 12V, a 15V Zener diode from $I_{FB}$ to PGND is recommended to prevent the voltage spike at $I_{FB}$ from exceeding the maximum voltage rating.

SS (Pin 9): Soft Start. Connect to an external capacitor to implement a soft start function. During moderate overload conditions, the soft start capacitor will be discharged slowly in order to reduce the duty cycle. In hard current limit, the soft start capacitor will be forced low immediately and the LTC1552 will rerun a complete soft start cycle. $C_{SS}$ must be selected such that during power-up the total surge current through Q1 will not exceed the current limit value.

COMP (Pin 10): External Compensation. The COMP pin is connected directly to the output of the error amplifier and the input of the PWM comparator. An RC network is used at this node to compensate the feedback loop to provide optimum transient response.

$\overline{OT}$ (Pin 11): Over Temperature Fault. $\overline{OT}$ is an open drain output and will be pulled low if OUTEN is less than 2V. If OUTEN = 0, $\overline{OT}$ pulls low.

$\overline{FAULT}$ (Pin 12): Fault Condition. $\overline{FAULT}$ is an open drain output. If $V_{OUT}$ reaches 15% above the rated value, $\overline{FAULT}$ will go low and G1 and G2 will be disabled. Once triggered, the LTC1552 will remain in this state until the power supply is recycled or the OUTEN pin is toggled. If OUTEN = 0, $\overline{FAULT}$ floats.

PWRGD (Pin 13): Open Drain Signal to Indicate Validity of Output Voltage. A high indicates that the output has settled to within ±5% of the rated output for more than 300µs. PWRGD will go low if the output is out of regulation for more than 100µs. If OUTEN = 0, PWRGD pulls low.

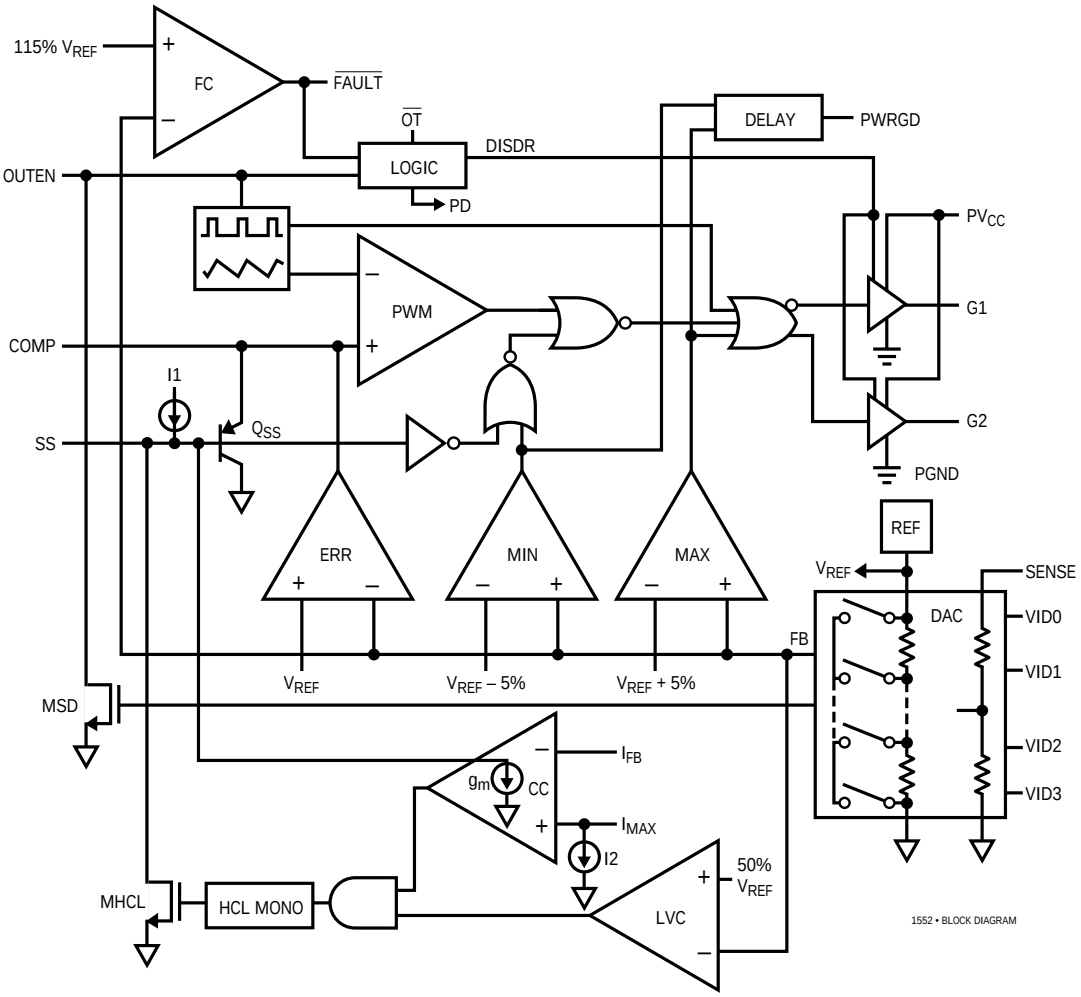
NC (Pin 14): No Internal Connection. This pin will be VID4 in a future version of the LTC1552 conforming to the Intel VRM 8.1 specification.

VID0, VID1, VID2, VID3 (Pins 18, 17, 16, 15): Digital Voltage Select. TTL inputs used to set the regulated output voltage required by the processor (Table 3). There is an internal 5.6k pull-up at each pin. When all four VID*n* pins are high or floating, the OUTEN pin is forced to GND internally and the chip will shut down.

OUTEN (Pin 19): Output Enable. TTL input which enables the output voltage. The external MOSFET temperature can be monitored with an external thermistor as shown in Figure 13. When the OUTEN input voltage drops below 2V, $\overline{OT}$ trips. As OUTEN drops below 1.7V, the drivers are internally disabled to prevent the MOSFETs from heating further. If OUTEN is less than 1.2V for longer than 30µs, the LTC1552 will enter shutdown mode. The internal oscillator can be synchronized to an external clock by applying the external clocking signal to the OUTEN pin.

G1 (Pin 20): Gate Drive for the Upper N-Channel MOSFET, Q1. This output will swing from $PV_{CC}$ to PGND. It will always be low when G2 is high or the output is disabled.

# BLOCK DIAGRAM




# TEST CIRCUITS

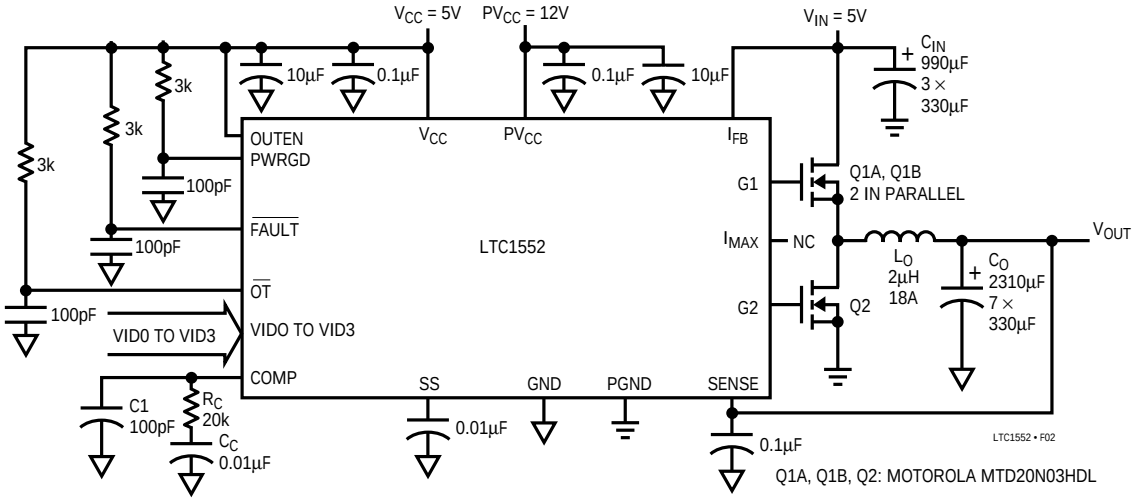



Figure 2

## TEST CIRCUITS

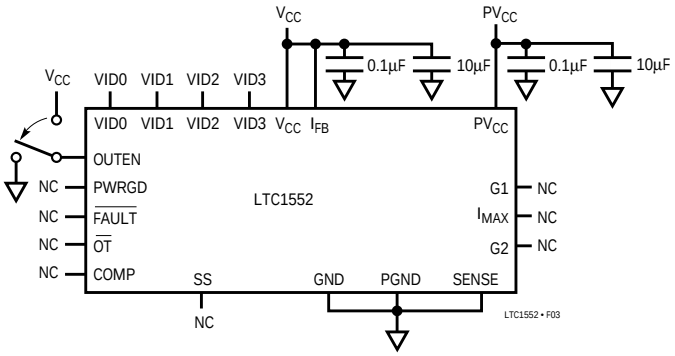



Figure 3

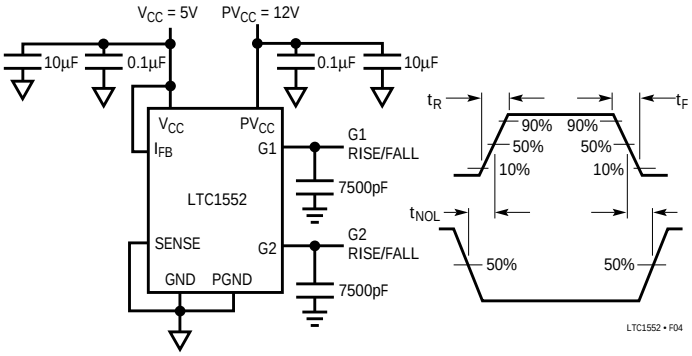



Figure 4

## FUNCTION TABLES

Table 1. $\overline{OT}$ Logic

| INPUT OUTEN (V) | OUTPUT $\overline{OT}$* |
|---|---|
| <2 | 0 |
| >2 | 1 |

Table 2. PWRGD and $\overline{FAULT}$ Logic

| INPUT | | OUTPUT* | | |
|---|---|---|---|---|
| OUTEN | $V_{SENSE}$** | $\overline{OT}$ | $\overline{FAULT}$ | PWRGD |
| 0 | X | 0 | 1 | 0 |
| 1 | <95% | 1 | 1 | 0 |
| 1 | >95%/<105% | 1 | 1 | 1 |
| 1 | >105% | 1 | 1 | 0 |
| 1 | >115% | 1 | 0 | 0 |

* With external pull-up resistor.
** With respect to the rated output voltage.
X Don't care.

Table 3. Rated Output Voltage

| INPUT PIN | | | | RATED OUTPUT VOLTAGE (V) |
|---|---|---|---|---|
| VID3 | VID2 | VID1 | VID0 | |
| 1 | 1 | 1 | 1 | SHUTDOWN |
| 1 | 1 | 1 | 0 | 2.1 |
| 1 | 1 | 0 | 1 | 2.2 |
| 1 | 1 | 0 | 0 | 2.3 |
| 1 | 0 | 1 | 1 | 2.4 |
| 1 | 0 | 1 | 0 | 2.5 |
| 1 | 0 | 0 | 1 | 2.6 |
| 1 | 0 | 0 | 0 | 2.7 |
| 0 | 1 | 1 | 1 | 2.8 |
| 0 | 1 | 1 | 0 | 2.9 |
| 0 | 1 | 0 | 1 | 3.0 |
| 0 | 1 | 0 | 0 | 3.1 |
| 0 | 0 | 1 | 1 | 3.2 |
| 0 | 0 | 1 | 0 | 3.3 |
| 0 | 0 | 0 | 1 | 3.4 |
| 0 | 0 | 0 | 0 | 3.5 |

# APPLICATIONS INFORMATION

## OVERVIEW

The LTC1552 is a voltage feedback synchronous switching regulator controller (see Block Diagram) designed for use in high power, low voltage step-down (buck) converters. It is designed to satisfy the requirements of the Intel Pentium Pro power supply specification. It includes an on-chip DAC to control the output voltage, a PWM generator, a precision reference trimmed to ±1%, two high power MOSFET gate drivers and all the necessary feedback and control circuitry to form a complete switching regulator circuit.

The LTC1552 includes a current limit sensing circuit that uses the upper external power MOSFET as a current sensing element, eliminating the need for an external sense resistor. Once the current comparator, CC, detects an over-current condition, the duty cycle is reduced by discharging the soft start capacitor through a voltage controlled current source. Under severe overloads or output short-circuit conditions, the chip will be repeatedly forced into soft start until the short is removed, preventing the external components from being damaged. Under output overvoltage conditions, the MOSFET drivers will be disabled permanently until the chip power supply is recycled or the OUTEN pin is toggled.

OUTEN can optionally be connected to an external negative temperature coefficient (NTC) thermistor placed near the external MOSFETs or the microprocessor. Three threshold levels are internally provided to prevent the external circuitry from overheating. When OUTEN drops to 2V, $\overline{OT}$ will trip, issuing a warning to the external CPU. If the temperature continues to rise and the OUTEN input drops to 1.7V, the G1 and G2 pins will be disabled. Once OUTEN goes below 1.2V, the LTC1552 will go into shutdown mode, cutting the supply current to a minimum. If thermal shutdown is not required, OUTEN can be connected to a conventional TTL enable signal. The free running 300kHz PWM frequency can be synchronized to a faster external clock connected to OUTEN. Adjusting the oscillator frequency can add flexibility in the external component selection. See the Clock Synchronization section.

Output regulation can be monitored with the PWRGD pin which in turn monitors the internal MIN and MAX comparators. If the output is ±5% beyond the rated value for more than 100µs, the PWRGD output will be pulled low. Once the output has settled within ±5% of the rated value for more than 300µs, PWRGD will return high.

## THEORY OF OPERATION

### Primary Feedback Loop

The LTC1552 senses the output voltage of the circuit at the output capacitor with the SENSE pin and feeds this voltage back to the internal transconductance error amplifier ERR. ERR compares the resistor-divided output voltage FB to the 1.265V reference and passes an error signal to the PWM comparator. A pulse width modulated signal is generated by comparing this error signal with a fixed frequency sawtooth waveform generated by the oscillator. This PWM signal controls the external MOSFETs through G1 and G2, closing the loop. Loop compensation is achieved with an external compensation network at the COMP pin, which is connected to the output node of the ERR transconductance amplifier.

### MIN, MAX Feedback Loops

Two additional comparators in the feedback loop provide high speed fault correction in situations where the ERR amplifier may not respond quickly enough. MIN compares the feedback signal FB to a voltage 60mV (5%) below the internal reference. If FB is lower than the threshold of this comparator, the MIN comparator overrides the ERR amplifier and forces the loop to full duty cycle, set by the internal oscillator at about 90%. Similarly, the MAX comparator forces the output to 0% duty cycle if FB is more than 5% above the internal reference. To prevent these two comparators from triggering due to noise, the MIN and MAX comparators' response times are deliberately controlled so that they take two or three cycles to respond. These two comparators help prevent extreme output perturbations with fast output transients, while allowing the main feedback loop to be optimally compensated for stability.

### Soft Start and Current Limit

The LTC1552 includes a soft start circuit which is used for initial start-up and during current limit operation. The SS pin requires an external capacitor to GND, with the value determined by the required soft start time. An internal 14µA current source is included to charge the external SS

## APPLICATIONS INFORMATION

capacitor. During start-up, the COMP pin is clamped to a diode drop above the voltage at the soft start pin. This prevents the error amplifier, ERR, from forcing the loop to maximum duty cycle. The LTC1552 will begin to operate at low duty cycle as the SS pin rises above about 1.2V ($V_{COMP}$ = 1.8V). As SS continues to rise, $Q_{SS}$ turns off and the error amplifier begins to regulate the output. The MIN comparator is disabled when soft start is active to prevent it from overriding the soft start function.

The LTC1552 includes yet another feedback loop to control operation in current limit. Just before every falling edge of G1, the current comparator, CC, samples-and-holds the voltage drop measured across the external MOSFET Q1 at the $I_{FB}$ pin. Note that when $V_{IN}$ = 12V, the $I_{FB}$ pin requires an external Zener to PGND to prevent voltage transients at the switching node between Q1 and Q2 from damaging internal structures. CC compares the voltage at $I_{FB}$ to the voltage at the $I_{MAX}$ pin. As the peak current rises, the measured voltage across Q1 increases, due to the drop across the $R_{DS(ON)}$ of Q1. When the voltage at $I_{FB}$ drops below $I_{MAX}$, indicating that Q1's drain current has exceeded the maximum level, CC starts to pull current out of the external soft start capacitor, cutting the duty cycle and controlling the output current level. The CC comparator pulls current out of the SS pin in proportion to the voltage difference between $I_{FB}$ and $I_{MAX}$. Under minor overload conditions, the SS pin will fall gradually, creating a time delay before current limit takes effect. Very short, mild overloads may not affect the output voltage at all. More significant overload conditions will allow the SS pin to reach a steady state and the output will remain at a reduced voltage until the overload is removed. Serious overloads will generate a large overdrive at CC, allowing it to pull SS down quickly and preventing damage to the output components.

By using the $R_{DS(ON)}$ of Q1 to measure the output current, the current limiting circuit eliminates the sense resistor that would otherwise be required. This helps minimize the number of components in the high current path. Note that the current limit circuitry is not designed to be highly accurate; it is meant to prevent damage to the power supply circuitry during fault conditions. The exact current level where the limiting circuit begins to take effect will vary from unit to unit as the $R_{DS(ON)}$ of Q1 varies.

For a given current limit level, the external resistor from $I_{MAX}$ to $V_{IN}$ can be determined by:

$$R_{IMAX} = \frac{(I_{LMAX})(R_{DS(ON)Q1})}{I_{IMAX}}$$

where:

$$I_{LMAX} = I_{LOAD} + \frac{I_{RIPPLE}}{2}$$

$I_{LOAD}$ = maximum load current

$I_{RIPPLE}$ = inductor ripple current

$$= \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

$f_{OSC}$ = LTC1552 oscillator frequency = 300kHz

$L_O$ = inductor value

$R_{DS(ON)Q1}$ = on resistance of Q1 at $I_{LMAX}$

$I_{IMAX}$ = internal 185$\mu$A sink current at $I_{MAX}$

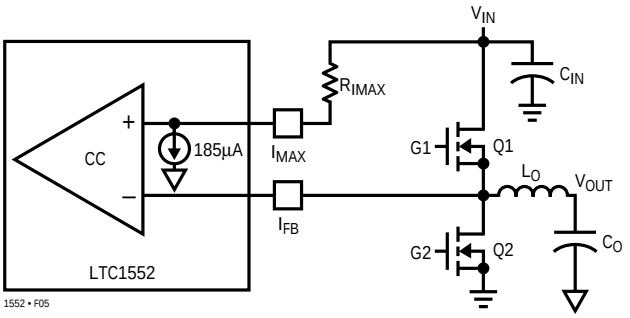



Figure 5. Current Limit Setting

### OUTEN and Thermistor Input

The LTC1552 includes a low power shutdown mode, controlled by the logic at the OUTEN pin. A high at OUTEN allows the part to operate normally. A low level at OUTEN stops all internal switching, pulls COMP and SS to ground internally and turns Q1 and Q2 off; $\overline{OT}$ and PWRGD are pulled low, and $\overline{FAULT}$ is left floating. In shutdown, the LTC1552 quiescent current will drop to about 150µA; this remaining current is used to keep the thermistor sensing circuit at OUTEN alive. Note that the leakage current of the external MOSFETs may add to the total shutdown current consumed by the circuit, especially at elevated temperature.

# APPLICATIONS INFORMATION

OUTEN is designed with multiple thresholds to allow it to also be utilized for over temperature protection. The power MOSFET operating temperature can be monitored with an external negative temperature coefficient (NTC) thermistor mounted next to the external MOSFET which is expected to run the hottest-usually the high side device, Q1. Electrically, the thermistor should form a voltage divider with another resistor, R1, connected to $V_{CC}$. Their midpoint should be connected to OUTEN (see Figure 6). As the temperature increases, the OUTEN pin voltage is reduced. Under normal operating conditions, the OUTEN pin should stay above 2V. All circuits will function normally, and $\overline{OT}$ will remain in a high state. If the temperature gets abnormally high, the OUTEN pin voltage will eventually drop below 2V. $\overline{OT}$ will switch to a logic low, providing an overtemperature warning to the system. As OUTEN drops below 1.7V, the LTC1552 disables both FET drivers. This shuts the FET driver supply down, preventing any further heating. If OUTEN is less than 1.2V, the LTC1552 will enter shutdown mode. To activate any of these three modes, the OUTEN voltage must drop below the respective threshold for longer than 30µs.

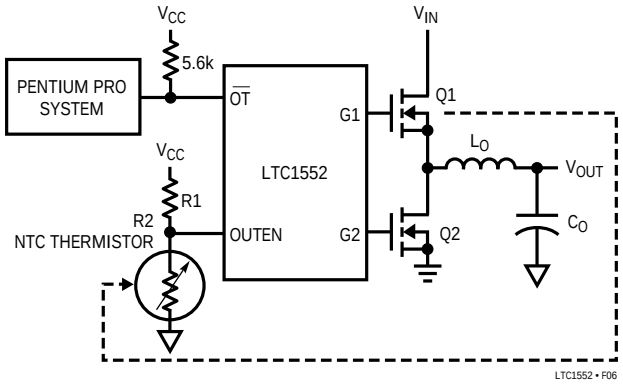



Figure 6. OUTEN Pin as a Thermistor Input

## Clock Synchronization

The internal oscillator can be synchronized to an external clock by applying the external clocking signal to the OUTEN pin. The synchronizing range extends from the internal 300kHz operating frequency up to 500kHz. If the external frequency is much higher than the natural free running frequency, the peak-to-peak sawtooth amplitude within the LTC1552 will decrease. Since the loop gain is inversely proportional to the amplitude of the sawtooth, the compensation network may need to be adjusted slightly. Note that the temperature sensing circuitry does not operate when external synchronization is used.

## MOSFET Gate Drive

Power for the internal MOSFET drivers is supplied by $PV_{CC}$. This supply must be above the input supply voltage by at least one power MOSFET $V_{GS(ON)}$ for efficient operation. This higher voltage can be supplied with a separate supply, or it can be generated using a simple charge pump as shown in Figure 7. The 90% maximum duty cycle ensures sufficient off-time to refresh the charge pump during each cycle. Figure 8 shows a tripling charge pump, which provides additional $V_{GS}$ overdrive to the external MOSFETs. This circuit can be useful for standard threshold MOSFETs which demand a higher turn-on voltage. An 18V Zener diode (1N5248B) is recommended with tripler charge pump designs to ensure that $PV_{CC}$ never exceeds the LTC1552's 20V absolute maximum $PV_{CC}$ voltage. This becomes more critical as $V_{IN}$ rises. With $V_{IN}$ = 12V, the doubler circuit of Figure 7 will also exceed the 20V limit. Figure 9 shows an alternate 17V charge pump derived from both the 5V and 12V supplies.

Upon power down, G1 and G2 will both be held low to prevent output voltage undershoot. On power-up or wake-up from thermal shutdown, the drivers are designed such that G2 will be held low until G1 first goes high.

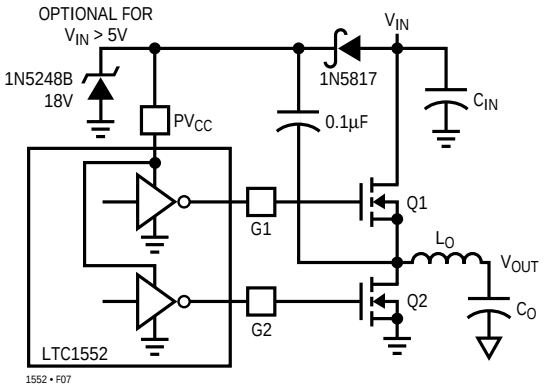



Figure 7. Doubling Charge Pump

## APPLICATIONS INFORMATION

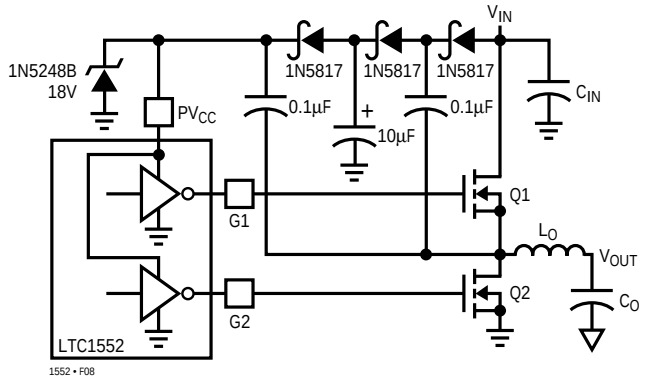



Figure 8. Tripling Charge Pump

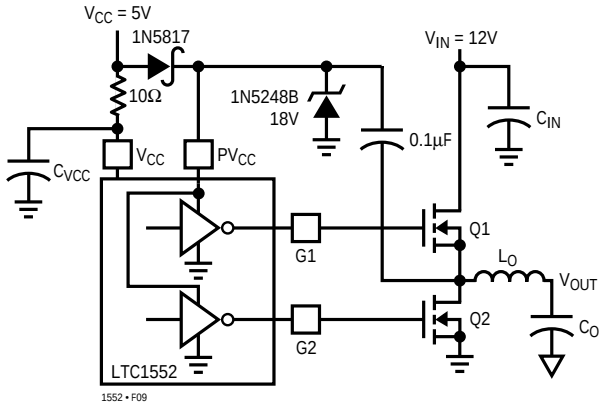



Figure 9. 17V Charge Pump for $V_{IN}$ = 12V

### Power MOSFETs

Two N-channel power MOSFETs are required for most LTC1552 circuits. They should be selected based primarily on threshold and on-resistance considerations. Thermal dissipation is often a secondary concern in high efficiency designs. The required MOSFET threshold should be determined based on the available power supply voltages and/or the complexity of the gate drive charge pump scheme. In 5V input designs where a 12V supply is used to power $PV_{CC}$, standard MOSFETs with $R_{DS(ON)}$ specified at $V_{GS}$ = 5V or 6V can be used with good results. The current drawn from the 12V supply varies with the MOSFETs used and the LTC1552 operating frequency, but is generally less than 50mA.

LTC1552 designs that use a 5V $V_{IN}$ voltage and a doubler charge pump to generate $PV_{CC}$ will not provide enough drive voltage to fully enhance standard power MOSFETs. Under this condition, the effective MOSFET $R_{DS(ON)}$ may be quite high, raising the dissipation in the FETs and reducing efficiency. Logic level FETs are a better choice for 5V–only systems or 12V input systems using the 17V charge pump of Figure 9. They can be fully enhanced with the generated charge pump voltage and will operate at maximum efficiency. Note that doubler charge pump designs running from supplies higher than 5V, and all tripler charge pump designs, should include a Zener clamp diode at $PV_{CC}$ to prevent transients from exceeding the absolute maximum rating at that pin. See the MOSFET Gate Drive section for more charge pump information.

Once the threshold voltage has been selected, $R_{DS(ON)}$ should be chosen based on input and output voltage, allowable power dissipation and maximum required output current. In a typical LTC1552 buck converter circuit operating in continuous mode, the average inductor current is equal to the output load current. This current is always flowing through either Q1 or Q2 with the power dissipation split up according to the duty cycle:

$$DC(Q1) = \frac{V_{OUT}}{V_{IN}}$$

$$DC(Q2) = 1 - \frac{V_{OUT}}{V_{IN}} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The $R_{DS(ON)}$ required for a given conduction loss can now be calculated by rearranging the relation $P = I^2R$.

$$R_{DS(ON)}(Q1) = \frac{P_{MAX}(Q1)}{[DC(Q1)](I_{MAX}^2)} = \frac{(V_{IN})[P_{MAX}(Q1)]}{(V_{OUT})(I_{MAX}^2)}$$

$$R_{DS(ON)}(Q2) = \frac{P_{MAX}(Q2)}{[DC(Q2)](I_{MAX}^2)} = \frac{(V_{IN})[P_{MAX}(Q2)]}{(V_{IN} - V_{OUT})(I_{MAX}^2)}$$

## APPLICATIONS INFORMATION

$P_{MAX}$ should be calculated based primarily on required efficiency. A typical high efficiency circuit designed for Pentium Pro with a 5V input and 3.1V, 11.2A output might allow no more than 3% efficiency loss at full load for each MOSFET. Assuming roughly 90% overall efficiency at this current level, this gives a $P_{MAX}$ value of [(3.1 • 11.2A/0.9)(0.03)] = 1.16W per FET and a required $R_{DS(ON)}$ of:

$$R_{DS(ON)}(Q1) = \frac{(5V)(1.16W)}{(3.1V)(11.2A^2)} = 0.015\Omega$$

$$R_{DS(ON)}(Q2) = \frac{(5V)(1.16W)}{(5V - 3.1V)(11.2A^2)} = 0.024\Omega$$

Note that the required $R_{DS(ON)}$ for Q2 is roughly twice that of Q1 in this example. This application might specify a single 0.024Ω device for Q2 and parallel two more of the same devices to form Q1. Note also that while the required $R_{DS(ON)}$ values suggest large MOSFETs, the dissipation numbers are only 1.16W per device or less—large TO-220 packages and heat sinks are not necessarily required in high efficiency applications. Siliconix Si4410DY or International Rectifier IRF7413 (both in SO-8) or Siliconix SUD50N03 or Motorola MTD20N03HDL (both in DPAK) are small footprint surface mount devices with $R_{DS(ON)}$ values below 0.03Ω at 5V of gate drive that work well in LTC1552 circuits. Note that using a higher $P_{MAX}$ value in the $R_{DS(ON)}$ calculations will generally decrease MOSFET cost and circuit efficiency and increase MOSFET heat sink requirements.

### Inductor Selection

The inductor is often the largest component in the LTC1552 design and should be chosen carefully. Inductor value and type should be chosen based on output slew rate requirements and expected peak current. Inductor value is primarily controlled by the required current slew rate. The maximum rate of rise of current in the inductor is set by its value, the input-to-output voltage differential and the maximum duty cycle of the LTC1552. In a typical 5V input, 3.1V output application, the maximum rise time will be:

$$(90\%)\frac{(V_{IN} - V_{OUT})(Amps)}{(L)(Second)} = \frac{1.71}{L}\frac{A}{\mu s}$$

where L is the inductor value in µH. With proper frequency compensation, the combination of the inductor and output capacitor will determine the transient recovery time. In general, a smaller value inductor will improve transient response at the expense of ripple and inductor core saturation rating. A 2µH inductor would have a 0.86A/µs rise time in this application, resulting in a 5.8µs delay in responding to a 5A load current step. During this 5.8µs, the difference between the inductor current and the output current must be made up by the output capacitor, causing a temporary voltage droop at the output. To minimize this effect, the inductor value should usually be in the 1µH to 5µH range for most typical 5V input LTC1552 circuits. Different combinations of input and output voltages and expected loads may require different values.

Once the required value is known, the inductor core type can be chosen based on peak current and efficiency requirements. Peak current in the inductor will be equal to the maximum output load current plus half of the peak-to-peak inductor ripple current. Ripple current is set by the inductor value, the input and output voltage and the operating frequency. If the efficiency is high, the ripple current is approximately equal to:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

$f_{OSC}$ = LTC1552 oscillator frequency

$L_O$ = inductor value

Solving this equation with our typical 5V to 3.1V application with a 2µH inductor, we get:

$$\frac{(1.9)(0.62)}{(300kHz)(2\mu H)} = 1.96A_{P-P}$$

Peak inductor current at 11.2A load:

$$11.2A + \frac{1.96A}{2} = 12.18A$$

## APPLICATIONS INFORMATION

The ripple current should generally be between 10% and 40% of the output current. The inductor must be able to withstand this peak current without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. Note that in non-current-limited circuits, the current in the inductor may rise above this maximum under short-circuit or fault conditions; the inductor should be sized accordingly to withstand this additional current. Inductors with gradual saturation characteristics are often the best choice.

### Input and Output Capacitors

A typical LTC1552 design puts significant demands on both the input and the output capacitors. During normal steady load operation, a buck converter like the LTC1552 draws square waves of current from the input supply at the switching frequency. The peak current value is equal to the output load current and the minimum value is near zero. Most of this current is supplied by the input bypass capacitor. The resulting RMS current flow in the input capacitor will heat it up, causing premature capacitor failure in extreme cases. Maximum RMS current occurs with 50% PWM duty cycle, giving an RMS current value equal to $I_{OUT}/2$. A low ESR input capacitor with an adequate ripple current rating must be used to ensure reliable operation. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours (three months) lifetime at rated temperature. Further derating of the input capacitor ripple current beyond the manufacturer's specification is recommended to extend the useful life of the circuit.

The output capacitor in a buck converter sees much less ripple current under steady-state conditions than the input capacitor. Peak-to-peak current is equal to that in the inductor, usually 10% to 40% of the total load current. Output capacitor duty places a premium not on power dissipation but on ESR. During an output load transient, the output capacitor must supply all of the additional load current demanded by the load until the LTC1552 can adjust the inductor current to the new value. ESR in the output capacitor results in a step in the output voltage equal to the ESR value multiplied by the change in load current. An 11A load step with a 0.05Ω ESR output capacitor will result in a 550mV output voltage shift; this is 18% of the output voltage for a 3.1V supply! Because of the strong relationship between output capacitor ESR and output load transient response, the output capacitor is usually chosen for ESR, not for capacitance value; a capacitor with suitable ESR will usually have a larger capacitance value than is needed to control steady-state output ripple.

Electrolytic capacitors rated for use in switching power supplies with specified ripple current ratings and ESR can be used effectively in LTC1552 applications. OS-CON electrolytic capacitors from Sanyo and other manufacturers give excellent performance and have a very high performance/size ratio for electrolytic capacitors. Surface mount applications can use either electrolytic or dry tantalum capacitors. Tantalum capacitors must be surge tested and specified for use in switching power supplies. Low cost, generic tantalums are know to have very short lives followed by explosive deaths in switching power supply applications. AVX TPS series surface mount devices are popular surge tested tantalum capacitors that work well in LTC1552 applications.

A common way to lower ESR and raise ripple current capability is to parallel several capacitors. A typical LTC1552 application might exhibit 5A input ripple current. Sanyo OS-CON part number 10SA220M (220µF/10V) capacitors feature 2.3A allowable ripple current at 85°C; three in parallel at the input (to withstand the input ripple current) will meet the above requirements. Similarly, AVX TPSE337M006R0100 (330µF/6V) have a rated maximum ESR of 100mΩ; seven in parallel will lower the net output capacitor ESR to 14mΩ.

### Feedback Loop Compensation

The LTC1552 voltage feedback loop is compensated at the COMP pin, attached to the output node of the internal $g_m$ error amplifier. The feedback loop can generally be compensated properly with an RC + C network from COMP to GND as shown in Figure 10.

Loop stability is affected by the inductor and output capacitor values and by other factors. Although a mathematical approach to frequency compensation can be used, the added complication of input and/or output

# APPLICATIONS INFORMATION

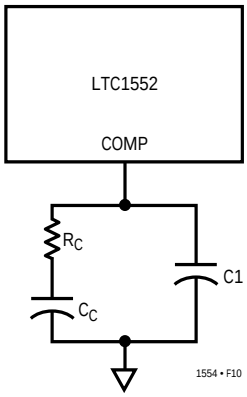



Figure 10. Compensation Pin Hook-Up

filters, unknown capacitor ESR, and gross operating point changes with input voltage, load current variations and frequency of operation, all suggest a more practical empirical method. This can be done by injecting a transient current at the load and using an RC network box to iterate toward the final compensation values, or by obtaining the optimum loop response using a network analyzer to find the actual loop poles and zeros.

Table 4 shows the suggested compensation components for 5V to 3.1V applications based on the inductor and output capacitor values. The values were calculated using multiple paralleled 330µF AVX TPS series surface mount tantalum capacitors as the output capacitor. The optimum component values might deviate from the suggested values slightly because of board layout and operating condition differences.

Table 4. Suggested Compensation Network for 5V to 3.1V Application Using Multiple 330µF AVX Output Capacitors

| $L_O$ (µH) | $C_O$(µF) | $R_C$(kΩ) | $C_C$(µF) | C1 (pF) |
|---|---|---|---|---|
| 1 | 990 | 2.7 | 0.01 | 330 |
| 1 | 1980 | 5.1 | 0.0047 | 180 |
| 1 | 4950 | 15 | 0.0018 | 68 |
| 1 | 9900 | 27 | 0.001 | 39 |
| 2.7 | 990 | 5.1 | 0.0047 | 180 |
| 2.7 | 1980 | 10 | 0.0022 | 100 |
| 2.7 | 4950 | 27 | 0.001 | 39 |
| 2.7 | 9900 | 51 | 470pF | 18 |
| 5.6 | 990 | 15 | 0.0018 | 68 |
| 5.6 | 1980 | 27 | 0.001 | 33 |
| 5.6 | 4950 | 68 | 330pF | 15 |
| 5.6 | 9900 | 150 | 180pF | 10 |

## VID0, VID1, VID2, VID3, PWRGD AND $\overline{FAULT}$

The digital inputs (VID0, VID1, VID2, VID3) program the internal DAC which in turn controls the output voltage. These digital input controls are intended to be static and are not designed for high speed switching. Forcing $V_{OUT}$ to step from a high to a low voltage suddenly by changing the VID*n* pins quickly can cause $\overline{FAULT}$ to trip.

Figure 11 shows the relationship between the $V_{OUT}$ voltage, PWRGD and $\overline{FAULT}$. To prevent PWRGD from interrupting the CPU unnecessarily, the LTC1552 has a built in $t_{PWRBAD}$ delay to prevent noise at the SENSE pin from toggling PWRGD. The internal time delay is designed to take about 100µs for PWRGD to go low and 300µs for it to recover. Once PWRGD goes low, the internal circuitry watches for the output voltage to exceed 115% of the rated voltage. If this happens, $\overline{FAULT}$ will be triggered. Once $\overline{FAULT}$ is triggered, G1 and G2 will be forced low immediately and the LTC1552 will remain in this state until $V_{CC}$ power supply is recycled or OUTEN is toggled.

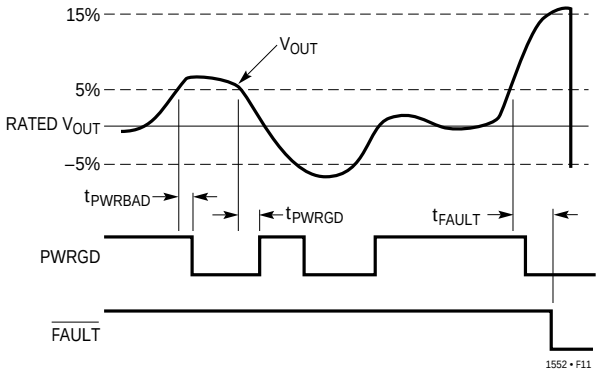



Figure 11. PWRGD and $\overline{FAULT}$

## LAYOUT CONSIDERATIONS

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1552. These items are also illustrated graphically in the layout diagram of Figure 12. The thicker lines show the high current paths. Note that at 10A current levels or above, current density in the PC board itself is a serious concern. Traces carrying high current should be as wide as possible. For example, a PCB fabricated with 2oz. copper requires a minimum trace width of 0.15" to carry 10A.

## APPLICATIONS INFORMATION

1. The signal and power grounds should be segregated. The LTC1552 signal ground must return to the (–) plate of the output capacitor, the negative terminal of SS and the COMP RC network. The power ground should return to the source of the lower MOSFET and the (–) plate of the $C_{IN}$ and the lead lengths should be as short as possible. The power ground and signal ground should be brought together at only one point, right at the LTC1552 GND and PGND pins. This helps to minimize internal ground disturbances in the LTC1552 and prevents differences in ground potential from disrupting internal circuit operation.
2. The $V_{CC}$ and $PV_{CC}$ decoupling capacitors should be as close to the LTC1552 as possible. The 10µF bypass capacitors shown at $V_{CC}$ and $PV_{CC}$ will help provide optimum regulation performance.
3. The (+) plate of $C_{IN}$ should be connected as close as possible to the drain of the upper MOSFET. An additional 1µF ceramic capacitor between $V_{IN}$ and power ground is recommended.
4. The SENSE pin is very sensitive to pickup from the switching node. Care should be taken to isolate SENSE from possible capacitive coupling to the inductor switching signal. A 0.1µF is required between the SENSE pin and the GND pin next to the LTC1552.
5. OUTEN is a high impedance input and should be externally pulled up to a logic HIGH for normal operation.

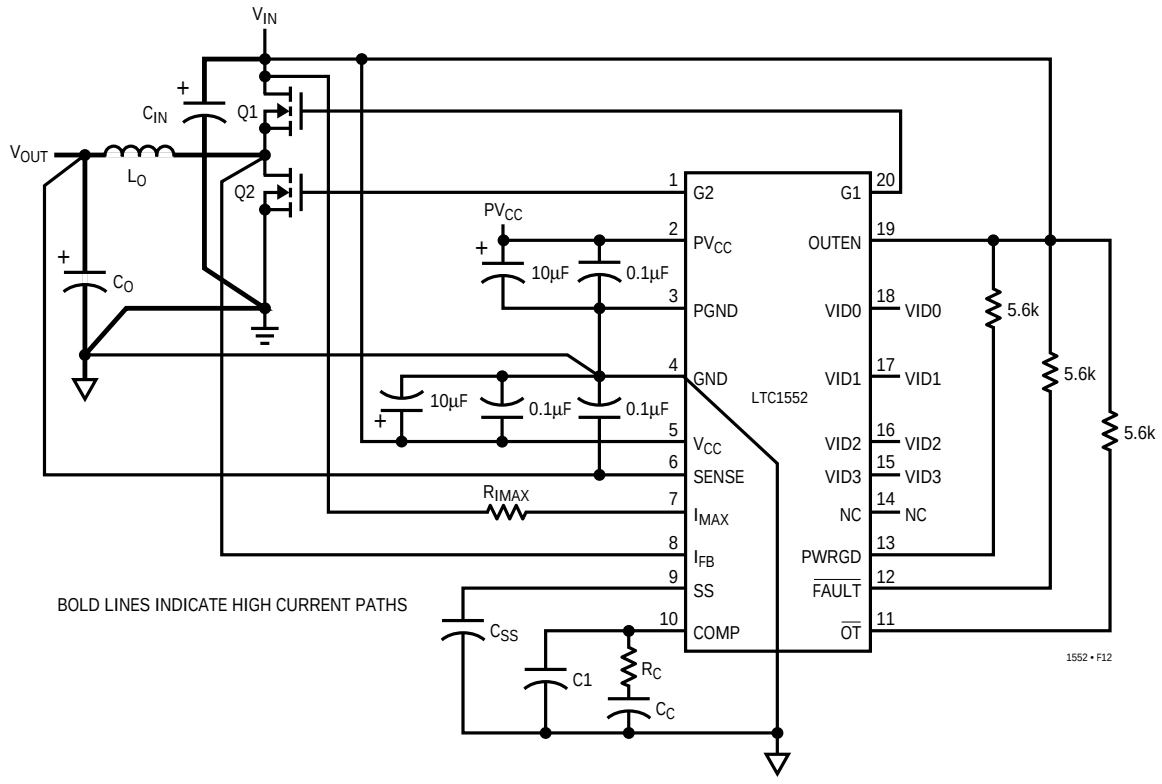



Figure 12. LTC1552 Layout Diagram

## TYPICAL APPLICATION

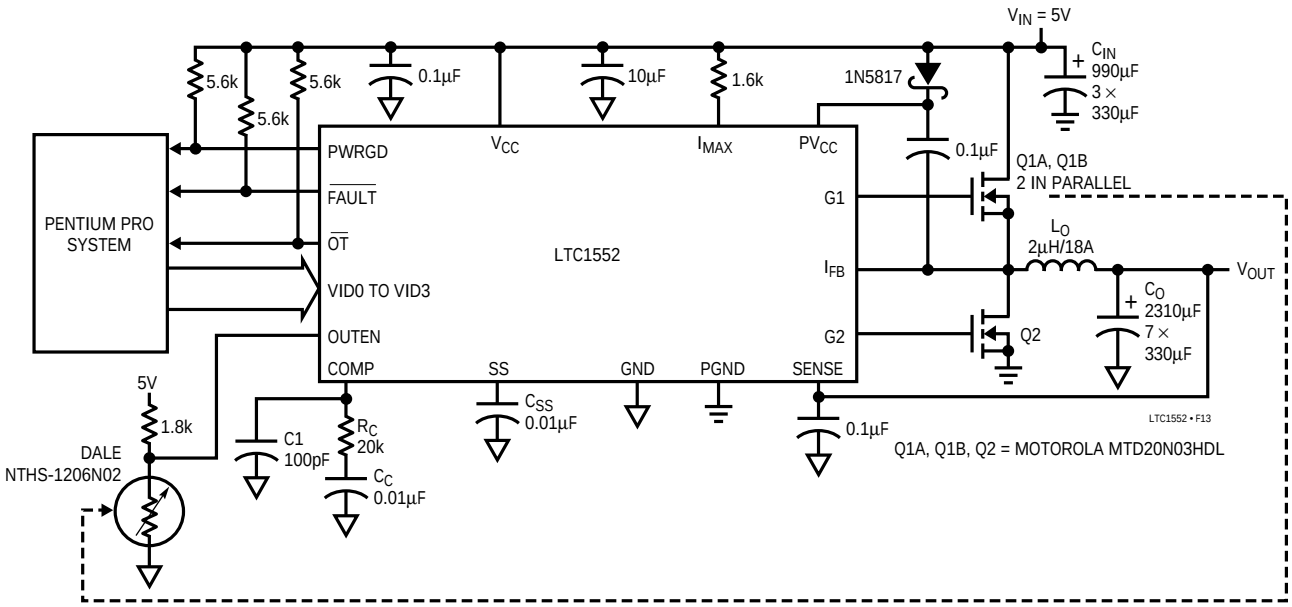
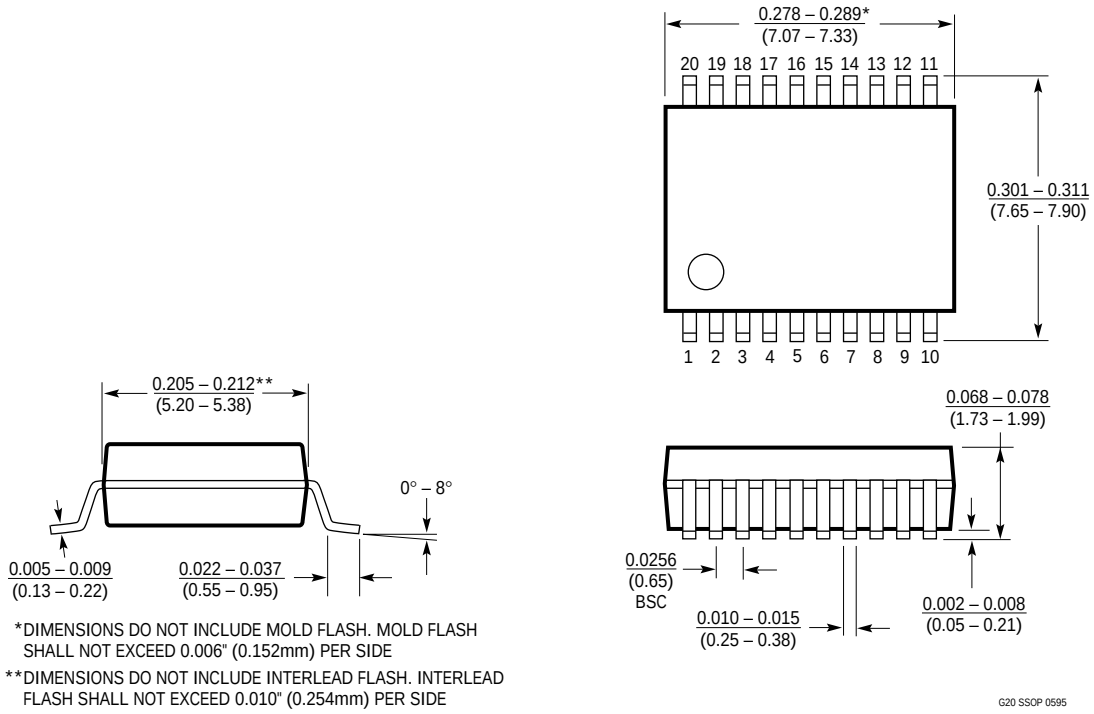



Figure 13. Single Supply 5V to 2.1V to 3.5V Application with Thermal Monitor

## PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
20-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)




*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

## TYPICAL APPLICATION

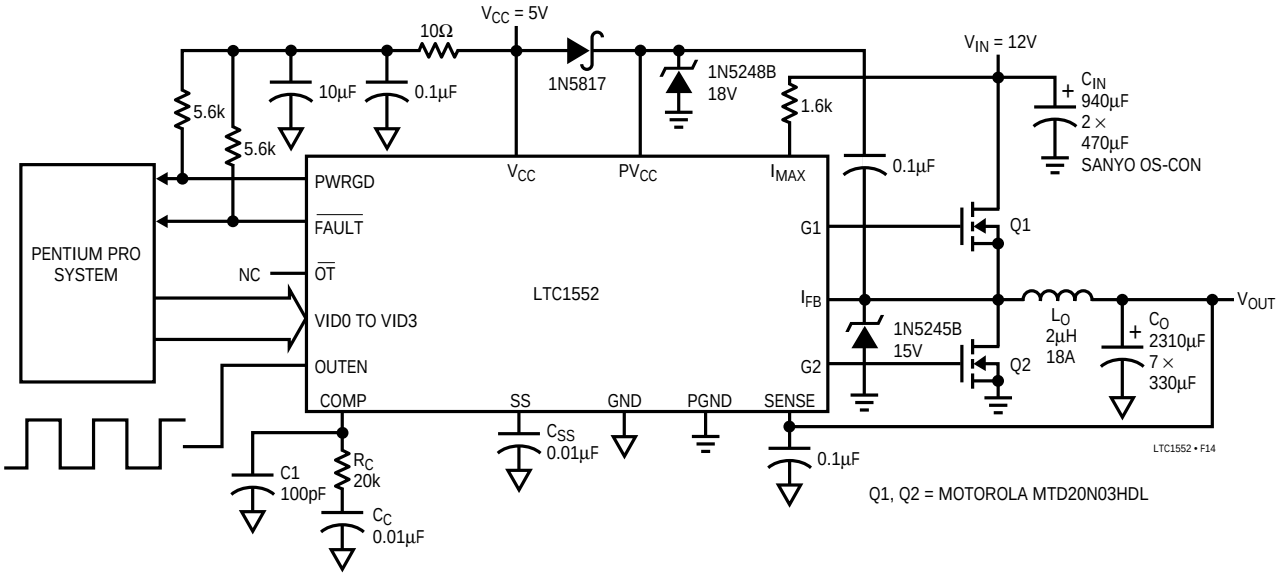



Figure 14. Synchronized 12V to 3.5V Application

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1142 | Current Mode Dual Step-Down Switching Regulator Controller | Dual Version of LTC1148 |
| LTC1148 | Current Mode Step-Down Switching Regulator Controller | Synchronous, $V_{IN} \leq 20V$ |
| LTC1149 | Current Mode Step-Down Switching Regulator Controller | Synchronous, $V_{IN} \leq 48V$, for Standard Threshold FETs |
| LTC1159 | Current Mode Step-Down Switching Regulator Controller | Synchronous, $V_{IN} \leq 40V$, for Logic Threshold FETs |
| LTC1266 | Current Mode Step-Up/-Down Switching Regulator Controller | Synchronous N- or P-Channel FETs, Comparator/Low-Battery Detector |
| LTC1430 | High Power Step-Down Switching Regulator Controller | Synchronous N-Channel FETs, Voltage Mode |
| LTC1435 | High Efficiency Low Noise Synchronous Stepdown Switching Regulator | Drive Synchronous N-Channel, $V_{IN} \leq 36V$ |
| LTC1438 | Dual High Efficiency Low Noise Synchronous Stepdown Switching Regulator | Dual LTC1435 with Power-On Reset |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