RP56LD, RP336LD, and RP144LD
Low Voltage V.90/K56flex™/V.34/V.32bis
Modem Data Pumps for Low Power Applications

Introduction

The CONEXANT™ RP56LD, RP336LD, and RP144LD Modem Data Pump (MDP) families support data/fax modem, voice coding/decoding, optional full-duplex speakerphone, and optional AudioSpan (Table 1). Low voltage and low power consumption support portable applications. Downloadable architecture allows upgrading of MDP code from the host/DTE.

In V.90/K56flex mode (RP56), the MDP can receive data at speeds up to 56 kbps from a digitally connected V.90- or K56flex-compatible central site modem. These MDPs take advantage of the PSTN which is primarily digital except for the client modem to central office local loop and are ideal for applications such as remote access to an Internet service provider (ISP), on-line service, or corporate site. The MDP can send upstream data at speeds up to V.34 rates.

In V.34 data mode (RP56 and RP336), the MDP can connect at the highest data rate the channel can support from 33.6 kbps to 2400 bps with auto-fallback to V.32bis.

In V.32 bis mode, the MDP can connect at the highest data rate the channel can support from 14.4 kbps to 4800 bps with optional auto-fallback to lower rate modulations.

Internal HDLC support eliminates the need for an external serial input/output (SIO) device in the DTE for products incorporating error correction and T.30 protocols.

Voice mode includes an Adaptive Differential Pulse Code Modulation (ADPCM) voice coder and decoder (codec). The codec compresses and decompresses voice signals for efficient digital storage of voice messages. The codec operates at 28.8k, 21.6k, or 14.4k bps (4-bit, 3-bit, or 2-bit quantization, respectively) with a 7.2 kHz or 8.0 kHz sample rate.

A voice pass-through mode allows the host to transmit and receive uncompressed voice samples in 16-bit linear form at 7.2 kHz, 8.0 kHz, or 11.025 kHz sample rate, or in 8-bit A-Law/µ-Law PCM form at 8.0 kHz sample rate.

SP models support position-independent full-duplex speakerphone (FDSP) operation using a dual internal integrated analog circuit to interface with the telephone line and the audio input/out (i.e., a headset, handset, or a microphone with external speaker).

SP models in 144-pin TQFP also support a 4-line voice serial interface used to transfer 16-bit linear or 8-bit A-Law/µ-Law PCM FDSP voice samples with acoustic echo cancellation to and from the host.

SP models also support AudioSpan (analog simultaneous audio/voice and data) operation at a data rate of 4.8 kbps.

The MDP operates over the public switched telephone network (PSTN) through the appropriate line termination.

Features

- Downloadable MDP code from the host/DTE
- 2-wire full-duplex
  - V.90 and K56flex (RP56 models)
  - V.34 (33.6 kbps) (RP56 and RP336 models)
  - V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21
  - Bell 212 and 103
- 2-wire half-duplex
  - V.34 fax, V.17, V.33, V.29, V.27 ter, and V.21 ch 2
  - Bell 208
  - Short train option in V.17 and V.27 ter
- Serial synchronous and asynchronous data
- Parallel synchronous and asynchronous data
- Parallel synchronous SDLC/HDLC support
- In-band secondary channel (V.34 and V.32 bis)
- Automatic mode selection (AMS)
- Automatic rate adaption (ARA)
- Digital near-end and far-end echo cancellation
- Bulk delay for satellite transmission
- ADPCM voice mode (7.2 kHz or 8.0 kHz)
- Voice pass-through mode (7.2 kHz, 8.0 kHz, or 11.025 kHz)
- Full-duplex speakerphone (SP models)
  - Acoustic and line echo cancellation
  - Programmable microphone AGC
  - Microphone volume selection and muting
  - Speaker volume control and muting; room monitor
- Voice serial data interface (144-pin TQFP, SP models)
  - 16-bit linear or 8-bit A-Law/µ-Law PCM voice samples
  - FDSP support with acoustic echo cancellation
- AudioSpan (SP models)
  - ITU-T V.61 modulation (4.8 kbps data plus audio)
  - Handset, headset, or half-duplex speakerphone
- TTL and CMOS compatible DTE interface
  - ITU-T V.24 (EIA/TIA-232-E) (data/control)
  - Microprocessor bus (data/configuration/control)
- Dynamic range: -9 dBm to -43 dBm
- Adjustable speaker output to monitor received signal
- DMA support interrupt lines
- Transmit and receive (16+128)-byte FIFO data buffers
- NRZI encoding/decoding
- 511 pattern generation/detection
- V.8 and V.8 bis signaling
- V.13 signaling
- Diagnostic capability
  - V.54 inter-DCE signaling
  - V.54 local analog and remote digital loopback
- +3.3V operation with +5V tolerant inputs
  - +5V or +3.3V analog signal interface
- Low power consumption:
  - Normal Mode = 260 mW; Sleep Mode = 40 mW
- Low profile, small footprint package
  - 100-pin PQFP or 144-pin TQFP
  - Meets PC Card Type II envelope requirements

Table 1. Modem Models and Functions

Modem/Part Number[1]		Package and Package Options			Supported Functions[2]				
Model Number	Part No.	Package	Clock/Crystal Input	Analog Interface Voltage	V.90/K56flex Data	V.34 Data	V.32 bis Data, V.34 Fax, Remote Voice	FDSP, AudioSpan	Voice Serial Interface
RP56LD/SP	R6764-21	100-Pin PQFP	Clock	+3.3V	Y	Y	Y	Y	–
RP56LD	R6764-24	100-Pin PQFP	Clock	+3.3V	Y	Y	Y	–	–
RP336LD/SP	R6764-26	100-Pin PQFP	Clock	+3.3V	–	Y	Y	Y	–
RP336LD	R6764-28	100-Pin PQFP	Clock	+3.3V	–	Y	Y	–	–
RP144LD/SP	R6764-22	100-Pin PQFP	Clock	+3.3V	–	–	Y	Y	–
RP144LD	R6764-29	100-Pin PQFP	Clock	+3.3V	–	–	Y	–	–
RP56LD/SP	R6785-21	144-Pin TQFP	Clock/Crystal	+3.3V/+5V	Y	Y	Y	Y	Y
RP56LD	R6785-24	144-Pin TQFP	Clock/Crystal	+3.3V/+5V	Y	Y	Y	–	–
RP336LD/SP	R6785-26	144-Pin TQFP	Clock/Crystal	+3.3V/+5V	–	Y	Y	Y	Y
RP336LD	R6785-28	144-Pin TQFP	Clock/Crystal	+3.3V/+5V	–	Y	Y	–	–

Notes:

1. Model/part number options:
   - L Low power
   - D Downloadable
   - SP Speakerphone.
2. Supported functions (Y = Supported; – = Not supported):
   - FDSP Full-duplex speakerphone
   - Remote Voice Remote voice record and playback
   - AudioSpan Analog simultaneous voice and data.

Technical Description

The MDP functional interface is illustrated in Figure 1.

Configurations and Rates

The selectable MDP configurations, signaling rates, and data rates are listed in Table 2.

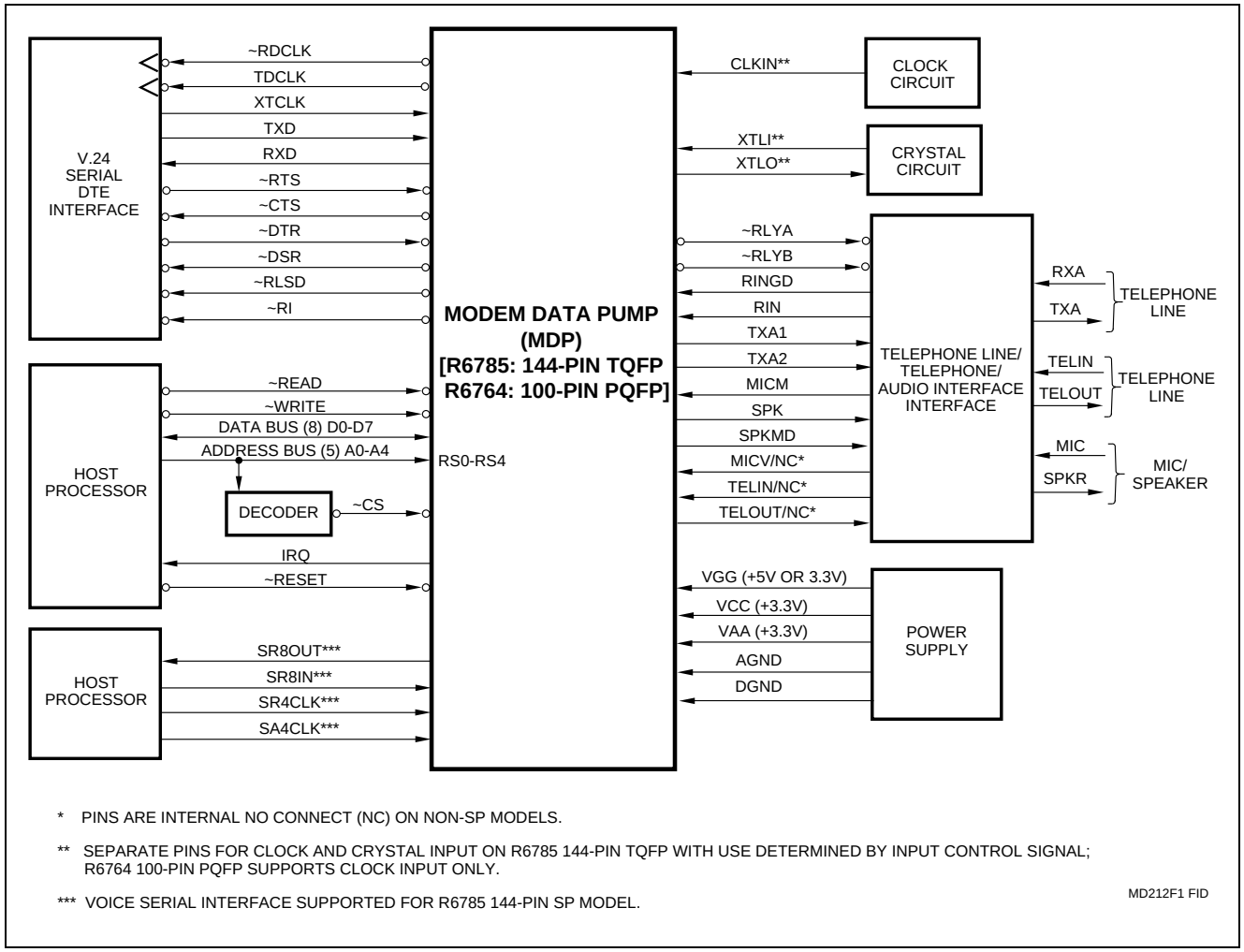

Figure 1. MDP Functional Interface

Table 2. Configurations, Signaling Rates, and Data Rates

Configuration	Modulation	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Symbol Rate (Symbols/Sec.)	Bits/Symbol - Data	Bits/Symbol - TCM	Constellation Points
V.90/K56flex PCM*	PCM	–	56000R/V.34ratesT[4]	8000	Dynamic	–	–
V.34 33600 TCM**	TCM	Note 2	33600	Note 2	Note 2	Note 2	Note 2
V.34 31200 TCM**	TCM	Note 2	31200	Note 2	Note 2	Note 2	Note 2
V.34 28800 TCM**	TCM	Note 2	28800	Note 2	Note 2	Note 2	Note 2
V.34 26400 TCM**	TCM	Note 2	26400	Note 2	Note 2	Note 2	Note 2
V.34 24000 TCM**	TCM	Note 2	24000	Note 2	Note 2	Note 2	Note 2
V.34 21600 TCM**	TCM	Note 2	21600	Note 2	Note 2	Note 2	Note 2
V.34 19200 TCM**	TCM	Note 2	19200	Note 2	Note 2	Note 2	Note 2
V.34 16800 TCM**	TCM	Note 2	16800	Note 2	Note 2	Note 2	Note 2
V.34 14400 TCM**	TCM	Note 2	14400	Note 2	Note 2	Note 2	Note 2
V.34 12000 TCM**	TCM	Note 2	12000	Note 2	Note 2	Note 2	Note 2
V.34 9600 TCM**	TCM	Note 2	9600	Note 2	Note 2	Note 2	Note 2
V.34 7200 TCM**	TCM	Note 2	7200	Note 2	Note 2	Note 2	Note 2
V.34 4800 TCM**	TCM	Note 2	4800	Note 2	Note 2	Note 2	Note 2
V.34 2400 TCM**	TCM	Note 2	2400	Note 2	Note 2	Note 2	Note 2
V.32 bis 14400 TCM	TCM	1800	14400	2400	6	1	128
V.32 bis 12000 TCM	TCM	1800	12000	2400	5	1	64
V.32 bis 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 bis 7200 TCM	TCM	1800	7200	2400	3	1	16
V.32 bis 4800	QAM	1800	4800	2400	2	0	4
V.32 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 9600	QAM	1800	9600	2400	4	0	16
V.32 4800	QAM	1800	4800	2400	2	0	4
V.22 bis 2400	QAM	1200/2400	2400	600	4	0	16
V.22 bis 1200	DPSK	1200/2400	1200	600	2	0	4
V.22 1200	DPSK	1200/2400	1200	600	2	0	4
V.22 600	DPSK	1200/2400	600	600	1	0	4
V.23 1200/75	FSK	1700/420	1200/75	1200	1	0	–
V.21	FSK	1080/1750	0–300	300	1	0	–
Bell 208 4800	DPSK	1800	4800	1600	3	0	8
Bell 212A	DPSK	1200/2400	1200	600	2	0	4
Bell 103	FSK	1170/2125	0–300	300	1	0	–
V.23 1200/75	FSK	1700/420	1200/75	1200	1	0	–
V.21	FSK	1080/1750	0–300	300	1	0	–
V.17 14400 TCM/V.33[3]	TCM	1800	14400	2400	6	1	128
V.17 12000 TCM/V.33[3]	TCM	1800	12000	2400	5	1	64
V.17 9600 TCM[3]	TCM	1800	9600	2400	4	1	32
V.17 7200 TCM[3]	TCM	1800	7200	2400	3	1	16
V.29 9600[3]	QAM	1700	9600	2400	4	0	16
V.29 7200[3]	QAM	1700	7200	2400	3	0	8
V.29 4800[3]	QAM	1700	4800	2400	2	0	4
V.27 4800[3]	DPSK	1800	4800	1600	3	0	8
V.27 2400[3]	DPSK	1800	2400	1200	2	0	4
V.21 Channel 2[3]	FSK	1750	300	300	1	0	–
Tone Transmit	–	–	–	–	–	–	–

Notes:

1. Modulation legend: TCM: Trellis-Coded Modulation; QAM: Quadrature Amplitude Modulation; FSK: Frequency Shift Keying; DPSK: Differential Phase Shift Keying

2. Adaptive; established during handshake:

	Carrier Frequency (Hz)	
Symbol Rate (Baud)	V.34 Low Carrier	V.34 High Carrier
2400	1600	1800
2800	1680	1867
3000	1800	2000
3200	1829	1920
3429	1959	1959

3. Models with fax support only.
4. Maximum data rate.
* RP56 models only.
** RP56 and RP336 models only.

Automatic Mode Selection

When automatic mode selection (AMS) is enabled, the MDP configures itself to the highest compatible data rate supported by the remote modem (AUTO bit). Automode operation is supported in V.90, K56flex, V.34, V.32 bis, V.32 V.22 bis, V.22, V.21, V.23, Bell 212A, and Bell 103 modes.

Automatic Rate Adaption (ARA)

In V.90, K56flex, V.34, and V.32 bis modes, automatic rate adaption (ARA) can be enabled to select the highest data rate possible based on the measured eye quality monitor (EQM) (EARC bit). This selection occurs during handshake/retrain and rate renegotiation.

Tone Generation

The MDP can generate single or dual voice-band tones from 0 Hz to 3600 Hz with a resolution of 0.15 Hz and an accuracy of ± 0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the MDP to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to ITU-T recommendations V.90, V.34, V.32 bis, V.32, V.17, V.33, V.29, V.27 ter, V.22 bis, V.22, V.23, or V.21, and is compatible with Bell 208, 212A, or 103, depending on the model and selected configuration.

RTS - CTS Response Time

The response times of CTS relative to a corresponding transition of RTS are listed in Table 3.

Transmit Level

The transmitter output level is selectable from -4 dBm to -19 dBm (VAA = +3.3V) or 0 dBm to -15 dBm (VAA = +5V) in 1 dB steps and is accurate to ±0.5 dB when used with an external hybrid. The output level can also be fine tuned by changing a gain constant in MDP DSP RAM. The maximum V.34/V.32 bis/V.32 transmit level for acceptable receive performance should not exceed -9 dBm.

Note: In V.34 mode, the transmit level may be automatically changed during the handshake. This automatic adjustment of the transmit level may be disabled via a parameter in DSP RAM.

Transmitter Timing

Transmitter timing is selectable between internal (±0.01%), external, or slave.

Scrambler/Descrambler

A self-synchronizing scrambler/descrambler is used in accordance with the selected configuration.

Answer Tone

When the NV25 bit is a zero, the MDP generates a 2100 Hz answer tone at the beginning of the answer handshake for 5.0 seconds (V.8) or 3.6 seconds (V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21). The answer tone has 180° phase reversals every 0.45 second to disable network echo cancellers (V.8, V.32 bis, V.32).

Table 3. RTS-CTS Response Times

Configuration	RTS-CTS Response[1]		Turn-Off Sequence[3]
	Constant Carrier	Controlled Carrier	
V.90, K56flex, V.34, V.32 bis, V.32	± 2 ms	N/A	N/A
V.33/V.17 Long	N/A	1393 ms[2]	15 ms[4]
V.33/V.17 Short	N/A	142 ms[2]	15 ms[4]
V.29	N/A	253 ms[2]	12 ms
V.27 4800 Long	N/A	708 ms[2]	7 ms[4]
V.27 4800 Short	N/A	50 ms[2]	7 ms[4]
V.27 2400 Long	N/A	943 ms[2]	10 ms[4]
V.27 2400 Short	N/A	67 ms[2]	10 ms[4]
V.22 bis, V.22, Bell 212A	± 2 ms	270 ms	N/A
V.21	500 ms	500 ms	N/A
V.23, Bell 103	210 ms	210 ms	N/A

Notes:

1. Times listed are CTS turn-on. The CTS OFF-to-ON response time is host programmable in DSP RAM. (Full-duplex modes only.)
2. Add echo protector tone duration plus 20 ms when echo protector tone is used during turn-on.
3. Turn-off sequence consists of transmission of remaining data and scrambled ones for controlled carrier operation. CTS turn-off is less than 2 ms for all configurations.
4. Plus 20 ms of no transmitted energy.
5. N/A = not applicable.

Receive Level

The MDP satisfies performance requirements for received line signal levels from –9 dBm to –43 dBm measured at the Receiver Analog (RXA) (TIP and RING) input (-15 dBm at RIN).

Note: A 6 dB pad is required between TIP and RING and the RIN input.

Receiver Timing

The timing recovery circuit can track a frequency error in the associated transmit timing source of ±0.035% (V.22 bis) or ±0.01% (other configurations).

Carrier Recovery

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier.

Clamping

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector (~RLSD) is off. ~RLSD can be clamped off (RLSDE bit).

Echo Canceller

A data echo canceller with near-end and far-end echo cancellation is included for 2-wire full-duplex V.34/V.32 bis/V.32 operation. The combined echo span of near and far cancellers can be up to 40 ms. The proportion allotted to each end is automatically determined by the MDP. The delay between near-end and far-end echoes can be up to 1.2 seconds.

V.90 and K56flex echo cancellation is also provided.

ADPCM Voice Mode

The Adaptive Differential Pulse Code Modulation (ADPCM) voice coder and decoder (codec) compresses and decompresses voice signals for efficient digital storage of voice messages. The codec operates at 28.8k, 21.6k, or 14.4k bps (4-bit, 3-bit, or 2-bit quantization, respectively) with a 7.2 kHz or 8.0 kHz sample rate.

Transmit Voice. 16-bit compressed transmit voice can be sent to the MDP ADPCM codec for decompression then to the digital-to-analog converter (DAC) by the host.

Receive Voice. 16-bit received voice samples from the MDP analog-to-digital converter (ADC) can be sent to the ADPCM codec for compression, and then be read by the host.

Voice Pass-Through Mode

Voice pass-through mode allows the host to transmit and receive uncompressed voice samples in 16-bit linear form at 7.2 kHz, 8.0 kHz, or 11.025 kHz sample rate, or in 8-bit A-Law/µ-Law PCM form at 8.0 kHz sample rate.

Transmit Voice. Transmit voice samples can be sent to the MDP DAC from the host.

Receive Voice. Received voice samples from the MDP ADC can be read by the host.

Speakerphone Voice/Audio Paths (SP Models)

The MDP incorporates a dual integrated analog interface. The voice/audio transmit and receive signals can be routed through several paths. The voice/audio paths are available in the speakerphone mode configuration and are selected through DSP RAM.

The voice/audio input can be taken from one of four different sources: telephone line input (RIN), handset (TELIN), microphone (MICM or MICV).

The speaker output (SPK) can originate from one of five different sources: RIN, TELIN, MICM or MICV or from the MDP's internal voice playback mode.

The voice/audio output may be routed to the telephone line output (TXA1 and TXA2) or handset (TELOUT).

The voice paths can be switched to allow an audio input to be routed to the telephone line output through a variable gain for applications such as music-on-hold.

The "room monitor" mode allows the MDP to receive audio from its surroundings and concurrently transmit the audio to a remote site.

Voice Serial Interface (SP models in 144-Pin TQFP)

A 4-pin serial interface supports the transfer of 16-bit linear or 8-bit A-Law/µ-Law PCM voice samples in full-duplex speakerphone form with acoustic echo cancellation to and from the host. These signals can be used in concurrent voice and data applications such as host-controlled DSVD by the host. Signals supported are Serial Data Output (S8OUT), Serial Data In (SR8IN), Serial Shift Clock (SR4CLK), and Sample Shift Clock (SA4CLK).

Analog voice on the MICV input pin is converted to 16-bit linear or 8-bit A-Law/µ-Law PCM digital voice samples and output on the SR8OUT pin to the host. Digital voice in 16-bit linear or 8-bit A-Law/µ-Law PCM form is received from the host on the SR8IN pin, converted to analog form and routed to the SPK output pin. SA4CLK provides the bit clock used to shift data bits in on the SR8IN pin and out on the SR8OUT pin. SR8CLK provides the frame clock used to synchronize words shifted in on the SR8IN pin and shifted out on the SR8OUT pin.

AudioSpan Mode (SP Models)

AudioSpan provides full-duplex analog simultaneous audio/voice and data over a single telephone line at a data rate with audio of 4800 bps using V.61 modulation. AudioSpan can send any type of audio waveform, including music. Data can be sent with or without error correction. The audio/voice interface can be in the form of a headset, handset, or a microphone and speaker (half-duplex speakerphone). Handset echo cancellation is provided.

Data Formats

Serial Synchronous Data

Data rate: 300-56000 bps (RP56), 300-33600 bps (RP56 and RP336), or 300-14400 bps, ±0.01%.

Selectable clock: Internal, external, or slave.

Serial Asynchronous Data

Data rate: 300-56000 bps (RP56), 300-33600 bps (RP56 and RP336), or 300-14400 bps, +1% (or +2.3%), -2.5%;

0-300 bps (V.21 and Bell 103);

1200/75 bps (V.23).

Bits per character: 7, 8, 9, 10, or 11.

Parallel Synchronous Data

Normal sync: 8-bit data for transmit and receive

Data rate: 300-56000 bps (RP56), 300-33600 bps (RP56 and RP336), or 300-14400 bps, ±0.01%.

SDLC/HDLC support:

Transmitter: Flag generation, 0 bit stuffing, CRC-16 or CRC-32 generation.

Receiver: Flag detection, 0 bit deletion, CRC-16 or CRC-32 checking.

Parallel Asynchronous Data

Data rate: 300-56000 bps (RP56), 300-33600 bps (RP56 and RP336), or 300-14400 bps, +1% (or 2.3%), -2.5%;

1200, 300, or 75 bps (FSK).

Data bits per character: 5, 6, 7, or 8.

Parity generation/checking: Odd, even, or 9th data bit.

Async/Sync and Sync/Async Conversion

An asynchronous-to-synchronous converter is provided in the transmitter and a synchronous-to-asynchronous converter is provided in the receiver. The converters operate in both serial and parallel modes. The asynchronous character format is 1 start bit, 5 to 8 data bits, an optional parity bit, and 1 or 2 stop bits. Valid character size, including all bits, is 7, 8, 9, 10, or 11 bits per character. Two ranges of signaling rates are provided:

- Basic range: +1% to –2.5%
- Extended overspeed range: +2.3% to –2.5%

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters. Break handling is performed as described in V.14.

Asynchronous characters are accepted on the TXD serial input and are issued on the RXD serial output.

V.54 Inter-DCE Signaling

The MDP supports V.54 inter-DCE signaling procedures in synchronous and asynchronous configurations. Transmission and detection of the preparatory, acknowledgment, and termination phases as defined in V.54 are provided. Three control bits in the transmitter allow the host to send the appropriate bit patterns (V54T, V54A, and V54P bits). Three control bits in the receiver are used to enable one of three bit pattern detectors (V54TE, V54AE, and V54PE bits). A status bit indicates when the selected pattern detector has found the corresponding bit pattern (V54DT bit).

V.13 Remote RTS Signaling

The MDP supports V.13 remote RTS signaling. Transmission and detection of signaling bit patterns in response to a change of state in the RTS bit or the ~RTS input signal are provided. The RRTSE bit enables V.13 signaling. The RTSDE bit enables detection of V.13 patterns. The RTSDT status bit indicates the state of the remote RTS signal. This feature may be used to clamp/unclamp the local ~RLSD and RXD signals in response to a change in the remote RTS signal in order to simulate controlled carrier operation in a constant carrier environment. The MDP automatically clamps and unclamps ~RLSD.

Dialing and Answering

The host can dial and answer using supported DTMF/pulse dialing and tone detection functions. The major parameters are host programmable.

Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path.

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This circuit is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The squarer may be disabled by the SQDIS bit causing tone detector C to be an eighth order filter. The tone detectors are disabled in data mode.

The tone detection sample rate is 9600 Hz in V.8 and V.34 modes and is 7200 Hz in non-V.34 modes. The default call progress filter coefficients are based on a 7200 Hz sampling rate and apply to non-V.34 modes only. The maximum detection bandwidth is equal to one-half the sample rate.

The default bandwidths and thresholds of the tone detectors are:

Tone Detector	Bandwidth	Turn-On Threshold	Turn-Off Threshold
A	245 – 650 Hz	–25 dBm	–31 dBm
B	360 – 440 Hz	–25 dBm	–31 dBm
C Prefilter	0 – 500 Hz	N/A	N/A
C	50 – 110 Hz	*	*

* Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the range –1 dBm to –26 dBm.

511 Pattern Generation/Detection

In synchronous mode, a 511 pattern can be generated and detected (control bit S511). Use of this bit pattern during self-test eliminates the need for external test equipment.

In-Band Secondary Channel

A full-duplex in-band secondary channel is provided in V.34 (all speeds) and V.32 bis/V.32 (7200 bps and above) modes. Control bit SECEN enables and disables the secondary channel operation. The secondary channel operates in parallel data mode with independent transmit and receive interrupts and data buffers. The main channel may operate in parallel or serial mode.

In V.34 modes, the secondary channel rate is 200 bps.

In V.32 bis/V.32 modes, the secondary channel rate is 150 bps. This rate is also host programmable in V.32 bis/V.32 modes.

Transmit and Receive FIFO Data Buffers

Two (16+128)-byte first-in first-out (FIFO) data buffers allow the DTE/host to rapidly output up to 144 bytes of transmit data and input up to 144 bytes of accumulated received data. The receiver FIFO is always enabled. The transmitter FIFO is enabled by the FIFOEN control bit. TXHF and RXHF bits operate off the lower 16 bits and indicate the corresponding FIFO buffer half full (8 or more

bytes loaded) status. TXFNF and RXFNE bits indicate the TXFIFO buffer not full and RXFIFO buffer not empty status, respectively. An interrupt mask register allows an interrupt request to be generated whenever the TXFNF, RXFNE, RXHF, or TXHF status bit changes state. The 128-byte FIFO extensions are enabled by default and can be disabled by clearing a bit in RAM.

DMA Support Interrupt Request Lines

DMA support is available in synchronous, asynchronous, and HDLC parallel data modes. Control bit DMAE enables and disables DMA support. When DMA support is enabled, the MDP ~RI and ~DSR lines are assigned to Transmitter Request (TXRQ) and Receiver Request (RXRQ) hardware output interrupt request lines, respectively. The TXRQ and RXRQ signals follow the assertion of the TDBE and RDBF interrupt bits thus allowing the DTE/host to respond immediately to the interrupt request without masking out status bits to determine the interrupt source.

NRZI Encoding/Decoding

NRZI data encoding/decoding may be selected in synchronous and HDLC modes instead of the default NRZ (control bit NRZIEN). In NRZ encoding, a 1 is represented by a high level and a 0 is represented by a low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

ITU-T CRC-32 Support

ITU-T CRC-32 generation/checking may be selected instead of the default ITU-T CRC-16 in HDLC mode using DSP RAM access.

Caller ID Demodulation

Caller ID information can be demodulated in V.23 1200 receive configuration and presented to the host/DTE in serial (RXD) and parallel (RBUFFER) form.

Telephone Line Interface

Line Transformer Interface. V.90/K56flex/V.34/V.32 bis/V.32 places high requirements upon the Data Access Arrangement (DAA) to the telephone line. Any non-linear distortion generated by the DAA in the transmit direction cannot be canceled by the MDP's echo canceller and interferes with data reception. The designer must, therefore, ensure that the total harmonic distortion seen at the RXA input to the MDP be at least 65 dB below the minimum level of received signal. Due to the wider bandwidth requirements in V.90, K56flex, and V.34, the DAA must maintain linearity from 10 Hz to 4000 Hz.

Relay Control. Direct control of the off-hook and talk/data relays is provided. Internal relay drivers allow direct connection to the off-hook (RLYA) and talk/data (RLYB) relays. The talk/data relay output can optionally be used for pulse dial.

Speaker Interface

An analog speaker output (SPK) is provided with on/off and volume control logic incorporated in the MDP. An external amplifier is recommended if driving non-amplified speakers.

A digital speaker output (SPKMD) is provided which reflects the received analog input signal digitized to TTL high or low level by an internal comparator to create a PC Card (PCMCIA)-compatible signal.

Additional Information

Additional information is provided in the RP56LD, RP336LD, and RP144LD Modem Designer's Guide (Order No. 1155).

Hardware Interface Signals

A functional interconnect diagram showing the typical MDP connection in a system is illustrated in Figure 2. Any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). An active low signal is indicated by a tilde preceding the signal name (e.g., ~RESET).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., ~RDCLK), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The 144-pin TQFP MDP hardware interface signals are shown Figure 2.

The 144-pin TQFP MDP signal pin assignments are shown Figure 3 and are listed in Table 4.

The 100-pin PQFP MDP hardware interface signals are shown Figure 4.

The 100-pin PQFP MDP signal pin assignments are shown Figure 5 and are listed in Table 5.

The MDP hardware interface signals are described in Table 6.

The digital interface characteristics are defined in Table 7.

The analog interface characteristics are defined Table 8.

The power requirements are defined in Table 9.

The absolute maximum ratings are defined in Table 10.

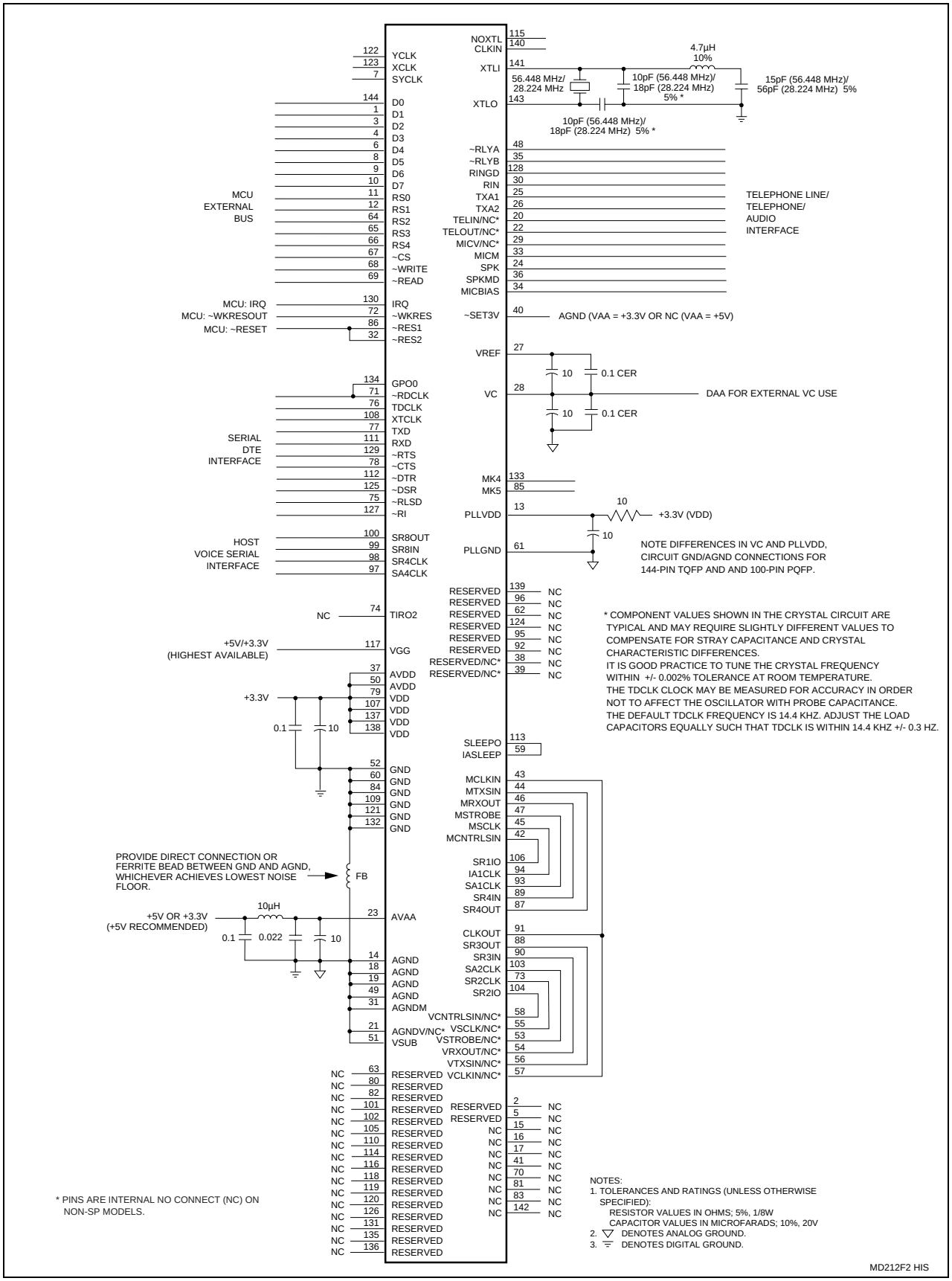

Figure 2. MDP Hardware Interface Signals-144-Pin TQFP

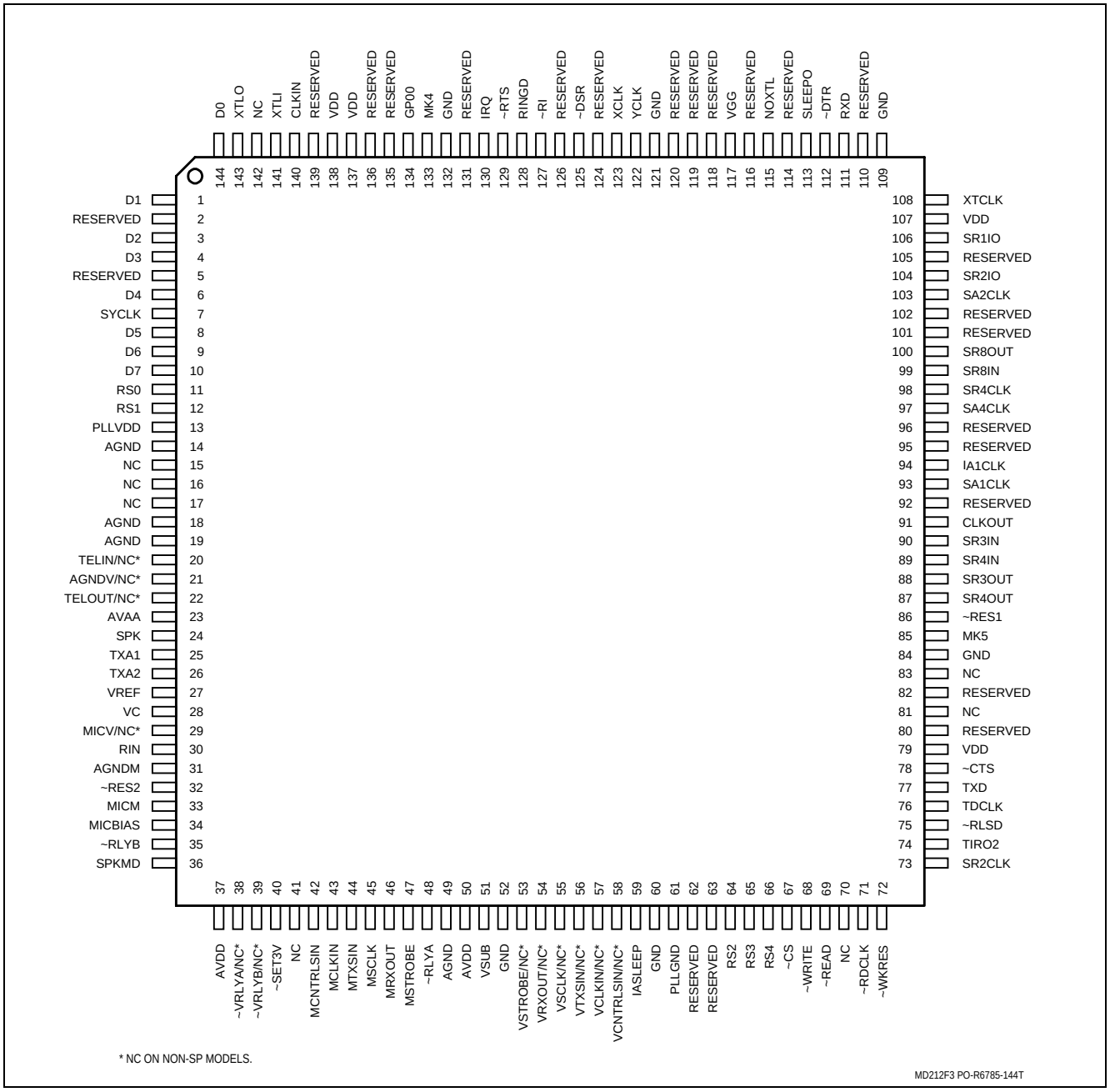

Figure 3. MDP Pin Signals - 144-Pin TQFP

Table 4. MDP Pin Signals - 144-Pin TQFP

Pin	Signal Label	I/O Type	Interface[3]	Pin	Signal Label	I/O Type	Interface
1	D1	IA/OB	Host Parallel Interface	73	SR2CLK	DI	To VSCLK (55)
2	RESERVED		NC	74	TIRO2	IA	NC
3	D2	IA/OB	Host Parallel Interface	75	~RLSD	OA	DTE Serial Interface
4	D3	IA/OB	Host Parallel Interface	76	TDCLK	OA	DTE Serial Interface
5	RESERVED		NC	77	TXD	IA	DTE Serial Interface
6	D4	IA/OB	Host Parallel Interface	78	~CTS	OA	DTE Serial Interface
7	SYCLK	OA	Controller	79	VDD	PWR	+3.3V
8	D5	IA/OB	Host Parallel Interface	80	RESERVED		NC
9	D6	IA/OB	Host Parallel Interface	81	NC		NC
10	D7	IA/OB	Host Parallel Interface	82	RESERVED		NC
11	RS0	IA	Host Parallel Interface	83	NC		NC
12	RS1	IA	Host Parallel Interface	84	GND	GND	DGND
13	PLLVDD	PLL	To +3.3 (VDD) through 10 Ω and to AGND though10 µF	85	MK5	IA	PLL Circuit Select (Note 4)
14	AGND	GND	AGND	86	~RES1		PIF: ~RESET SIF: Reset circuit
15	NC		NC	87	SR4OUT	DI	To MTXSIN (44)
16	NC		NC	88	SR3OUT	DI	To VTXSIN (56)
17	NC		NC	89	SR4IN	DI	To MRXOUT (46)
18	AGND	GND	AGND	90	SR3IN	DI	To VRXOUT (54)
19	AGND	GND	AGND	91	CLKOUT	DI	To MCLKIN (43) & VCLKIN (57)
20	TELIN/NC*	I(DA)	Line/Audio Interface	92	RESERVED		NC
21	AGNDV/NC*	GND	AGND	93	SA1CLK	DI	To MSTROBE (47)
22	TELOUT/NC*	O(DD)	Line/Audio Interface	94	IA1CLK	DI	To MSCLK (45)
23	AVAA	PWR	+3.3VA or +5VA	95	RESERVED		NC
24	SPK	O(DF)	Line/Audio Interface	96	RESERVED		NC
25	TXA1	O(DD)	Line/Audio Interface	97	SA4CLK	OA	Host Voice Serial Interface
26	TXA2	O(DD)	Line/Audio Interface	98	SR4CLK	OA	Host Voice Serial Interface
27	VREF	REF	VC through capacitors	99	SR8IN	IA	Host Voice Serial Interface
28	VC	REF	DAA; AGND thru capacitors	100	SR8OUT	OA	Host Voice Serial Interface
29	MICV/NC*	I(DA)	Line/Audio Interface	101	RESERVED		NC
30	RIN	I(DA)	Line/Audio Interface	102	RESERVED		NC
31	AGNDM	GND	AGND	103	SA2CLK	DI	To VSTROBE (53)
32	~RES2		PIF: ~RESET SIF: Reset circuit	104	SR2IO	DI	To VCNTRLSIN (58)
33	MICM	I(DA)	Line/Audio Interface	105	RESERVED		NC
34	MICBIAS		MICBIAS circuit	106	SR1IO	DI	To MCNTRLSIN (42)
35	~RLYB	OD	Line/Audio Interface	107	VDD	PWR	+3.3V
36	SPKMD	OA	Line/Audio Interface	108	XTCLK	IA	DTE Serial Interface
37	AVDD	PWR	+3.3V	109	GND	GND	DGND
38	RESERVED/NC*		NC	110	RESERVED		NC
39	RESERVED/NC*		NC	111	RXD	OA	DTE Serial Interface
40	~SET3V	IA	AGND (VAA = +3.3V) or NC (VAA = +5V)	112	~DTR	IA	DTE Serial Interface
41	NC		NC	113	SLEEPO	DI	To IASLEEP (59)
42	MCNTRLSIN	DI	To SR1IO (106)	114	RESERVED		NC
43	MCLKIN	DI	To CLKOUT (91)	115	NOXTL	IA	VCC or GND
44	MTXSIN	DI	To SR4OUT (87)	116	RESERVED		NC
45	MSCLK	DI	To IA1CLK (94)	117	VGG	REF	+5V or +3.3V
46	MRXOUT	DI	To SR4IN (89)	118	RESERVED		NC
47	MSTROBE	DI	To SA1CLK (93)	119	RESERVED		NC
48	~RLYA	OD	Line/Audio Interface	120	RESERVED		NC
49	AGND	GND	AGND	121	GND	GND	DGND
50	AVDD	PWR	+3.3V	122	YCLK	OA	NC
51	VSUB	GND	AGND	123	XCLK	OA	NC
52	GND	GND	DGND	124	RESERVED		NC
53	VSTROBE/NC*	DI	To SA2CLK (103)	125	~DSR	OA	DTE Serial Interface
54	VRXOUT/NC*	DI	To SR3IN (90)	126	RESERVED		NC
55	VSCLK/NC*	DI	To SR2CLK (73)	127	~RI	OA	DTE Serial Interface
56	VTXSIN/NC*	DI	To SR3OUT (88)	128	RINGD	IA	Line/Audio Interface
57	VCLKIN/NC*	DI	To CLKOUT (91)	129	~RTS	IA	DTE Serial Interface
58	VCNTRLSIN/NC*	DI	To SR2IO (104)	130	IRQ	IA	Host Parallel Interface
59	IASLEEP	DI	To SLEEPO (113)	131	RESERVED		NC
60	GND	GND	DGND	132	GND	GND	DGND

Table 4. MDP Pin Signals - 144-Pin TQFP (Cont'd)

Pin	Signal Label	I/O Type	Interface3	Pin	Signal Label	I/O Type	Interface
61	PLLGND	PLL	AGND	133	MK4	IA	PLL Circuit Select (Note 4)
62	RESERVED		NC	134	GP00	DI	To ~RDCLK (71)
63	RESERVED		NC	135	RESERVED		NC
64	RS2	IA	Host Parallel Interface	136	RESERVED		NC
65	RS3	IA	Host Parallel Interface	137	VDD	PWR	+3.3V
66	RS4	IA	Host Parallel Interface	138	VDD	PWR	+3.3V
67	~CS	IA	Host Parallel Interface	139	RESERVED		NC
68	~WRITE	IA	Host Parallel Interface	140	CLKIN	IA	Clock Circuit
69	~READ	IA	Host Parallel Interface	141	XTLI	I	Crystal Circuit
70	NC		NC	142	NC		NC
71	~RDCLK	OA	DTE Serial Interface	143	XTLO	O	Crystal Circuit
72	~WKRES	IA	MCU: READY/~WKRESOUT	144	D0	IA/OB	Host Parallel Interface

Notes:

1. I/O types:
   IA, IB = Digital input; OA, OB = Digital output.
   I(DA) = Analog input; O(DD), O(DF) = Analog output.
   DI = Device interconnect.
2. NC = No internal pin connection; RESERVED = No external connection allowed (may have internal connection).
3. Interface Legend:
   MDP = Modem Data Pump
   DTE = Data Terminal Equipment
   PIF = Parallel host interface
   SIF = Serial DTE interface.
4. An internal 55 kΩ pullup resistor is connected to this pin.

* NC on non-SP models.

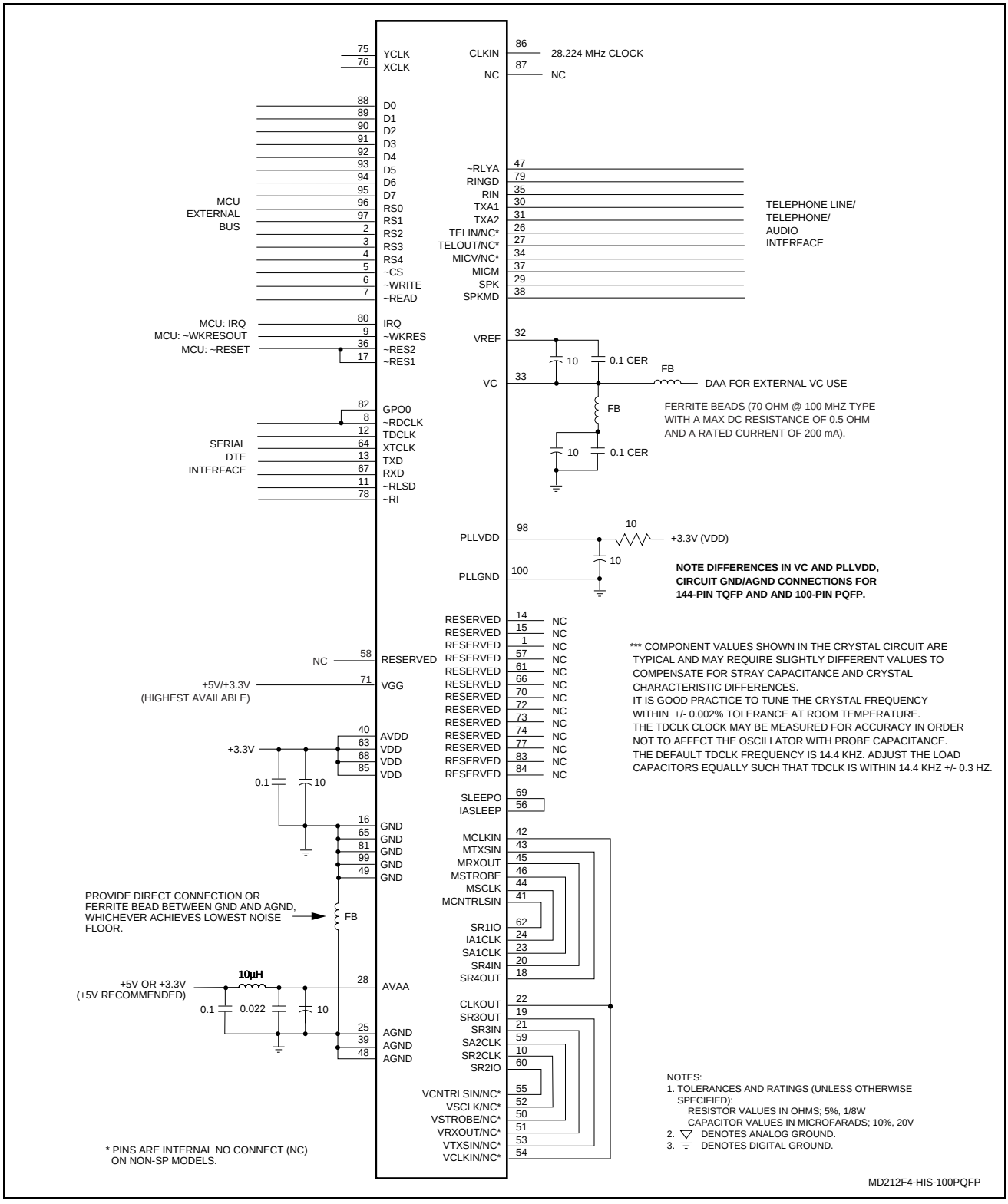

Figure 4. MDP Hardware Interface Signals-100-Pin PQFP

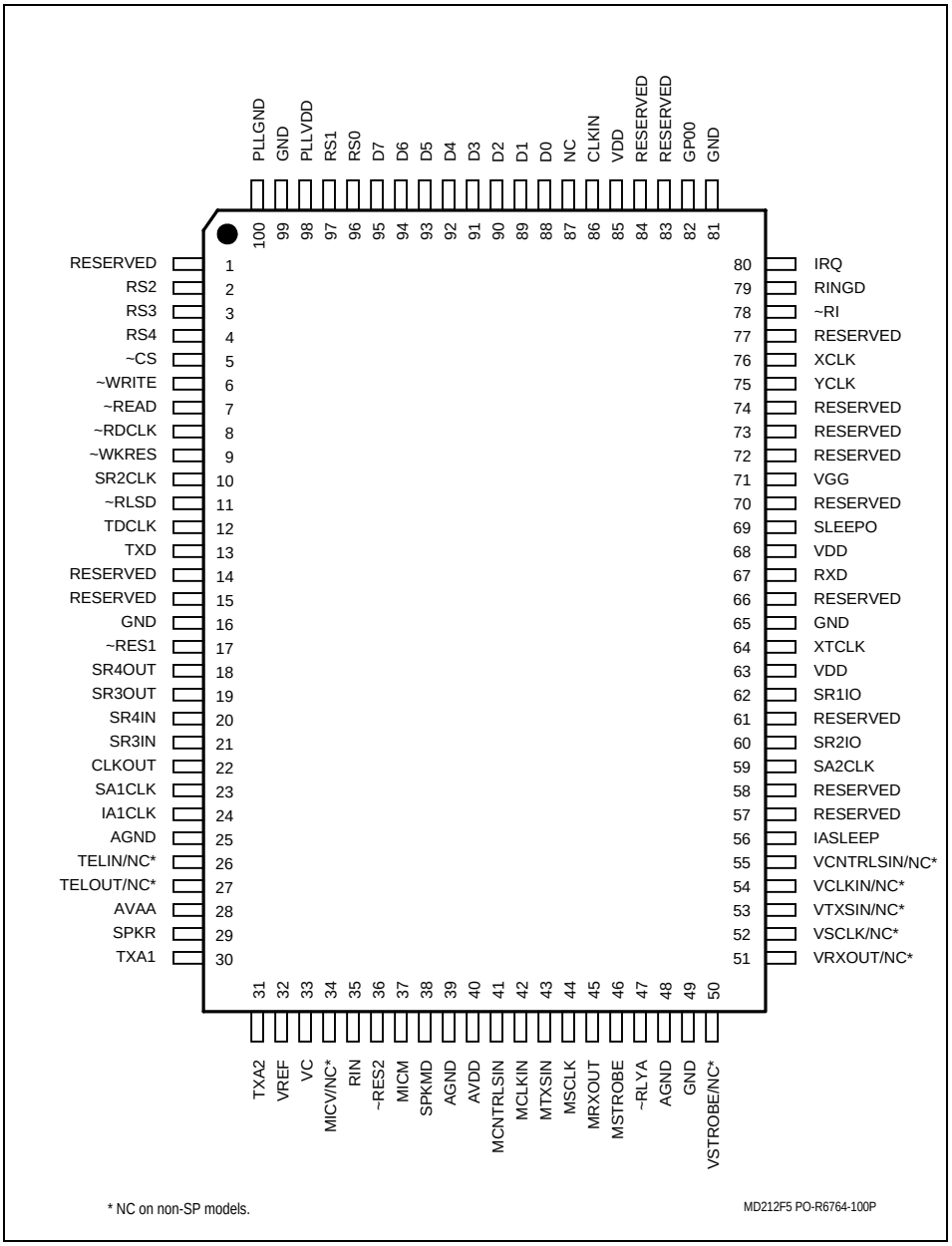

Figure 5. MDP Pin Signals - 100-Pin PQFP

Table 5. MDP Pin Signals - 100-Pin PQFP

Pin	Signal Label	I/O Type	Interface[3]	Pin	Signal Label	I/O Type	Interface
1	RESERVED		NC	51	VRXOUT/NC*	DI	To SR3IN (21)
2	RS2	IA	Host Parallel Interface	52	VSCLK/NC*	DI	To SR2CLK (10)
3	RS3	IA	Host Parallel Interface	53	VTXSIN/NC*	DI	To SR3OUT (19)
4	RS4	IA	Host Parallel Interface	54	VCLKIN/NC*	DI	To CLKOUT (22)
5	~CS	IA	Host Parallel Interface	55	VCNTRLSIN/NC*	DI	To SR2IO (60)
6	~WRITE	IA	Host Parallel Interface	56	IASLEEP	DI	To SLEEPO (69)
7	~READ	IA	Host Parallel Interface	57	RESERVED		NC
8	~RDCLK	OA	DTE Serial Interface	58	RESERVED		NC
9	~WKRES	IA	MCU: READY/~WKRESOUT	59	SA2CLK	DI	To VSTROBE (50)
10	SR2CLK	DI	To VSCLK (52)	60	SR2IO	DI	To VCNTRLSIN (55)
11	~RLSD	OA	DTE Serial Interface	61	RESERVED		NC
12	TDCLK	OA	DTE Serial Interface	62	SR1IO	DI	To MCNTRLSIN (41)
13	TXD	IA	DTE Serial Interface	63	VDD	PWR	+3.3V
14	RESERVED		NC	64	XTCLK	IA	DTE Serial Interface
15	RESERVED		NC	65	GND	GND	DGND
16	GND	GND	DGND	66	RESERVED		NC
17	~RES1		PIF: ~RESET SIF: Reset circuit	67	RXD	OA	DTE Serial Interface
18	SR4OUT	DI	To MTXSIN (43)	68	VDD	PWR	+3.3V
19	SR3OUT	DI	To VTXSIN (53)	69	SLEEPO	DI	To IASLEEP (56)
20	SR4IN	DI	To MRXOUT (45)	70	RESERVED		NC
21	SR3IN	DI	To VRXOUT (51)	71	VGG	REF	+5V or +3.3V
22	CLKOUT	DI	To MCLKIN (42) & VCLKIN (54)	72	RESERVED		NC
23	SA1CLK	DI	To MSTROBE (46)	73	RESERVED		NC
24	IA1CLK	DI	To MSCLK (44)	74	RESERVED		NC
25	AGND	GND	Analog Ground	75	YCLK	OA	NC
26	TELIN/NC*	I(DA)	Line/Audio Interface	76	XCLK	OA	NC
27	TELOUT/NC*	O(DD)	Line/Audio Interface	77	RESERVED		NC
28	AVAA	PWR	+3.3VA or +5VA	78	~RI	OA	DTE Serial Interface
29	SPK	O(DF)	Line/Audio Interface	79	RINGD	IA	Line/Audio Interface
30	TXA1	O(DD)	Line/Audio Interface	80	IRQ	IA	Host Parallel Interface
31	TXA2	O(DD)	Line/Audio Interface	81	GND	GND	DGND
32	VREF	REF	VC through capacitors	82	GP00	DI	To ~RDCLK (8)
33	VC	REF	DAA through FB; GND through capacitors and FB	83	RESERVED		NC
34	MICV/NC*	I(DA)	Line/Audio Interface	84	RESERVED		NC
35	RIN	I(DA)	Line/Audio Interface	85	VDD	PWR	+3.3V
36	~RES2		PIF: ~RESET SIF: Reset circuit	86	CLKIN	I	Clock Circuit
37	MICM	I(DA)	Line/Audio Interface	87	NC		NC
38	SPKMD	OA	Line/Audio Interface	88	D0	IA/OB	Host Parallel Interface
39	AGND	GND	Analog Ground	89	D1	IA/OB	Host Parallel Interface
40	AVDD	PWR	+3.3V	90	D2	IA/OB	Host Parallel Interface
41	MCNTRLSIN	DI	To SR1IO (62)	91	D3	IA/OB	Host Parallel Interface
42	MCLKIN	DI	To CLKOUT (22)	92	D4	IA/OB	Host Parallel Interface
43	MTXSIN	DI	To SR4OUT (18)	93	D5	IA/OB	Host Parallel Interface
44	MSCLK	DI	To IA1CLK (24)	94	D6	IA/OB	Host Parallel Interface
45	MRXOUT	DI	To SR4IN (20)	95	D7	IA/OB	Host Parallel Interface
46	MSTROBE	DI	To SA1CLK (23)	96	RS0	IA	Host Parallel Interface
47	~RLYA	OD	NC	97	RS1	IA	Host Parallel Interface
48	AGND	GND	AGND	98	PLLVDD	PLL	To +3.3 (VDD) through 10 Ω and to DGND through 10 µF.
49	GND	GND	DGND	99	GND	GND	DGND
50	VSTROBE/NC*	DI	To SA2CLK (59)	100	PLLGND	PLL	DGND

Notes:

1. I/O types:
   IA, IB = Digital input; OA, OB = Digital output.
   I(DA) = Analog input; O(DD), O(DF) = Analog output.
   DI = Device interconnect.
2. NC = No internal pin connection;
   RESERVED = No external connection allowed (may have internal connection).
3. Interface Legend:
   MDP = Modem Data Pump
   DTE = Data Terminal Equipment
   PIF = Parallel host interface
   SIF = Serial DTE interface.

* NC on non-SP models.

Table 6. MDP Signal Definitions

Label	I/O Type	Signal/Definition
OVERHEAD SIGNALS		
CLKIN	IA	**Clock In (144-Pin TQFP).** If external clock is selected (NOXTL = low), connect to an external 56.448 MHz or 28.224 MHz clock circuit. The clock frequency is selected by the MK4 and MK5 inputs.
XTLI	I	**Crystal In (144-Pin TQFP).** If external crystal is selected (NOXTL = high), connect to an external 56.448 MHz or 28.224 MHz crystal circuit. The clock frequency is selected by the MK4 and MK5 inputs.
XTLO	O	**Crystal Out (144-Pin TQFP).** If external crystal is selected (NOXTL = high), connect to the external crystal circuit return.
NOXTL	IA	**No Crystal Circuit (144-Pin TQFP).** Selects external crystal (NOXTL = high, i.e., leave open or connect to VDD through 10kΩ) or clock (NOXTL = low, i.e., connect to GND) circuit. Internal pull-up provided.
XTLI/CLKIN	I	**Crystal In/Clock In (100-Pin PQFP).** Connect to an external 56.448 MHz/28.224 MHz crystal circuit (crystal input option) or to an external 56.448 MHz/28.224 MHz clock circuit (clock input option).
XTLO/NC	O	**Crystal Out/NC (100-Pin PQFP).** Connect to the external crystal circuit return (crystal input option) or leave open (clock input option).
~RES1, ~RES2	IA	**Reset.** ~RESET low holds the MDP in the reset state. ~RESET going high releases the MDP from the reset state and initiates normal operation using power turn-on (default) values. ~RESET must be held low for at least 3 µs. The MDP is ready to use 400 ms after the low-to-high transition of ~RESET. ~RES1 and ~RES2 are typically connected to the MCU ~RESET input and to the host bus ~RESET (or RESET through an inverter) line (parallel host) or reset circuit (serial DTE interface) which resets both the MCU and MDP upon power turn-on. ~RES1 and ~RES2 have active internal pull-up resistors.
~WKRES	IA	**Wake-up Reset.** ~WKRES is connected internally to ~RESET but will not drive the MDP ~RESET pins. Asserting ~WKRES performs the same reset function as the MDP ~RESET and typically used by the MCU to wake up the MDP from SLEEP Mode when the MDP ~RESET lines cannot be asserted (because they are also connected to the MCU ~RESET input). For a serial DTE or parallel host MCU configuration, connect ~WKRES to the MCU ~WKRESOUT output. ~WKRES has an active internal pull-up resistor.
VDD	PWR	**+3.3V Digital Circuit Power Supply.** Connect to +3.3V through digital circuit power supply filter.
AVDD	PWR	**+3.3V Analog Circuit Digital Power Supply.** Connect to +3.3V through digital circuit power supply filter.
AVAA	PWR	**Analog Circuit Analog Power Supply.** Connect to +3.3V or +5V (preferred) through analog circuit power supply filter. **Note:** When operating the analog circuitry at +3.3V, the transmit level is 4 dB lower and the converted receive level is 4 dB higher when compared to operating the analog circuitry at +5V. The transmit level must be adjusted accordingly using TLVL or other means.
VGG	REF	**Input Reference Voltage.** Reference voltage for +5V tolerant input pins. Connect to the highest of +3.3V or +5V available on the circuit board. A connection to +5V allows +5V or +3.3V input levels. A connection to +3.3V allows +3.3V input levels only.
GND	GND	**Digital Ground.** Connect to digital ground.
AGND	GND	**Analog Ground.** Connect to analog ground.
XCLK	OA	**X Clock.** Output clock at 56.448 MHz (PLL disabled) or 63.5045 (PLL enabled), which runs during MDP Normal Mode and is turned off during Sleep Mode.
YCLK	OA	**Y Clock.** Output clock at 28.224 MHz, which runs during MDP Normal Mode and is turned off during Sleep Mode.
SYCLK	OA	**System Clock.** Output clock at 28.224 MHz, which runs during MDP Normal Mode and during Sleep Mode.
PLLVDD	PLL	**PLLVDD Connection.** For the 144-pin TQFP, connect to +3.3V (VDD) through 10 Ω and to AGND through 10 (+) µF, For the 100-pin PQFP, connect to +3.3V (VDD) through 10 Ω and to DGND through 10 (+) µF.
PLLGND	PLL	**PLLGND Connection.** For the 144-pin TQFP, connect to AGND. For the 100-pin PQFP, connect to DGND.
~SET3V	IA	**Set Integrated Analog +3.3V Reference.** Selects analog circuit voltage reference: High (NC) = +5V, low (AGND) = +3.3V.

Table 6. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
OVERHEAD SIGNALS (CONTINUED)		
MK4	IA	**PLL Circuit Enable/Disable (144-Pin TQFP).** This pin disables (MK4 = high) or enables (MK4 = low, recommended setting) the internal PLL circuit. Connect this pin to GND to enable the PLL circuit. Internal pull-up provided. MK4 must be low if using the 28.224 MHz option. See MK5. Note: The 100-pin PQFP is internally bonded to enable the internal PLL.
MK5	IA	**PLL Circuit Frequency Select (144-Pin TQFP).** This pin selects the input frequency (MK5 high = 28.224 MHz, MK5 low = 56.448 MHz) when the internal PLL circuit is enabled (MK4 = low). If the PLL is disabled (MK4 = high), leave MK5 high and use 56.448 MHz. Internal pull-up provided. See MK4. If 28.224 MHz input frequency is used, MK4 must be low and MK5 must be high. **Note:** The 100-pin PQFP is internally bonded to select a 28.224 MHz input frequency. **MK4 / MK5 / PLL Enabled / Crystal/Clock** 0 / 0 / Yes / 56.448 MHz 0 / 1 / Yes / 28.224 MHz (Most common) 1 / 0 / No / Invalid Option 1 / 1 / No / 56.448 MHz
PARALLEL HOST INTERFACE		
Address, data, control, and interrupt hardware interface signals allow MDP connection to an 8086-compatible microprocessor bus. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000. The microprocessor interface allows a microprocessor to change MDP configuration, read or write channel and diagnostic data, and supervise MDP operation by writing control bits and reading status bits.		
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the MDP. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals.
RS0–RS4	IA	**Register Select Lines.** The five active high register select lines (RS0–RS4) address internal MDP interface memory registers and are typically connected to the five least significant lines (A0–A4) of the address bus. The MDP decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4, while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7). The most significant data bit is D7, while the least significant data bit is D0.
~CS	IA	**Chip Select.** ~CS selects the MDP for microprocessor bus operation. ~CS is typically generated by decoding host address bus lines.
~READ	IA	**Read Enable.** During a read cycle (~READ asserted), data from the selected interface memory register is gated onto the data bus by means of three-state drivers in the MDP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.
~WRITE	IA	**Write Enable.** During a write cycle (~WRITE asserted), data from the data bus is copied into the selected MDP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
IRQ	OA	I**nterrupt Request.** The MDP IRQ output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate MDP service. The IRQ output can be enabled in the MDP interface memory to indicate immediate change of conditions. The use of IRQ is optional depending upon MDP application. The IRQ output is driven by a TTL-compatible CMOS driver.
VOICE SERIAL INTERFACE (144-PIN R6785; SP MODEL)		
Timing and data signals provide a voice serial interface which is used to transfer 16-bit linear or 8-bit A-Law/µ-Law PCM voice samples in full-duplex speakerphone form with acoustic echo cancellation to and from the host. These signals can be used in concurrent voice and data applications by the host. In non-SP models, voice samples are not supported on these pins and these pins should be left open.		
SR8OUT	OA	**Serial Data Out.** Analog voice on the MICV input pin is converted to 16-bit linear or 8-bit A-Law/µ-Law PCM digital voice samples and output on this pin in serial form to the host.
SR8IN	IN	**Serial Data In.** Digital voice in 16-bit linear or 8-bit A-Law/µ-Law PCM form is received from the host on this serial data input pin, converted to analog form and routed to the SPKR output pin.
SR4CLK	IA	**Serial Shift Clock.** Serial bit clock used to shift data bits into the MDP on the SR8IN pin and out of the MDP on the SR8OUT pin. Connect to MDP CLKOUT (PB0) pin.
SA4CLK	IA	**Sample Shift Clock.** Serial frame clock used to synchronize words shifted in on the SR8IN pin and shifted out on the SR8OUT pin. SA4CLK clock edges must align with the rising edge of SR4CLK.

Table 6. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
DTE SERIAL INTERFACE		
Timing, data, control, and status signals provide a V.24-compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within a printed circuit board, stand-alone modem enclosures, or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA/RS-232-D voltage levels.		
TXD	IA	**Transmitted Data.** The MDP obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.
RXD	OA	**Received Data.** The MDP presents received serial data to the local DTE on the Received Data (RXD) output.
~RTS	IA	**Request to Send.** Activating ~RTS causes the MDP to transmit data on TXD when ~CTS becomes active. The ~RTS pin is logically ORed with the RTS bit.
~CTS	OA	**Clear To Send.** ~CTS active indicates to the local DTE that the MDP will transmit any data present on TXD. CTS response times from an active condition of RTS are shown in Table 3.
~RLSD	OA	**Received Line Signal Detector.** ~RLSD active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence. One of four ~RLSD receive level threshold options can be selected (RTH bits). A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than -43 dBm. The ~RLSD on and off thresholds are host programmable in DSP RAM.
~DTR	IA	**Data Terminal Ready.** In V.8, V.90, K56flex, V.34, V.32 bis, V.32, V.22 bis, V.22, or Bell 212A configuration, activating ~DTR initiates the handshake sequence. The DATA bit must be set to complete the handshake. In V.21, V.23, or Bell 103 configuration, activating ~DTR causes the MDP to enter the data state provided that the DATA bit is a 1. If in answer mode, the MDP immediately sends answer tone. In these modes, if controlled carrier is enabled, carrier is controlled by RTS. During the data mode, deactivating ~DTR causes the transmitter and receiver to turn off and return to the idle state. The ~DTR input and the DTR control bit are logically ORed.
~DSR	OA	**Data Set Ready.** ~DSR ON indicates that the MDP is in the data transfer state. ~DSR OFF indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator (~RI). ~DSR is OFF when the MDP is in a test mode (i.e., local analog or remote digital loopback). The DSR status bit reflects the state of the ~DSR output.
~RI	OA	**Ring Indicator.** ~RI output follows the ringing signal present on the line with a low level (0 V) during the ON time, and a high level during the OFF time coincident with the ringing signal. The RI status bit reflects the state of the ~RI output.
TDCLK	OA	**Transmit Data Clock.** The MDP outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50±1%. The TDCLK source can be internal, external (input on XTCLK), or slave (to ~RDCLK) as selected by TXCLK bits in interface memory.
XTCLK	IA	**External Transmit Clock.** In synchronous communication, an external transmit data clock can be connected to the MDP XTCLK input. The clock supplied at XTCLK must exhibit the same characteristics as TDCLK. The XTCLK input is then reflected at the TDCLK output.
~RDCLK	OA	**Receive Data Clock.** The MDP outputs a synchronous Receive Data Clock (~RDCLK) for USRT timing. The ~RDCLK frequency is the data rate (±0.01%) with a duty cycle of 50±1%. The ~RDCLK low-to-high transitions coincide with the center of the received data bits.

Table 6. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
TELEPHONE LINE/TELEPHONE/AUDIO INTERFACE SIGNALS AND REFERENCE VOLTAGE		
TXA1, TXA2	O(DF)	**Transmit Analog 1 and 2 Output.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 Ω load. Typically, TXA1 and TXA2 are connected to the telephone line interface or an optional external hybrid circuit.
RIN	I(DA)	**Receive Analog Input.** RIN is a single-ended input with 70K Ω input impedance. Typically, RIN is connected to telephone line interface or an optional external hybrid circuit. **NOTE: If not used, do not tie directly to ground; this input has a bias voltage of +1.35V (VAA = +3.3V) or +2.5V (VAA = +5V).**
RINGD	IA	**Ring Detect.** The RINGD input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving RINGD should be a 4N35 optoisolator or equivalent. The circuit driving RINGD should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. Detected ring signals are reflected on the ~RI output signal as well as the RI bit.
~RLYA (~OHRC, ~CALLID)	OD	**Relay A Control.** The ~RLYA open drain output can directly drive a reed relay coil with a minimum resistance of 360 ohms (9.2 mA max. @ +3.3V). A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). ~RLYA is controlled by host setting/resetting of the RA bit. In a typical application, ~RLYA is connected to the normally open Off-Hook relay (~OHRC). In this case, ~RLYA active closes the relay to connect the MDP to the telephone line. Alternatively, in a typical application, ~RLYA is connected to the normally open Caller ID relay (~CALLID). When the MDP detects a Calling Number Delivery (CND) message, the ~RLYA output is asserted to close the Caller ID relay in order to AC couple the CND information to the MDP RIN input (without closing the off-hook relay and allowing loop current flow which would indicate an off-hook condition).
~RLYB (~TALK)	OD	**Relay B Control.** The ~RLYB open drain output can directly drive a reed relay coil with a minimum resistance of 360 ohms (9.2 mA max. @ 3.3V). A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). ~RLYB is controlled by host setting/resetting of the RB bit. In a typical application, ~RLYB is connected to the normally closed Talk/Data relay (~TALK). In this case, ~RLYB active opens the relay to disconnect the handset from the telephone line.
MICM	I(DA)	**Modem Microphone Input.** MICM is a single-ended microphone input. The input impedance is > 70k Ω. **NOTE: If not used, do not tie directly to ground; this input has a bias voltage of +1.35V (VAA = +3.3V) or +2.5V (VAA = +5V).**
SPK	O(DF)	**Speaker Analog Output.** The SPK analog output can originate from one of five different sources: RIN, TELIN, MICM or MICV or from the MDP's internal voice playback mode. The SPK on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the SPK output is clamped to the voltage at the VC pin. The SPK output can drive an impedance as low as 300 ohms. In a typical application, the SPK output is an input to an external LM386 audio power amplifier.
SPKMD	OA	**Modem Speaker Digital Output.** The SPKMD digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator to create a PC Card (PCMCIA)-compatible signal.
VREF	REF	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
VC	REF	**Low Voltage Reference.** For the 144-pin TQFP, connect to AGND through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel. For the 100-pin PQFP, connect to a ferrite bead and connect the other end of the ferrite bead to DGND through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
MICV/NC*	I(DA)	**Voice Microphone Input.** MICV is a single-ended microphone input. Typically, MICV is connected to a microphone output for recording voice e.g., in a speakerphone application. **NOTE: If not used, do not tie directly to ground; this input has a bias voltage of +1.35V (VAA = +3.3V) or +2.5V (VAA = +5V).**
TELIN/NC*	I(DA)	**Telephone Analog Input.** TELIN is a single-ended input with 70K Ω input impedance. Typically, TELIN is connected to a telephone handset microphone circuit. **NOTE: If not used, do not tie directly to ground; this input has a bias voltage of +1.35V (VAA = +3.3V) or +2.5V (VAA = +5V).**
TELOUT/NC*	O(DF)	**Telephone Analog Output.** TELOUT is a single-ended output that can drive a 300 Ω load. Typically, TELOUT is connected to a telephone handset speaker circuit.
MICBIAS	REF	**Microphone Bias.** Microphone bias reference voltage.

Table 6. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
MISCELLANEOUS		
TIRO2	IA	NC
RESERVED		Reserved Function. May be connected to internal circuit. Leave open.
MDP INTERCONNECT		
GP00	DI	To ~RDCLK.
SLEEPO	DI	To IASLEEP.
IASLEEP	DI	To SLEEPO.
MSCLK	DI	To IA1CLK.
CLKOUT	DI	To MCLKIN & VCLKIN.
SR1IO	DI	To MCNTRLSIN.
SR3IN	DI	To VRXOUT.
IA1CLK	DI	To MSCLK.
SA1CLK	DI	To MSTROBE.
SR4OUT	DI	To MTXSIN.
MCLKIN	DI	To CLKOUT.
VCLKIN/NC*	DI	To CLKOUT.
MSTROBE	DI	To SA1CLK.
VSTROBE/NC*	DI	To SA2CLK.
MCNTRLSIN	DI	To SR1IO.
VSCLK/NC*	DI	To SR2CLK.
VCNTRLSIN/NC*	DI	To SR2IO.
MRXOUT	DI	To SR4IN.
VTXSIN/NC*	DI	To SR3OUT.
VRXOUT/NC*	DI	To SR3IN.
MTXSIN	DI	To SR4OUT.
SR2IO	DI	To VCNTRLSIN.
SR4IN	DI	To MRXOUT.
SR2CLK	DI	To VSCLK.
SA2CLK	DI	To VSTROBE.
SR3OUT	DI	To VTXSIN.

* NC on non-SP models. External interconnects as described can made for the NC pins on non-SP models in case SP models are ever substituted in the application design and SP support is required.

Table 7. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage	V_{IH}				Vdc	
Type IA		2.0	–	V_{CC}		
Input High Current	I_{IH}	–	–	40	µA	
Input Low Voltage	V_{IL}	0.3		0.8	VDC	
Input Low Current	I_{IL}	–	–	40	µA	
Input Leakage Current	I_{IN}	–	–	±100	µADC	V_{IN} = 0 to +3.3V, V_{CC} = 3.6V
Output High Voltage	V_{OH}		–	–	VDC	
Type OA		2.4	–	V_{CC}		I_{LOAD} = – 100 µA
Type OD						I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				VDC	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OD		–	–	0.75		I_{LOAD} = 15 mA
Three-State (Off) Current	I_{TSI}			±10	µADC	V_{IN} = 0.4 to V_{CC}-1

Table 8. Analog Electrical Characteristics

Signal Name	Type	Characteristic	Value
RIN, TELIN, MICM, MICV	I (DA)	Input Impedance	> 70K Ω
		AC Input Voltage Range	1.1 VP-P
		Reference Voltage	+1.35 VDC (VAA = +3.3V) or +2.5 VDC (VAA = +5V)
TXA1, TXA2, TELOUT	O (DD)	Minimum Load	300 Ω
		Maximum Capacitive Load	0 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	1.4 VP-P (VAA = +3.3V) or 2.2 VP-P (VAA = +5V) (with reference to ground and a 600 Ω load)
		Reference Voltage	+1.35 VDC (VAA = +3.3V) or +2.5 VDC (VAA = +5V)
		DC Offset Voltage	± 200 mV
SPK	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	1.4 VP-P (VAA = +3.3V) or 2.2 VP-P (VAA = +5V)
		Reference Voltage	+1.35 VDC (VAA = +3.3V) or +2.5 VDC (VAA = +5V)
		DC Offset Voltage	± 20 mV

Table 9. Current and Power Requirements

Mode	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)	Notes
Normal Mode	75	84	250	300	f = 28.224 MHz
Sleep Mode	10	—	33	—	f = 28.224 MHz
Stop Mode	<0.3	—	<1	—	f = 0 MHz

Notes:
1. Operating voltage: VDD = +3.3V ± 0.3V.
2. Test conditions: VDD = +3.3V for typical values; VDD = +3.6V for maximum values.
3. Input Ripple ≤ 0.1 Vpeak-peak.
4. f = Internal frequency.
5. Stop Mode is the same as Sleep Mode with clocks turned off.

Table 10. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +4.0	V
Input Voltage	V_{IN}		V
Except XTLI		-0.5 to (VGG +0.5)*	
XTLI		-0.5 to 3.9V	
Operating Temperature Range	T_A	-0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (VAA + 0.5)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VGG +0.5)*	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±400	mA

* VGG = +5.0V ± 5% or +3.3V ± 0.3V.

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