The RF MOSFET Line

RF Power Field Effect Transistor

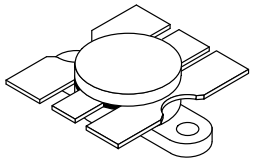
N–Channel Enhancement–Mode

MRF5035

35 W, 12.5 VOLTS, 512 MHz N–CHANNEL BROADBAND RF POWER FET

Designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 12.5 volt mobile, and base station FM equipment.

- Guaranteed Performance at 512 MHz, 12.5 Volt
  Output Power — 35 Watts
  Power Gain — 6.5 dB Min
  Efficiency — 50% Min
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 Load VSWR, @ 15.5 Volt, 512 MHz, 2 dB Overdrive
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 316–01, STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	36	Vdc
Drain–Gate Voltage (RGS = 1 MΩ)	V_{DGR}	36	Vdc
Gate–Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	97 0.56	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

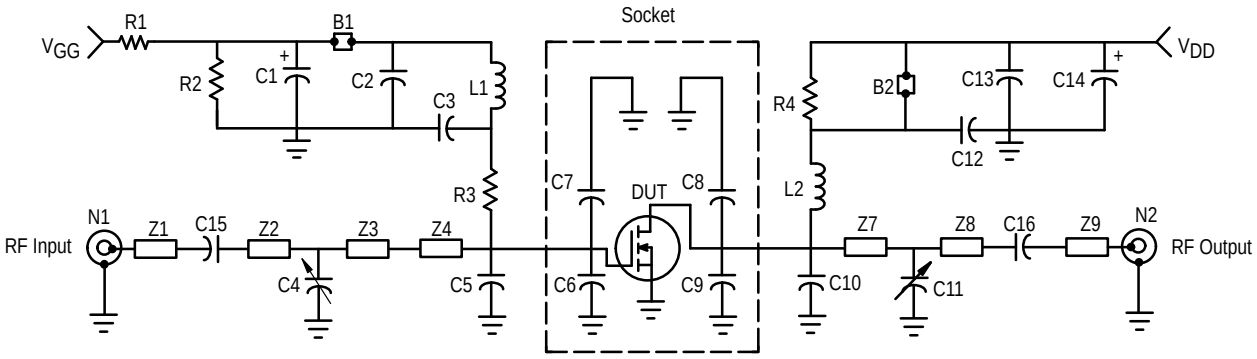
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 20 mAdc)	$V_{(BR)DSS}$	36	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	—	—	5	mAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	5	μAdc

(continued)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 25 mAdc)	$V_{GS(th)}$	1.25	2.3	3.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3 Adc)	$V_{DS(on)}$	—	—	0.422	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	3.2	—	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	88	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	197	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	18	24	29	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 35 W, I_{DQ} = 400 mA) f = 512 MHz	G_{ps}	6.5	7.5	—	dB
f = 175 MHz		—	12	—	
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 35 W, I_{DQ} = 400 mA) f = 512 MHz	η	50	55	—	%
f = 175 MHz		—	55	—	
Load Mismatch (V_{DD} = 15.5 Vdc, 2 dB Overdrive, f = 512 MHz, Load VSWR = 20:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			



Components List

B1, B2	Short Ferrite Bead, Fair Rite Products	N1, N2	Type N Flange Mount
C1, C14	10 µF, 50 V, Electrolytic	R1	1 kΩ, 1/4 W, Carbon
C2	1500 pF, Chip Capacitor	R2	1 MΩ, 1/4 W, Carbon
C3	140 pF, Chip Capacitor	R3	100 Ω, 1/4 W, Carbon
C4, C11	0–10pF, Trimmer Capacitor	R4	110 Ω, 1/4 W, Carbon
C5	30 pF, Chip Capacitor	Z1, Z9	Transmission Line*
C6, C7	43 pF, Chip Capacitor	Z2	Transmission Line*
C8, C9	36 pF, Chip Capacitor	Z3	Transmission Line*
C10	3.6 pF, Chip Capacitor	Z4	Transmission Line*
C12, C15, C16	120 pF, Chip Capacitor	Z7	Transmission Line*
C13	0.1 µF, Chip Capacitor	Z8	Transmission Line*
L1	5 Turns, 18 AWG, 0.116″ ID	Board	Glass Teflon® 0.060″
L2	8 Turns, 20 AWG, 0.125″ ID		*See Photomaster for Dimensions

Figure 1. 512 MHz Narrowband Test Circuit Electrical Schematic

TYPICAL CHARACTERISTICS

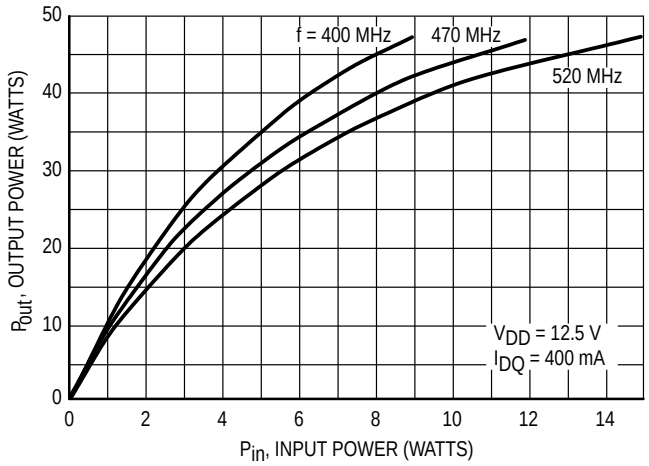


Figure 2. Output Power versus Input Power

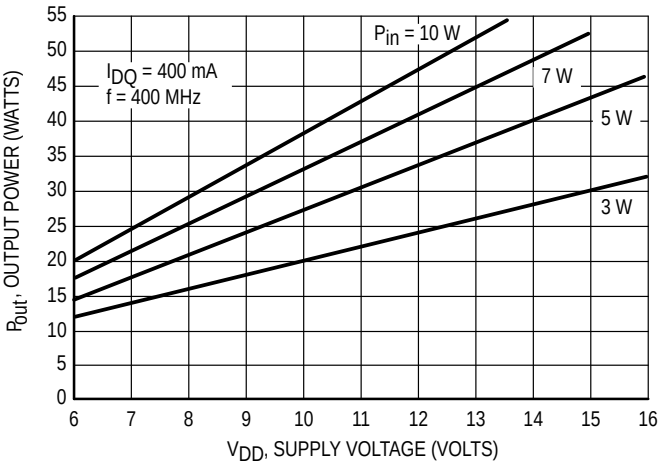


Figure 3. Output Power versus Supply Voltage

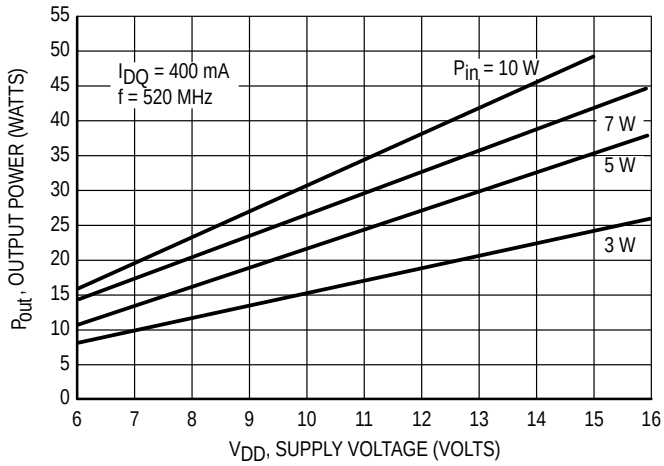


Figure 4. Output Power versus Supply Voltage

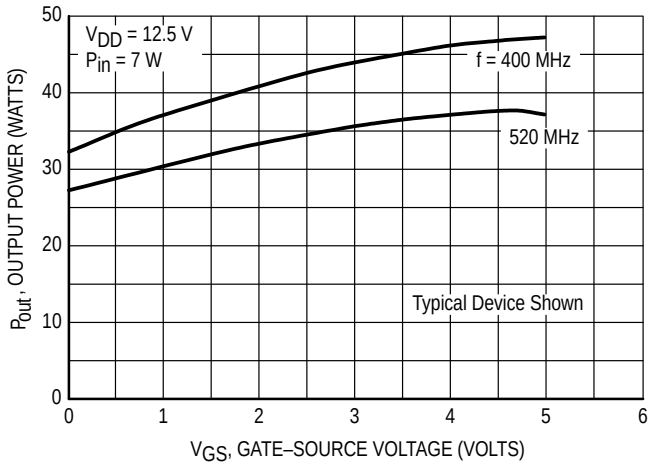


Figure 5. Output Power versus Gate Voltage

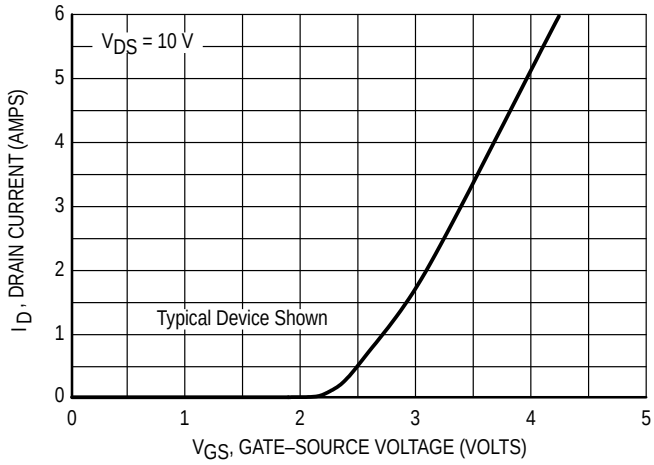


Figure 6. Drain Current versus Gate Voltage

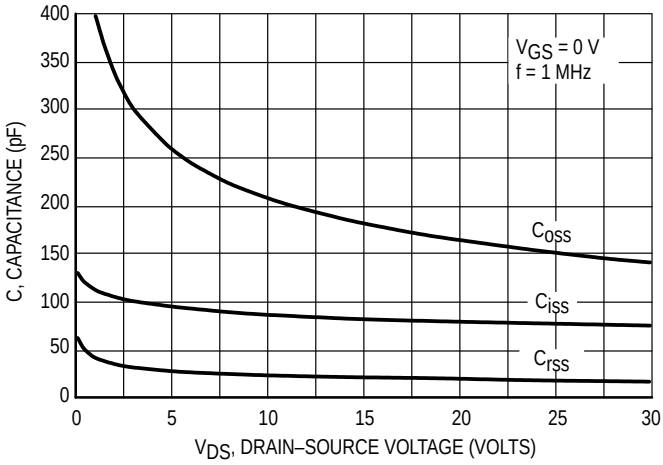


Figure 7. Capacitance versus Voltage

TYPICAL CHARACTERISTICS

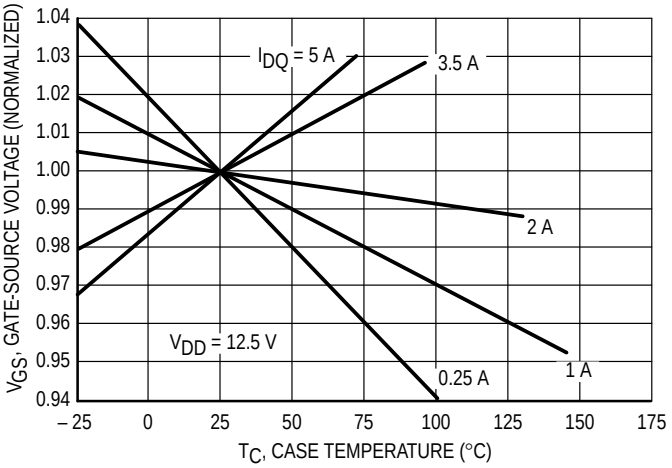


Figure 8. Gate–Source Voltage versus Case Temperature

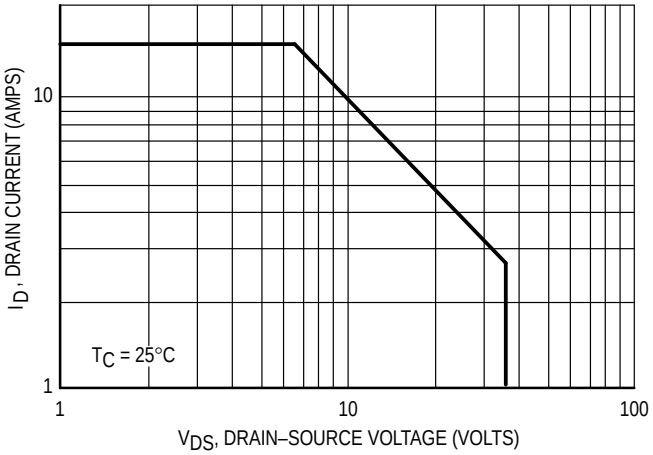
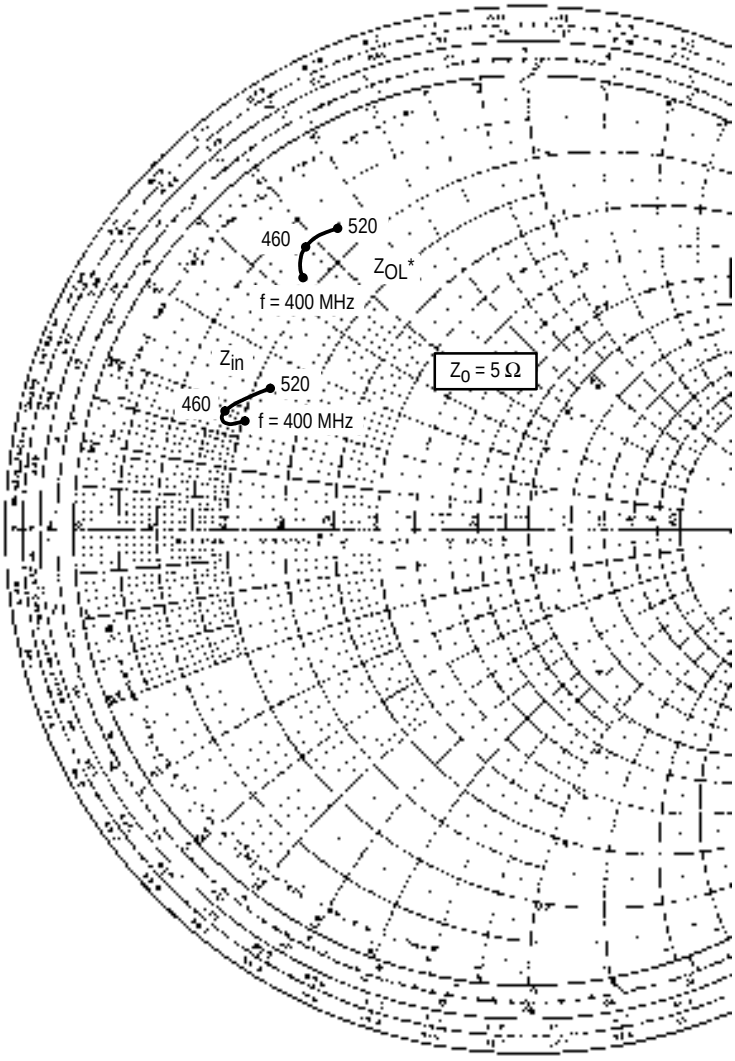


Figure 9. DC Safe Operating Area



V_{DD} = 12.5 V, I_{DQ} = 400 mA, P_{in} = 7.8 W,
Tune for Maximum Output Power

f (MHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
400	1.0 + j0.89	0.87 + j2.1
420	0.90 + j0.83	0.79 + j2.2
440	0.83 + j0.81	0.73 + j2.3
460	0.82 + j0.83	0.71 + j2.4
480	0.87 + j0.90	0.71 + j2.5
500	0.97 + j1.0	0.74 + j2.6
520	1.1 + j1.2	0.80 + j2.7

Z_{in} = Conjugate of source impedance.

Z_{OL}* = Conjugate of the load impedance at given input power, voltage and frequency that produces maximum output power.

Figure 10. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DS} = 12.5 V)

I_D = 100 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
25	0.74	–153	6.9	94	0.039	6	0.87	–169
50	0.74	–164	3.4	82	0.039	– 5	0.89	–174
100	0.77	–168	1.6	67	0.036	–16	0.90	–176
150	0.81	–170	1	56	0.032	– 25	0.92	–178
200	0.85	–171	0.69	46	0.028	– 31	0.93	–179
300	0.90	–174	0.38	32	0.019	– 36	0.96	179
400	0.93	–178	0.24	22	0.013	– 30	0.97	177
450	0.94	–179	0.20	19	0.010	– 22	0.97	175
500	0.95	179	0.17	16	0.008	– 8	0.98	174
600	0.96	176	0.12	13	0.008	27	0.98	172

I_D = 400 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
25	0.88	–163	7.8	94	0.018	7	0.93	–175
50	0.88	–172	3.9	87	0.018	3	0.93	–178
100	0.88	–176	1.9	77	0.018	–1	0.94	–180
150	0.89	–178	1.3	70	0.017	– 2	0.94	179
200	0.89	–179	0.91	63	0.016	–1	0.94	178
300	0.91	180	0.57	51	0.014	3	0.95	177
400	0.92	178	0.39	41	0.012	14	0.96	175
450	0.93	177	0.33	37	0.012	22	0.96	174
500	0.94	176	0.29	33	0.012	29	0.97	173
600	0.95	174	0.22	27	0.014	42	0.97	171

I_D = 1 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
25	0.92	–165	7.8	95	0.013	9	0.94	–177
50	0.91	–173	3.9	88	0.013	6	0.95	–179
100	0.92	–177	1.9	81	0.013	7	0.95	179
150	0.92	–179	1.3	75	0.013	9	0.95	179
200	0.92	180	0.95	69	0.012	12	0.95	178
300	0.93	178	0.61	59	0.012	21	0.96	176
400	0.94	176	0.43	50	0.013	32	0.96	174
450	0.94	175	0.38	46	0.013	37	0.97	174
500	0.94	174	0.33	43	0.014	42	0.97	173
600	0.95	173	0.26	36	0.016	49	0.97	171

I_D = 5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
25	0.94	–164	7.2	95	0.010	10	0.95	–178
50	0.94	–172	3.6	89	0.010	9	0.95	–180
100	0.94	–177	1.8	81	0.010	11	0.96	179
150	0.94	–179	1.2	76	0.011	16	0.96	178
200	0.94	179	0.89	70	0.011	21	0.96	177
300	0.95	177	0.57	61	0.011	31	0.96	176
400	0.95	176	0.42	52	0.013	41	0.97	174
450	0.95	175	0.36	48	0.013	45	0.97	173
500	0.96	174	0.32	45	0.014	48	0.97	172
600	0.96	172	0.26	39	0.017	54	0.97	171

DESIGN CONSIDERATIONS

The MRF5035 is a common–source, RF power, N–Channel enhancement mode, Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design. Motorola Application Note AN211A, “FETs in Theory and Practice,” is suggested reading for those not familiar with the construction and characteristics of FETs.

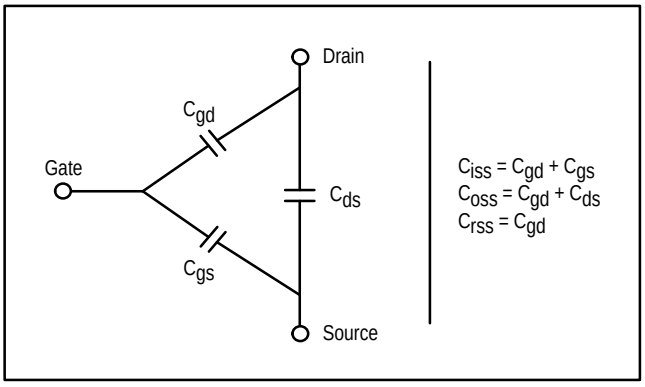
This device was designed primarily for 12.5 volt VHF and UHF Land Mobile FM power amplifier applications. The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{ds(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{ds(on)}$. For MOSFETs, $V_{ds(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high, on the order of 10^9 Ω, resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating – Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination – The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating must be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection – These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling networks.

Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since the MRF5035 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 6 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. The MRF5035 was characterized at I_{DQ} = 400 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws essentially no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

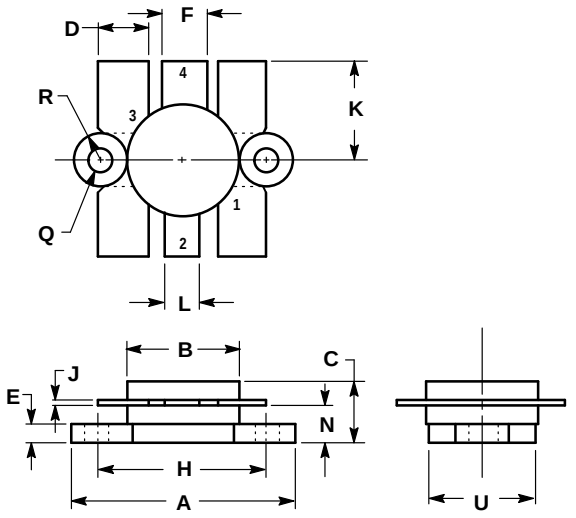
Power output of the MRF5035 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 5 is an example of output power variation with gate–source bias voltage with P_{in} held constant. This characteristic is very dependent on frequency and load line.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5035. For examples see Motorola Application Note AN721, “Impedance Matching Networks Applied to RF Power Transistors.” Both small–signal S–parameters and large–signal impedances are provided. While the S–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the high gain of the MRF5035 yield a device quite capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Different stabilizing techniques may be required depending on the desired gain and bandwidth of the application. The RF test fixture implements a resistor in shunt with the gate to improve stability. Two port stability analysis with the MRF5035 S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, “RF Small–Signal Design Using Two–Port Parameters,” for a discussion of two port network theory and stability.

PACKAGE DIMENSIONS



NOTES:
1. FLANGE IS ISOLATED IN ALL STYLES.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	24.38	25.14	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.58	0.210	0.220
E	2.16	3.04	0.085	0.120
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.17	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.31	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130
U	11.94	12.57	0.470	0.495

STYLE 3:
PIN 1. SOURCE
2. DRAIN
3. SOURCE
4. GATE

CASE 316–01
ISSUE D

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