M36L0R7060T1
M36L0R7060B1

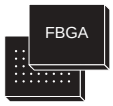
128 Mbit (Multiple Bank, Multilevel, Burst) Flash memory and 64 Mbit (Burst) PSRAM, 1.8 V supply, multichip package

Features

- Multichip package
  - 1 die of 128 Mbit (8 Mb x16, Multiple Bank, Multilevel, Burst) Flash memory
  - 1 die of 64 Mbit (4 Mb x16) Pseudo SRAM
- Supply voltage
  - V_{DDF} = V_{CCP} = V_{DDQF} = 1.7 to 1.95 V
  - V_{PPF} = 9 V for fast program
- Electronic signature
  - Manufacturer Code: 20h
  - Top Device Code M36L0R7060T1: 88C4h
  - Bottom Device Code M36L0R7060B1: 88C5h
- Package
  - ECOPACK®

Flash memory

- Synchronous / Asynchronous Read
  - Synchronous Burst Read mode: 54 MHz, 66 MHz
  - Random Access: 70 ns, 85 ns
- Synchronous Burst Read Suspend
- Programming time
  - 2.5 µs typical word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple Bank memory array: 8 Mbit banks
  - Parameter Blocks (top or bottom location)
- Common Flash Interface (CFI)
- 100 000 program/erase cycles per block
- Dual operations
  - program/erase in one Bank while read in others
  - No delay between read and write operations



TFBGA88 (ZAQ)
8 x 10 mm

- Security
  - 64 bit unique device number
  - 2112 bit user programmable OTP Cells
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked with zero latency
  - $\overline{WP}_F$ for Block Lock-Down
  - Absolute Write Protection with V_{PPF} = V_{SS}

PSRAM

- Access time: 70 ns
- Asynchronous Page Read
  - Page Size: 4, 8 or 16 words
  - Subsequent read within page: 20 ns
- Low power features
  - Automatic Temperature-compensated Self-Refresh (TCR)
  - Partial Array Self-Refresh (PASR)
  - Deep Power-Down (DPD) mode
- Synchronous Burst Read/Write

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1 Description

The M36L0R7060T1 and M36L0R7060B1 combine two memory devices in a multichip package:

- a 128-Mbit, Multiple Bank Flash memory, the M58LR128HT or M58LR128HB
- a 64-Mbit PseudoSRAM, the M69KB096AM

The purpose of this document is to describe how the two memory components operate with respect to each other. It must be read in conjunction with the M58LR128HTB and M69KB096AM datasheets, where all specifications required to operate the Flash memory and PSRAM components are fully detailed. These datasheets are available from your local STMicroelectronics distributor.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA88 (8 × 10 mm, 8 × 10 ball array, 0.8 mm pitch) package. The memory is supplied with all the bits erased (set to '1').

Figure 1. Logic diagram

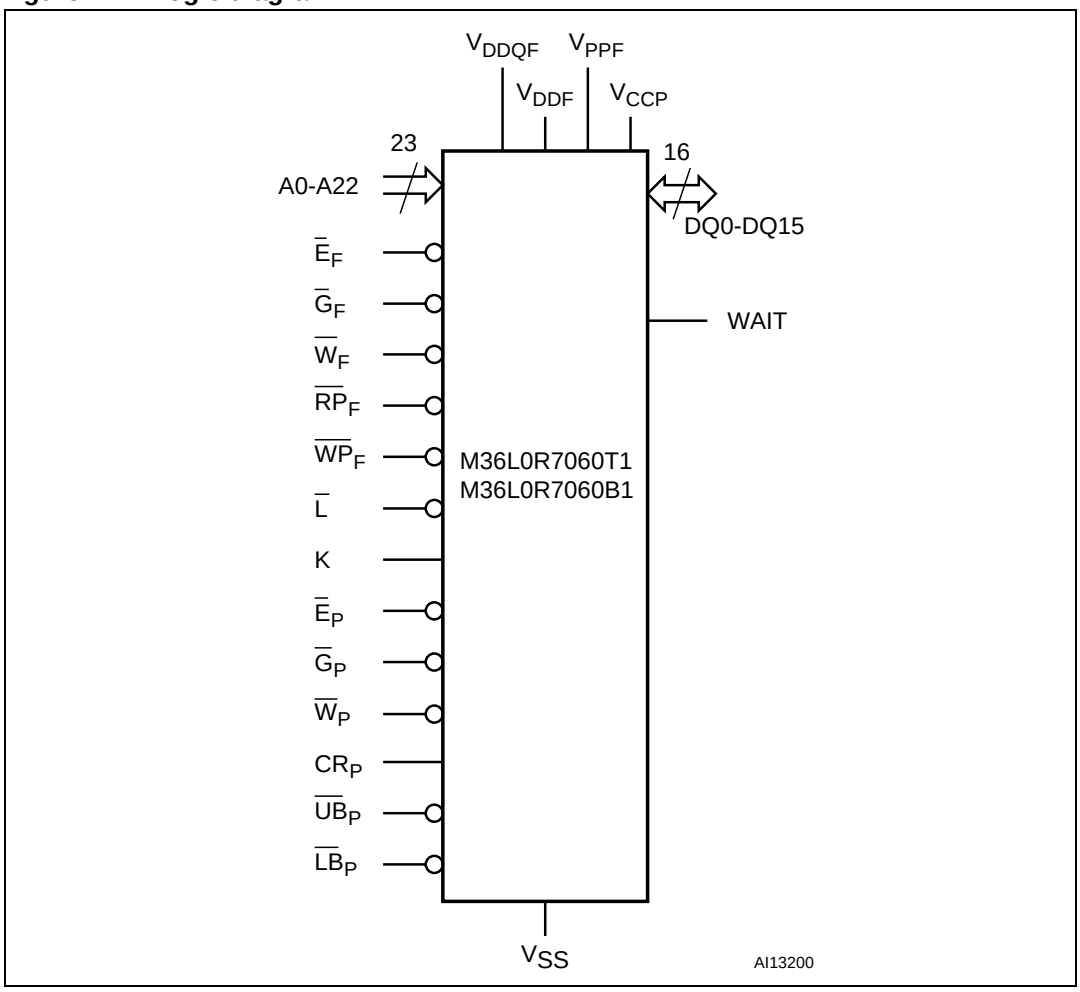
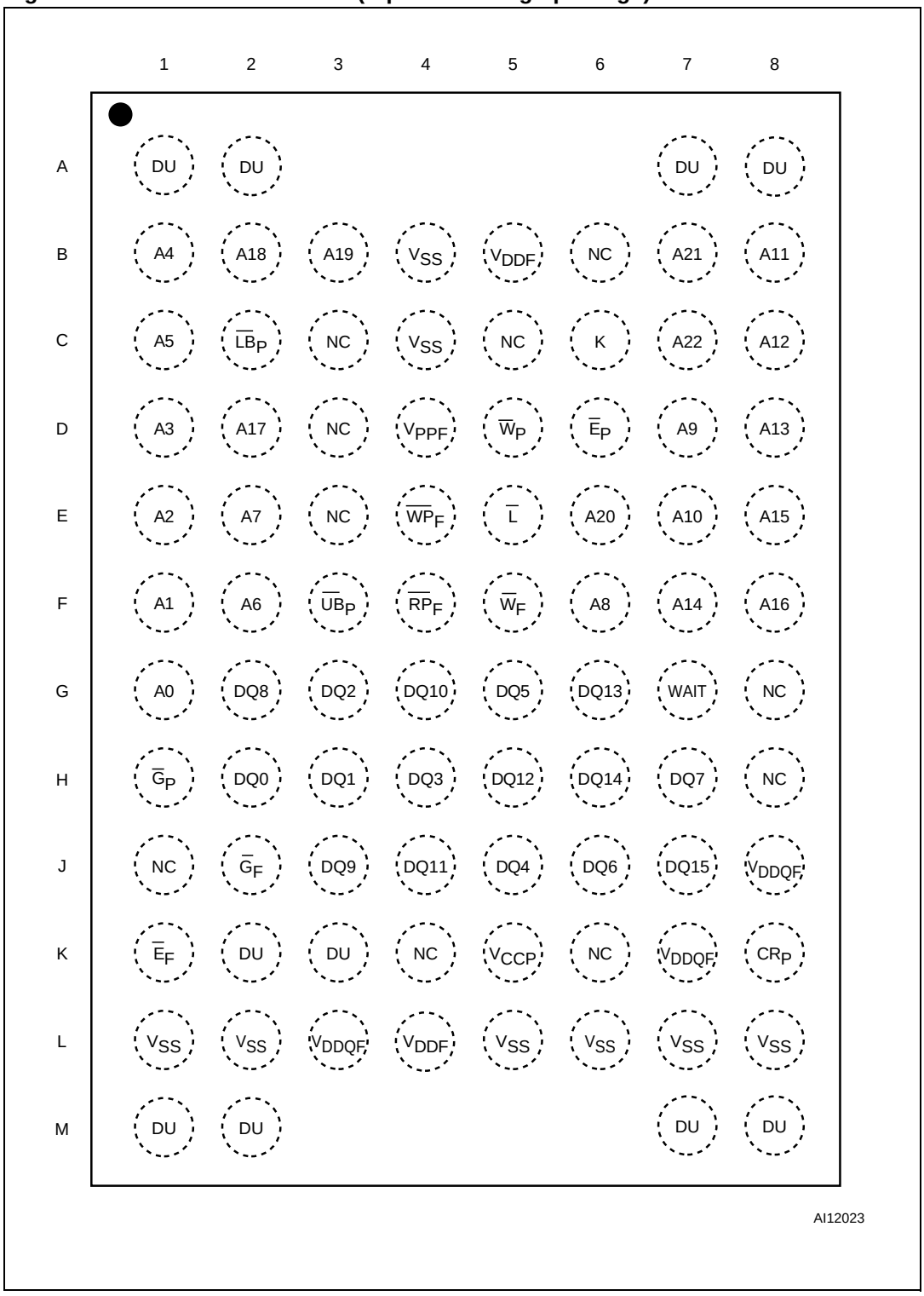


Table 1. Signal names

Signal name	Function	Direction
A0-A22	Address inputs	Inputs
DQ0-DQ15	Common Data input/output	I/O
$\overline{L}$	Latch Enable input for Flash memory and PSRAM	Input
K	Burst Clock for Flash memory and PSRAM	Input
WAIT	Wait Data in Burst Mode for Flash memory and PSRAM	Output
V_{DDF}	Flash memory power supply	
V_{DDQF}	Flash power supply for I/O buffers	
V_{PPF}	Flash optional supply voltage for Fast Program & Erase	
V_{SS}	Ground	
V_{CCP}	PSRAM power supply	
NC	Not connected internally	
DU	Do not use as internally connected	
Flash memory		
$\overline{E}_F$	Chip Enable input	Input
$\overline{G}_F$	Output Enable Input	Input
$\overline{W}_F$	Write Enable input	Input
$\overline{RP}_F$	Reset input	Input
$\overline{WP}_F$	Write Protect input	Input
PSRAM		
$\overline{E}_P$	Chip Enable input	Input
$\overline{G}_P$	Output Enable input	Input
$\overline{W}_P$	Write Enable input	Input
CR_P	Configuration Register Enable input	Input
$\overline{UB}_P$	Upper Byte Enable input	Input
$\overline{LB}_P$	Lower Byte Enable input	Input

Figure 2. TFBGA connections (top view through package)



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names*, for a brief overview of the signals connect-ed to this device.

2.1 Address inputs (A0-A22)

Addresses A0-A21 are common inputs for the Flash memory and PSRAM components. The other lines (A22) is an input for the Flash memory component only.

The Address inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. The Flash memory is accessed through the Chip Enable signal ($\overline{E}_F$) and through the Write Enable signal ($\overline{W}_F$), while the PSRAM is accessed through the Chip Enable signal ($\overline{E}_P$) and the Write Enable signal ($\overline{W}_P$).

2.2 Data input/output (DQ0-DQ15)

The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Bus Write operation.

For the PSRAM component, the upper Byte Data inputs/outputs (DQ8-DQ15) carry the data to or from the upper part of the selected address when Upper Byte Enable ($\overline{UB}_P$) is driven Low. The lower Byte Data inputs/outputs (DQ0-DQ7) carry the data to or from the lower part of the selected address when Lower Byte Enable ($\overline{LB}_P$) is driven Low. When both $\overline{UB}_P$ and $\overline{LB}_P$ are disabled, the Data inputs/outputs are high impedance.

2.3 Latch Enable ($\overline{L}$)

The Latch Enable pin is common to the Flash memory and PSRAM components.

For details of how the Latch Enable signal behaves, please refer to the datasheets of the respective memory components: M69KB096AM for the PSRAM and M58LR128HTB for the Flash memory.

2.4 Clock (K)

The Clock input pin is common to the Flash memory and PSRAM components.

For details of how the Clock signal behaves, please refer to the datasheets of the respective memory components: M69KB096AM for the PSRAM and M58LR128HTB for the Flash memory.

2.5 Wait (WAIT)

WAIT is an output pin common to the Flash memory and PSRAM components. However the WAIT signal does not behave in the same way for the PSRAM and the Flash memory.

For details of how it behaves, please refer to the M69KB096AM datasheet for the PSRAM and to the M58LR128HTB datasheet for the Flash memory.

2.6 Flash Chip Enable ($\overline{E}_F$)

The Flash Chip Enable input activates the control logic, input buffers, decoders and sense amplifiers of the Flash memory component. When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the Flash memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

2.7 Flash Output Enable ($\overline{G}_F$)

The Output Enable pin controls the data outputs during Flash memory Bus Read operations.

2.8 Flash Write Enable ($\overline{W}_F$)

The Write Enable controls the Bus Write operation of the Flash memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.9 Flash Write Protect ($\overline{WP}_F$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL}, Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, V_{IH}, Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (See the Lock Status Table in the M30L0R7000T1/B1 datasheet).

2.10 Flash Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the Flash memory. When Reset is at V_{IL}, the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to the M58LR128HTB datasheet, for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3 V logic without any additional circuitry. It can be tied to V_{RPH} (refer to the M58LR128HTB datasheet).

2.11 PSRAM Chip Enable input ($\overline{E}_P$)

The Chip Enable input activates the PSRAM when driven Low (asserted). When de-asserted (V_{IH}), the device is disabled, and goes automatically in low-power Standby mode or Deep Power-down mode, according to the RCR settings.

2.12 PSRAM Write Enable ($\overline{W}_P$)

Write Enable, $\overline{W}_P$, controls the Bus Write operation of the PSRAM. When asserted (V_{IL}), the device is in Write mode and Write operations can be performed either to the configuration registers or to the memory array.

2.13 PSRAM Output Enable ($\overline{G}_P$)

When held Low, V_{IL}, the Output Enable, $\overline{G}_P$, enables the Bus Read operations of the memory.

2.14 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte En-able, $\overline{UB}_P$, gates the data on the Upper Byte Data inputs/outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

2.15 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$, gates the data on the Lower Byte Data inputs/outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

If both $\overline{LB}_P$ and $\overline{UB}_P$ are disabled (High) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as $\overline{E}_P$ remains Low.

2.16 PSRAM Configuration Register Enable (CR_P)

When this signal is driven High, V_{IH}, bus read or write operations access either the value of the Refresh Configuration Register (RCR) or the Bus Configuration Register (BCR) according to the value of A19.

2.17 V_{DDF} supply voltage

V_{DDF} provides the power supply to the internal core of the Flash memory. It is the main power supply for all Flash memory operations (Read, Program and Erase).

2.18 V_{CCP} supply voltage

V_{CCP} provides the power supply to the internal core of the PSRAM device. It is the main power supply for all PSRAM operations.

2.19 V_{DDQF} supply voltage

V_{DDQF} provides the power supply for the Flash I/O pins. This allows all outputs to be powered independently of the Flash core power supplies, V_{DDF} and V_{CCP}.

2.20 V_{PPF} Program supply voltage

V_{PPF} is both a Flash control input and a Flash power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0V to V_{DDQF}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against Program or Erase, while V_{PP} in the V_{PP1} range enables these functions (see the M58LR128HTB datasheet for the relevant values). V_{PPF} is only sampled at the beginning of a Program or Erase; a change in its value after the operation has started does not have any effect and Program or Erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed.

2.21 V_{SS} ground

V_{SS} is the common ground reference for all voltage measurements in the Flash (core and I/O buffers) and PSRAM chips. It must be connected to the system ground.

Note: Each Flash memory device in a system should have their supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1 µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 5: AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

3 Functional description

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by two Chip Enable inputs: $\overline{E}_F$ for the Flash memory and $\overline{E}_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations on one of the Flash memory and the PSRAM components which would result in a data bus contention. Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 3. Functional block diagram

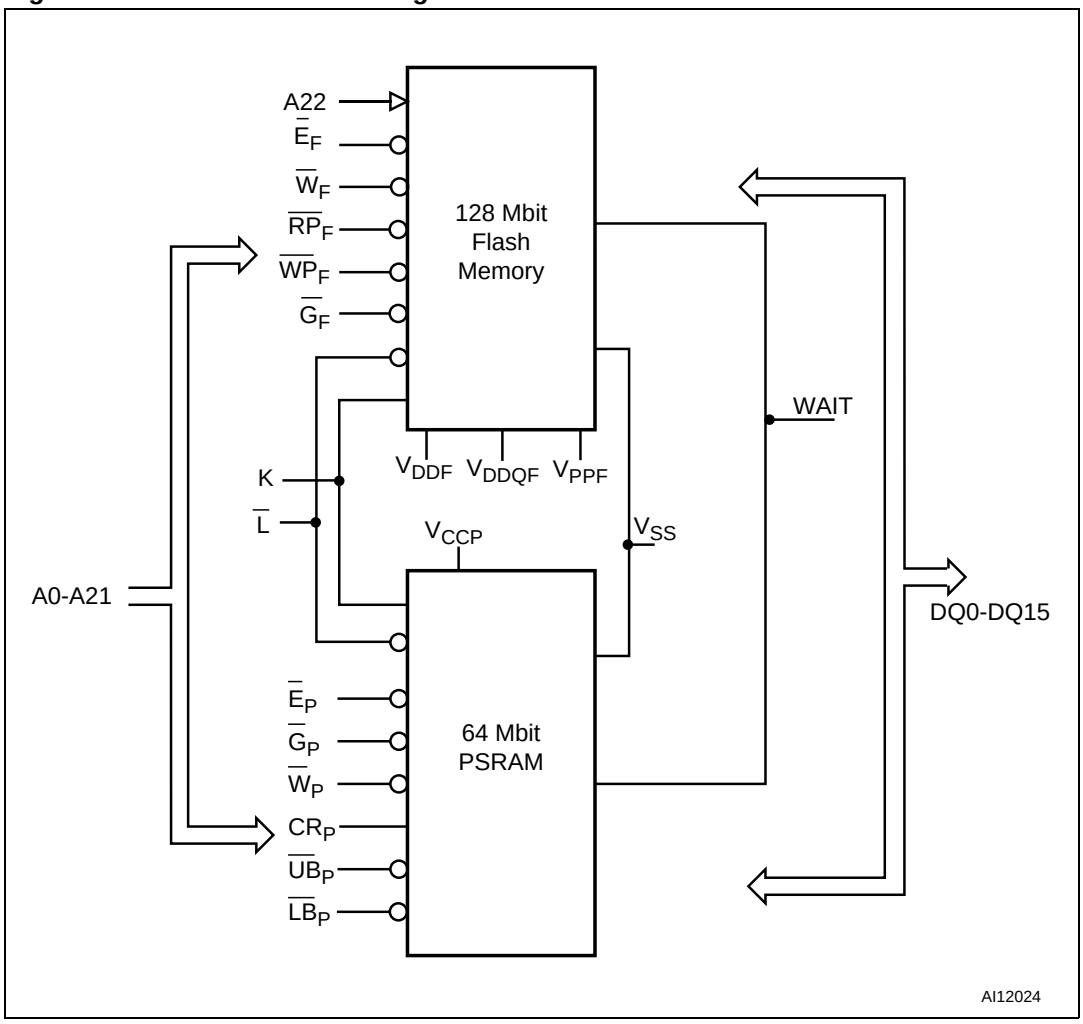


Table 2. Main operating modes(1)

Operation(2)(3)	$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{L}_F$	$\overline{RP}_F$	$WAIT_F$(4)	$\overline{E}_P$	CR_P	$\overline{G}_P$	$\overline{W}_P$	$\overline{LB}_P$,$\overline{UB}_P$	A19	A18	A0-A17 A20-A21	DQ15-DQ0
Flash Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}(5)	V_{IH}		PSRAM must be disabled.								Flash Data Out
Flash Write	V_{IL}	V_{IH}	V_{IL}	V_{IL}(5)	V_{IH}										Flash Data In
Flash Address Latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}										Flash Data Out or Hi-Z(6)
Flash Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}	Hi-Z	Any PSRAM mode is allowed.								Hi-Z
Flash Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z									Hi-Z
Flash Reset	X	X	X	X	V_{IL}	Hi-Z									Hi-Z
PSRAM Read	The Flash memory must be disabled.						V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Valid			PSRAM data out
PSRAM Write							V_{IL}	V_{IL}	X	V_{IL}	V_{IL}	Valid			PSRAM data in
PSRAM Program Configuration Register (CR Controlled)(7)							V_{IL}	V_{IH}	X	V_{IL}	X	00(RCR) 10(BCR) (8)		BCR/ RCR Data	Hi-Z
PSRAM Standby	Any Flash mode is allowed.						V_{IH}	V_{IL}	X	X	X	X	X	X	Hi-Z
PSRAM Deep Power-Down(9)							V_{IH}	X	X	X	X	X	X	X	Hi-Z

1. X = Don't care.
2. In the PSRAM, the Clock signal, K, must remain Low in asynchronous operating mode, and to achieve standby power in Standby and Deep Power-Down modes.
3. The PSRAM must have been configured to operate in asynchronous mode by setting BCR15 to '1' (default value).
4. WAIT signal polarity is configured using the Set Configuration Register command. See the M58LR128HTB datasheet for details.
5. $\overline{L}_F$ can be tied to V_{IH} if the valid address has been previously latched.
6. Depends on $\overline{G}_F$.
7. BCR and RCR only.
8. A18 and A19 are used to select the BCR, RCR or DIDR registers.
9. Bit 4 of the Refresh Configuration Register must be set to '0' and $\overline{E}$ must be maintained High, V_{IH}, during Deep Power-Down mode.

4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient operating temperature	–25	85	°C
T_{BIAS}	Temperature under bias	–25	85	°C
T_{STG}	Storage temperature	–55	125	°C
V_{IO}	Input or output voltage	–0.2	2.45	V
V_{DDF}, V_{DDQF}, V_{CCP}	Core and input/output supply voltages	–0.2	2.45	V
V_{PPF}	Flash program voltage	–0.2	10	V
I_O	Output short circuit current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 4: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Flash memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{DDF} supply voltage	1.7	1.95	–	–	V
V_{CCP} supply voltage	–	–	1.7	1.95	V
V_{DDQF} supply voltage	1.7	1.95	–	–	V
V_{PPF} supply voltage (Factory environment)	8.5	9.5	–	–	V
V_{PPF} supply voltage (Application environment)	–0.4	V_{DDQF} +0.4	–	–	V
Ambient operating temperature	–25	85	–25	85	°C
Load capacitance (C_L)	30		30		pF
Output circuit resistors (R_1, R_2)	16.7		16.7		kΩ
Input rise and fall times		5		2	ns
Input pulse voltages	0 to V_{DDQF}		0 to $V_{CCP}/2$		V
Input and output timing ref. voltages	$V_{DDQF}/2$		$V_{CCP}/2$		V

Figure 4. AC measurement I/O waveform

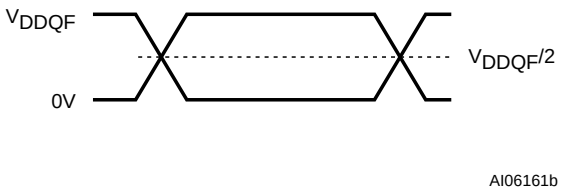


Figure 5. AC measurement load circuit

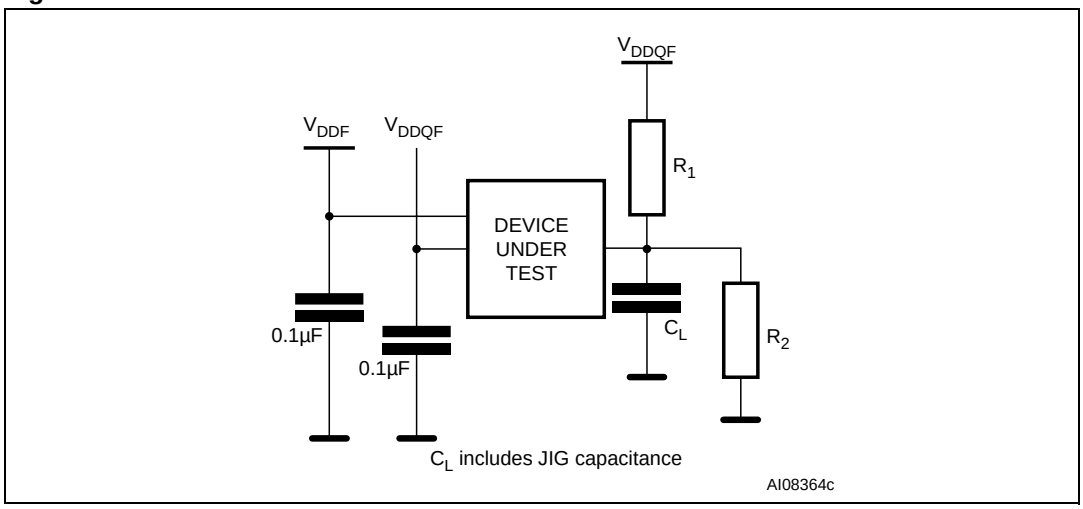


Table 5. Device capacitance

Symbol	Parameter	Test Condition	Min	Max(1)	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		14	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		18	pF

1. Sampled only, not 100% tested.

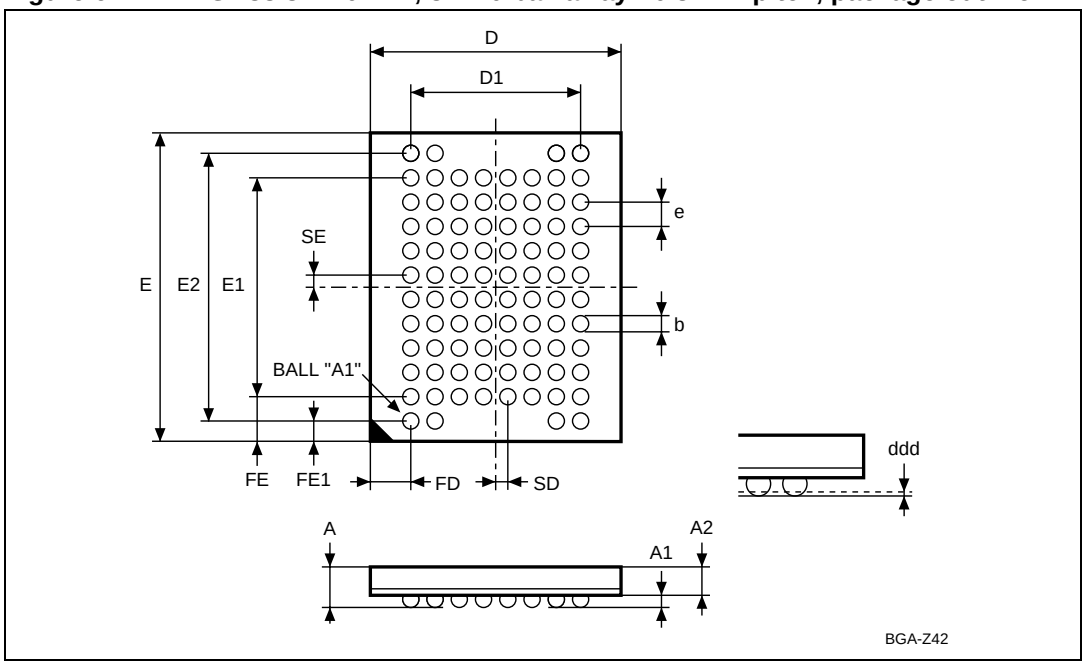
Please refer to the M58LR128HTB and M69KB096AM datasheets for further DC and AC characteristics values and illustrations.

6 Package mechanical

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 6. TFBGA88 8 × 10 mm, 8 × 10 ball array - 0.8 mm pitch, package outline



1. Drawing is not to scale.

Table 6. Stacked TFBGA88 8 × 10 mm - 8 × 10 active ball array, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.850			0.0335		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600			0.2205		
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200			0.2835		
E2	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	1.200			0.0472		
FE	1.400			0.0551		
FE1	0.600			0.0236		
SD	0.400			0.0157		
SE	0.400			0.0157		

7 Part numbering

Table 7. Ordering information scheme

Example: M36 L 0 R 7 0 6 0 T 1 ZAQ E

Device Type
M36 = Multichip package (Multiple Flash + RAM)

Flash 1 Architecture
L = Multilevel, Multiple Bank, Burst mode

Flash 2 Architecture
0 = No Die

Operating Voltage
R = V_{DDF} = V_{CCP} = V_{DDQF} = 1.7 to 1.95V

Flash 1 Density
7 = 128 Mbits

Flash 2 Density
0 = No Die

RAM 1 Density
6 = 64 Mbits

RAM 0 Density
0 = No Die

Parameter Blocks Location
T = Top Boot Block Flash
B = Bottom Boot Block Flash

Product Version
1 = 90 nm Flash technology Multilevel Design, 70 and 85 ns speed
0.11 µm PSRAM, 70 ns speed, burst mode

Package
ZAQ = Stacked TFBGA88 8 x 10 mm - 8 x 10 active ball array, 0.8 mm pitch

Option
E = ECOPACK® Standard packing
F = ECOPACK® Tape & Reel packing

Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
23-May-2006	0.1	First release.
31-Aug-2006	0.2	PSRAM changed to M69KM096AM. Blank and T removed below *Option* in *Table 7: Ordering information scheme*.
07-May-2007	1	Document status promoted from Target Specification to full Datasheet. 70 ns speed class and 66 MHz frequency added.

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