

T-75-27-07



Microcircuits

CM8870

CMOS DTMF Integrated Receivers

FEATURES

- Full DTMF receiver
- Less than 35 mW power consumption
- Industrial temperature range
- Uses quartz crystal or ceramic resonators
- Adjustable acquisition and release times
- 18-pin DIP, 18-pin SOIC, 20 pin PLCC

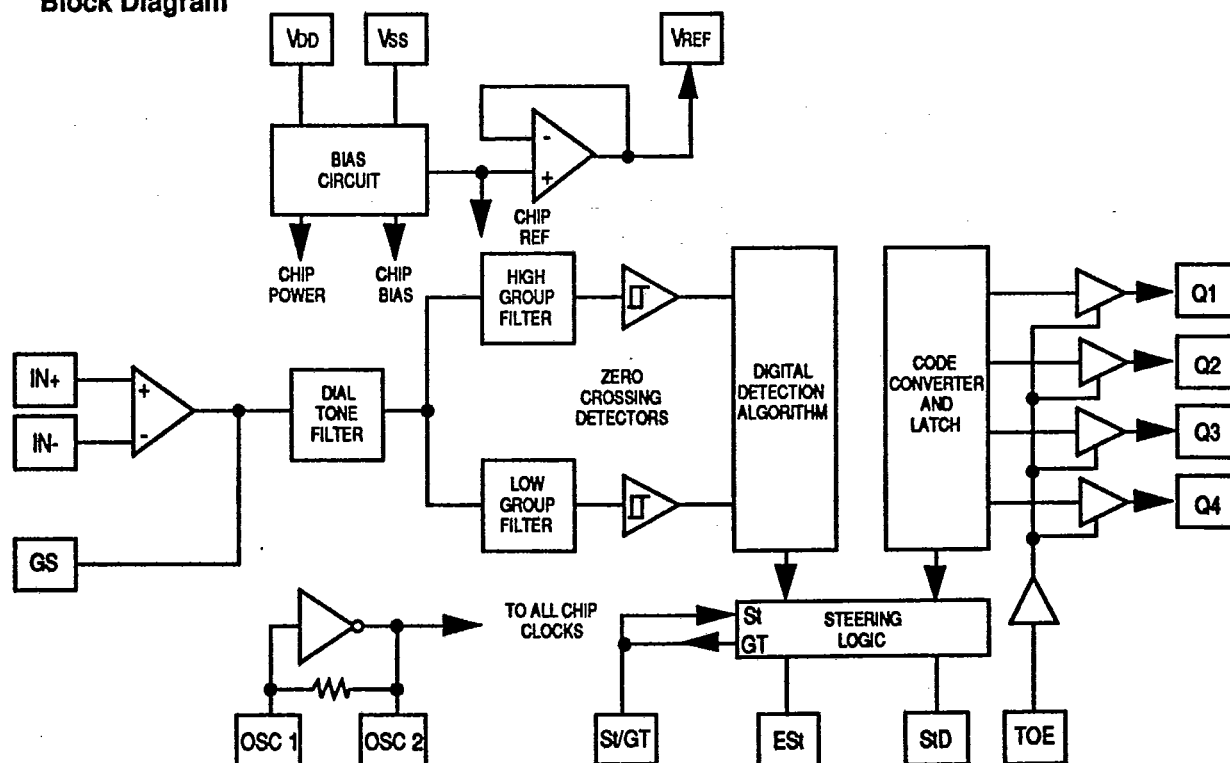
APPLICATIONS

- PABX
- Central office
- Mobile radio
- Remote control
- Remote data entry
- Call limiting
- Telephone answering systems
- Paging systems

GENERAL DESCRIPTION

The CMD CM8870 provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin DIP, SOIC, or 20-pin PLCC package. The CM8870 is manufactured using state-of-the-art CMOS process technology for low power consumption (35mW max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The CM8870 decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. The CM8870 minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal or ceramic resonator as an external component.

Block Diagram



Absolute Maximum Ratings: (Note 1)

| Parameter | Symbol | Value |
|--------------------------------|--------|------------------|
| Power Supply Voltage (VDD-VSS) | VDD | 6.0V Max |
| Voltage on any Pin | Vdc | VSS-0.3, VDD+0.3 |
| Current on any Pin | IDD | 10 mA Max |
| Operating Temperature | TA | -40°C to +85°C |
| Storage Temperature | TS | -65°C to +150°C |

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: All voltages referenced to VSS, VDD = 5.0V \pm 5%, TA = -40°C to +85°C unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|---------------------------------|----------------------------------|------|-----|------|------------|---------------------------------------|
| Operating Supply Voltage | VDD | 4.75 | | 5.25 | V | |
| Operating Supply Current | IDD | | 3.0 | 7.0 | mA | |
| Power Consumption | PO | | 15 | 35 | mW | f=3.579 MHz; VDD=5.0V |
| Low Level Input Voltage | VIL | | | 1.5 | V | VDD=5.0V |
| High Level Input Voltage | VIH | 3.5 | | | V | VDD=5.0V |
| Input Leakage Current | I _{IH} /I _{IL} | | 0.1 | | μ A | V _{IN} =VSS or VDD (Note 11) |
| Pull Up (Source) Current on TOE | ISO | | 6.5 | 20 | μ A | TOE=0V, VDD=5.0V |
| Input Impedance, (IN+, IN-) | RIN | 8 | 10 | | M Ω | @ 1KHz |
| Steering Threshold Voltage | V _{tst} | 2.2 | | 2.5 | V | VDD=5.0V |
| Low Level Output Voltage | VOL | | | 0.03 | V | VDD=5.0V, No Load |
| High Level Output Voltage | VOH | 4.97 | | | V | VDD=5.0V, No Load |
| Output Low (Sink) Current | IOL | 1.0 | 2.5 | | mA | VOUT=0.4V |
| Output High (Source) Current | IOH | 0.4 | 0.8 | | mA | VOUT=4.6V |
| Output Voltage | VREF | VREF | 2.4 | 2.7 | V | VDD=5.0V, No Load |
| Output Resistance | | ROR | 10 | | K Ω | |

Operating Characteristics: All voltages referenced to VSS, VDD = 5.0V \pm 5%, TA = -40°C to +85°C unless otherwise noted.
Gain Setting Amplifier

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|--------------------------------|-----------------|-----|-----|-----------|------------------|--------------------------------|
| Input Leakage Current | IIN | | | \pm 100 | nA | VSS < VIN < VDD |
| Input Resistance | RIN | 10 | | | M Ω | |
| Input Offset Voltage | VOS | | | \pm 25 | mV | |
| Power Supply Rejection | PSRR | 50 | | | dB | 1KHz (Note 12) |
| Common Mode Rejection | CMRR | 40 | | | dB | -3.0V < V _{IN} < 3.0V |
| DC Open Loop Voltage Gain | AVOL | 32 | | | dB | |
| Open Loop Unity Gain Bandwidth | f _c | 0.3 | | | MHz | |
| Output Voltage Swing | VO | 4.0 | | | V _{p-p} | RL \geq 100K Ω to VSS |
| Tolerable Capacitive Load (GS) | CL | | | 100 | pF | |
| Tolerable Resistive Load (GS) | RL | | | 50 | K Ω | |
| Common Mode Range | V _{cm} | 2.5 | | | V _{p-p} | No Load |



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AC Characteristics: All voltages referenced to VSS, VDD = 5.0V ±5%, TA = -40°C to +85°C, fCLK = 3.579545 MHz using test circuit (Fig. 1) unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Units | Notes |
|--|--------------------|--------|--------|-----------|-------|--|
| Valid Input Signal Levels (each tone of composite signal) | | -29 | | +1 | dBm | 1,2,3,4,5,8 |
| | | 27.5 | | 869 | mVRMS | |
| Positive Twist Accept | | | | 10 | dB | 2,3,4,8 |
| Negative Twist Accept | | | | 10 | dB | |
| Freq. Deviation Accept Limit | | | | 1.5%±2 Hz | Nom. | 2,3,5,8,10 |
| Freq. Deviation Reject Limit | | ±3.5% | | | Nom. | 2,3,5 |
| Third Tone Tolerance | | | -16 | | dB | 2,3,4,5,8,9,13,14 |
| Noise Tolerance | | | -12 | | dB | 2,3,4,5,6,8,9 |
| Dial Tone Tolerance | | | +22 | | dB | 2,3,4,5,7,8,9 |
| Tone Present Detection Time | tDP | 5 | 8 | 14 | mS | Refer to Timing Diagram (User Adjustable) Times shown are obtained with circuit in Fig. 1 |
| Tone Absent Detection Time | tDA | 0.5 | 3 | 8.5 | mS | |
| Min. Tone Duration Accept | tREC | | | 40 | mS | |
| Max. Tone Duration Reject | tREC | 20 | | | mS | |
| Min. Interdigit Pause Accept | tID | | | 40 | mS | |
| Max. Interdigit Pause Reject | tDO | 20 | | | mS | |
| Propagation Delay (St to Q) | tPQ | | 6 | 11 | μS | TOE = VDD |
| Propagation Delay (St to StD) | tPStD | | 9 | 16 | μS | |
| Output Data Set Up (Q to StD) | tQStD | | 3.4 | | μS | |
| Propagation Delay (TOE to Q) | Enable | tPTE | 50 | | nS | RL = 10KΩ CL = 50pF |
| | Disable | tPTD | 300 | | nS | |
| Crystal/Clock Frequency | fCLK | 3.5759 | 3.5795 | 3.5831 | MHz | |
| Clock Output (OSC 2) | Capacitive Load | CLO | | 30 | pF | |

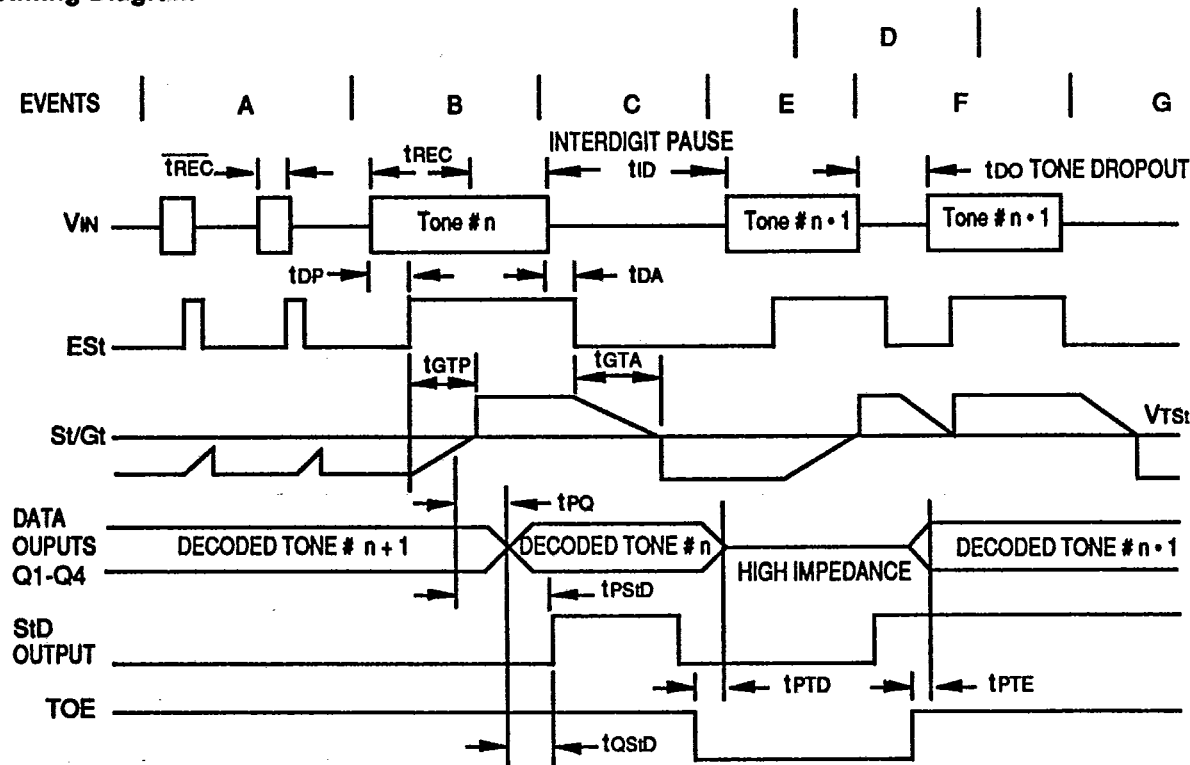
Notes:

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%.
8. For an error rate of better than 1 in 10,000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and TOE.
12. External voltage source used to bias VREF.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 1. Input DTMF tone level at -28 dBm.



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Timing Diagram



Explanation of Events

- A) Tone bursts detected, tone duration invalid, outputs not updated.
- B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.
- C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.
- D) Outputs switched to high impedance state.
- E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).
- F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.
- G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

- VIN DTMF composite input signal.
- EST Early Steering Output. Indicates detection of valid tone frequencies.
- ST/GT Steering input/guard time output. Drives external RC timing circuit.
- Q1-Q4 4-bit decoded tone output.
- ST/D Delayed Steering Output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
- TOE Tone Output Enable (input). A low level shifts Q1-Q4 to its high impedance state.
- \overline{tREC} Maximum DTMF signal duration not detected as valid.
- tREC Minimum DTMF signal duration required for valid recognition.
- tID Minimum time between valid DTMF signals.
- tDO Maximum allowable drop-out during valid DTMF signal.
- tDP Time to detect the presence of valid DTMF signals.
- tDA Time to detect the absence of valid DTMF signals.
- tGTP Guard time, tone present.
- tGTA Guard time, tone absent.



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between signals. Thus, as
ort to be considered valid,
l interruptions (drop outs)
lid pause. This capability,
selecting the steering time
ne designer to tailor per-
y of system requirements.

ire independent selection
le steering circuit of Figure
ues are chosen according

+ tGTP

7 RC

r of the device and t_{REC} is
to be recognized by the
is recommended for most
selected by the designer.
e of R for a t_{REC} of 40
A typical circuit using this
n in Figure 1. The timing
ommunication applications
Different steering arrange-
Independently the guard-
id tone absent (tGTA). This
stem specifications which
mits on both tone durator

ows the designer to tailor
lk-off and noise immunity.
-off performance, since it
nes simulated by speech
for long enough to be
a relatively short t_{REC} with
riate for extremely noisy
sition time and immunity to
its. Design information for
n in Figure 5.

CM8870 provides a differ-
er as well as a bias source
e inputs at mid-rail.

on of a feedback resistor to
justment of gain.

n, the input pins are con-
ith the op-amp connected
the input at $1/2 V_{DD}$. Figure
uration, which permits the
dback resistor R_5 .

ompleted with the addition of
st crystal or ceramic reso-
ncy of 3.579545 MHz. A
n be connected as shown
e crystal or resonator re-

Functional Description

The CMD CM8870 DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP, SOIC or 20-pin PLCC package configuration. The CM8870's internal architecture consists of a bandsplit filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The CM8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (EST). Any subsequent loss of signal condition will cause EST to fall.

Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by EST. A logic high on EST causes V_c (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (EST remains high) for the validation period (tGTP), V_c reaches the threshold (V_{Tst}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives V_c to V_{DD} . GT continues to drive high as long as EST remains high. Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse

to validate the interdigit pause
well as rejecting signals too sh
the receiver will tolerate signa
too short to be considered a va
together with the capability of s
constants externally, allows th
formance to meet a wide variety

Guard Time Adjustment

In situations which do not requ
of receive and pause, the simpl
4 is applicable. Component val
to the following formula:

$$t_{REC} = t_{DP}$$

$$t_{GTP} \approx 0.6$$

The value of t_{DP} is a parameter
the minimum signal duration
receiver. A value for C of 0.1 uF
applications, leaving R to be
For example, a suitable value
milliseconds would be 300K.
steering configuration is show
requirements for most teleco
are satisfied with this circuit. D
ments may be used to select
times for tone-present (tGTP) ar
may be necessary to meet sy
place both accept and reject lin
and interdigit pause.

Guard time adjustment also al
system parameters such as ta
Increasing t_{REC} improves talk
reduces the probability that to
will maintain signal condition
registered. On the other hand,
a long t_{DO} would be approp
environments where fast acqui
drop-outs would be requiremen
guard time adjustment is show

Input Configuration

The input arrangement of the
ential input operational amplifie
(VREF) which is used to bias th

Provision is made for connecti
the op-amp output (GS) for ad

In a single-ended configuratio
nected as shown in Figure 1 w
for unity gain and VREF biasing
6 shows the differential config
adjustment of gain with the fee

Clock Circuit

The internal clock circuit is com
a standard television color bur
nator having a resonant frequ
number of CM8870 devices ca
in Figure 7 such that only one
quired.



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Pin Function Table

| Name | Description | |
|--|--|--|
| IN+ IN- | Non-inverting input Inverting input | Connections to the front-end differential amplifier |
| GS | Gain Select. Gives access to output of front-end differential amplifier for connection of feedback resistor. | |
| VREF | Reference voltage output (nominally V _{DD} /2). May be used to bias the inputs at mid-rail. | |
| OSC 1 | Clock input | 3.579545 MHz crystal connected between these pins completes internal oscillator. |
| OSC 2 | Clock output | |
| Vss | Negative power supply (Normally connected to 0V). | |
| TOE | Three-state output enable (input). Logic high enables the outputs Q ₁ -Q ₄ . Internal pull-up. | |
| Q ₁ Q ₂ Q ₃ Q ₄ | Three-state outputs. When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Fig. 2.) | |
| StD | Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below V _{TSI} . | |
| ES _t | Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ES _t to return to a logic low. | |
| St/GT | Steering input/guard time output (bidirectional). A voltage greater than V _{TSI} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V _{TSI} frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ES _t and the voltage on St. (See Fig. 2.) | |
| VDD | Positive power supply | |
| IC | Internal connection. Must be tied to Vss. | |

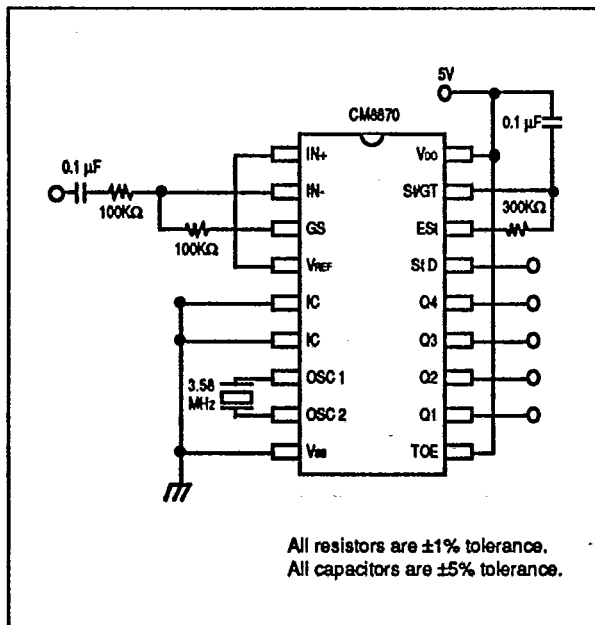


Figure 1. Single Ended Input Configuration

| FLOW | FHIGH | KEY | TOE | Q4 | Q3 | Q2 | Q1 |
|------|-------|-----|-----|----|----|----|----|
| 697 | 1209 | 1 | H | 0 | 0 | 0 | 1 |
| 697 | 1336 | 2 | H | 0 | 0 | 1 | 0 |
| 697 | 1477 | 3 | H | 0 | 0 | 1 | 1 |
| 770 | 1209 | 4 | H | 0 | 1 | 0 | 0 |
| 770 | 1336 | 5 | H | 0 | 1 | 0 | 1 |
| 770 | 1477 | 6 | H | 0 | 1 | 1 | 0 |
| 852 | 1209 | 7 | H | 0 | 1 | 1 | 1 |
| 852 | 1336 | 8 | H | 1 | 0 | 0 | 0 |
| 852 | 1477 | 9 | H | 1 | 0 | 0 | 1 |
| 941 | 1336 | 0 | H | 1 | 0 | 1 | 0 |
| 941 | 1209 | . | H | 1 | 0 | 1 | 1 |
| 941 | 1477 | # | H | 1 | 1 | 0 | 0 |
| 697 | 1633 | A | H | 1 | 1 | 0 | 1 |
| 770 | 1633 | B | H | 1 | 1 | 1 | 0 |
| 852 | 1633 | C | H | 1 | 1 | 1 | 1 |
| 941 | 1633 | D | H | 0 | 0 | 0 | 0 |
| - | - | ANY | L | Z | Z | Z | Z |

L = Logic Low, H = Logic High, Z = High Impedance

Figure 2. Functional Decode Table



CM8870

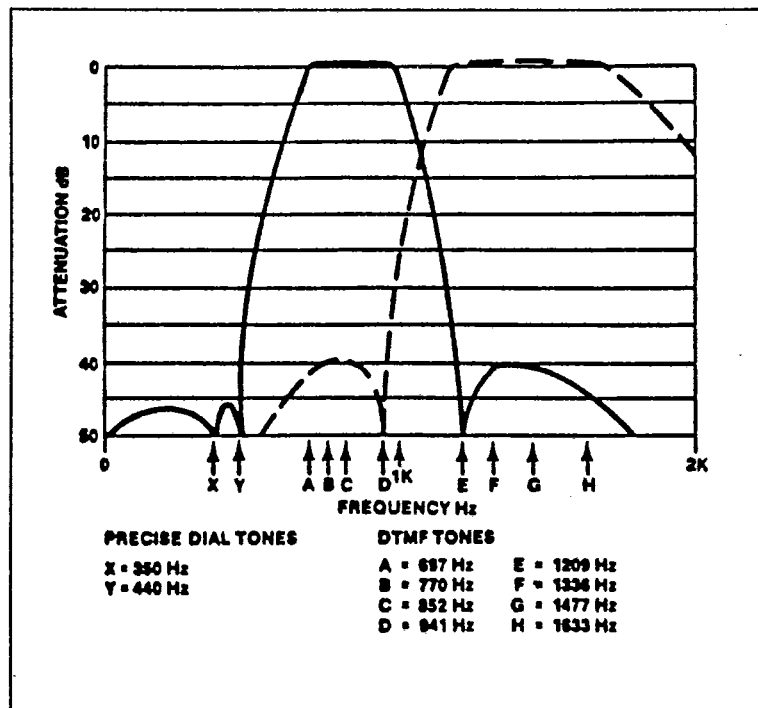


Figure 3. Typical Filter Characteristic

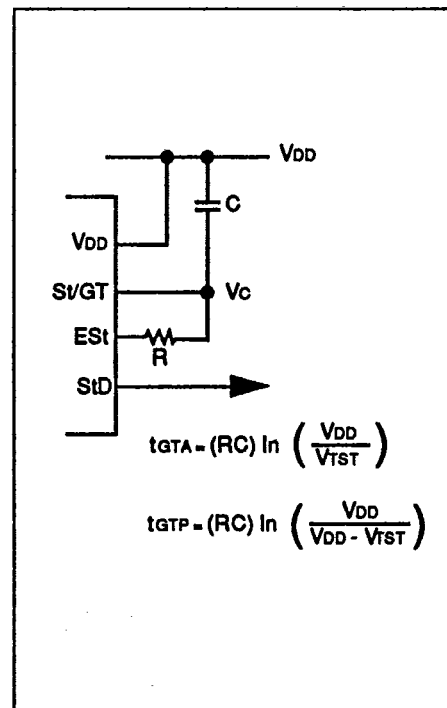


Figure 4. Basic Steering Circuit

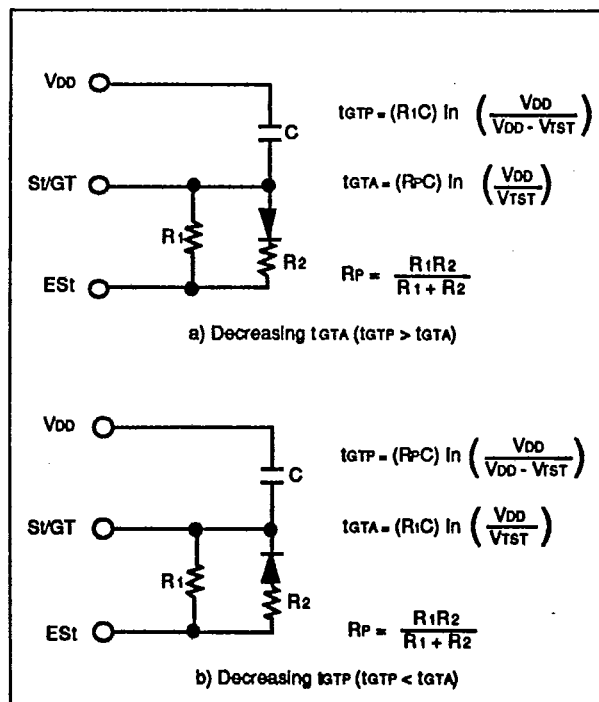


Figure 5. Guard Time Adjustment

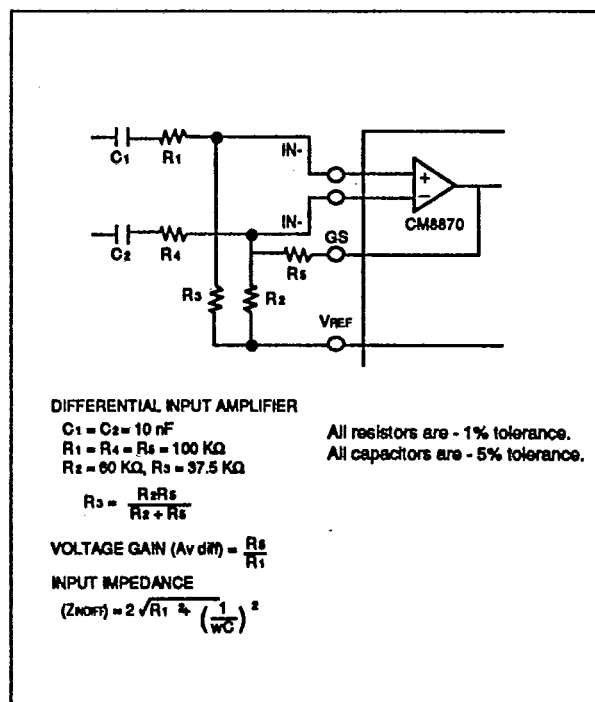


Figure 6. Differential Input Configuration

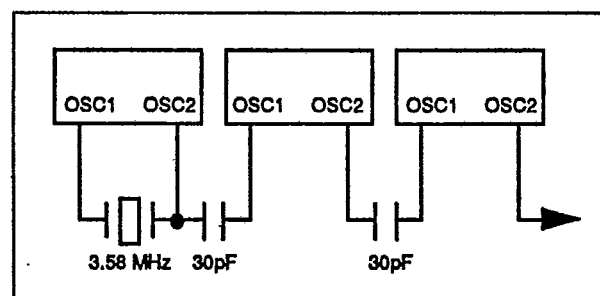
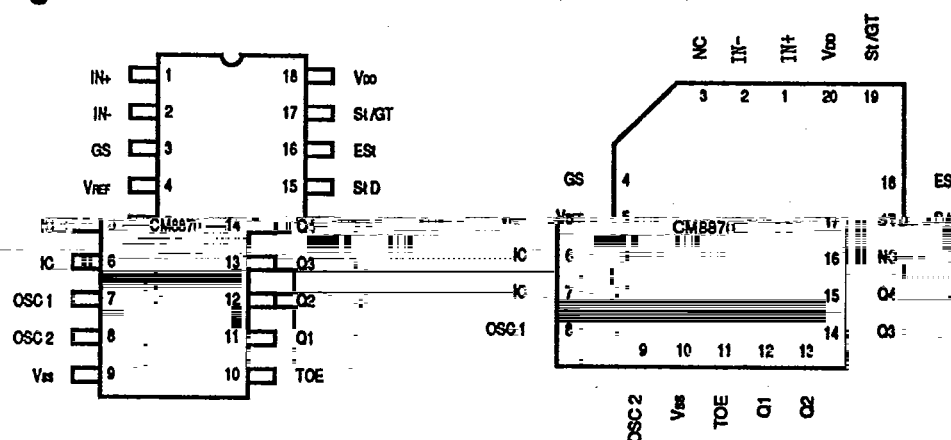
**CM8870**

Figure 7. CM8870C Crystal Connection

Pin Configuration**Ordering Information**

Product Identification Number

CM8870

D

I

Package

P - Plastic E - Leaded Chip Carrier S - SOIC
 C - Ceramic L - Leadless Chip Carrier
 D - Cerdip X - Dice

Temperature/Processing

None - 0°C to +70°C, ±5% P.S. Tol.
 I - -40°C to +85°C, ±5% P.S. Tol.