Ordering number : ENN7308

CMOS IC

LC75348, 75348M

Single-Chip Electronic Volume and Tone Control System

Overview

The LC75348 and LC75348M are electronic volume and tone control ICs that provide volume, balance, 2-band equalizer, input gain control, and input switching functions while requiring a minimal number of external components.

Functions

- Volume: 81 levels: 0 dB to –79 dB (in 1 dB steps) and –∞.
  The left and right channels are controlled independently, allowing a balance function to be implemented.
- Bass: Peaking characteristics bass control with ±20 dB range in 2 dB steps.
- Treble: Shelving characteristics treble control with ±10 dB range in 2 dB steps.
- Selector: One of 4 inputs can be selected for both left and right channels.
- Input gain: Input signal amplification from 0 to +30 dB (in 2 dB steps)

Features

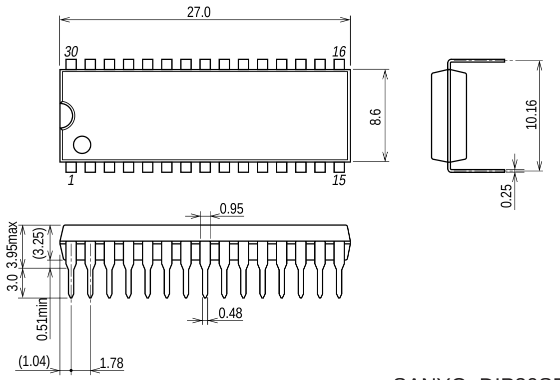
- Built-in buffer amplifiers reduce the number of external components required.
- Fabricated in a silicon gate CMOS process for minimal switching noise from built-in switches and minimal switching noise even when there is no input signal.
- Built-in zero cross circuits minimize switching noise when input signals are present.
- Built-in $V_{DD}/2$ reference voltage generator circuit.
- All functions are controlled from serial data. Supports the CCB bus.

Package Dimensions

unit: mm

3196-DIP30SD

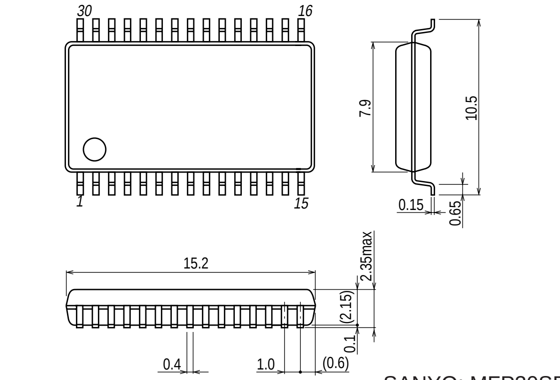
[LC75348]



SANYO: DIP30SD

3216-MFP30SD

[LC75348M]



SANYO: MFP30SD

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

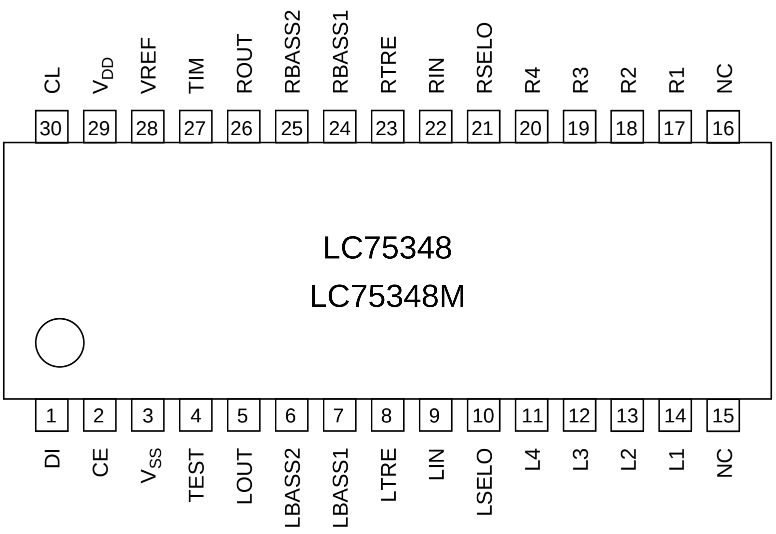
SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions		Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}		11	V
Maximum input voltage	V_{IN} max	All input pins		V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 75°C, Independent IC	LC75348	450	mW
		Ta ≤ 75°C, Mounted on a PCB	LC75348M		
Operating temperature	Topr			–30 to +75	°C
Storage temperature	Tstg			–40 to +125	°C

Pin Assignment



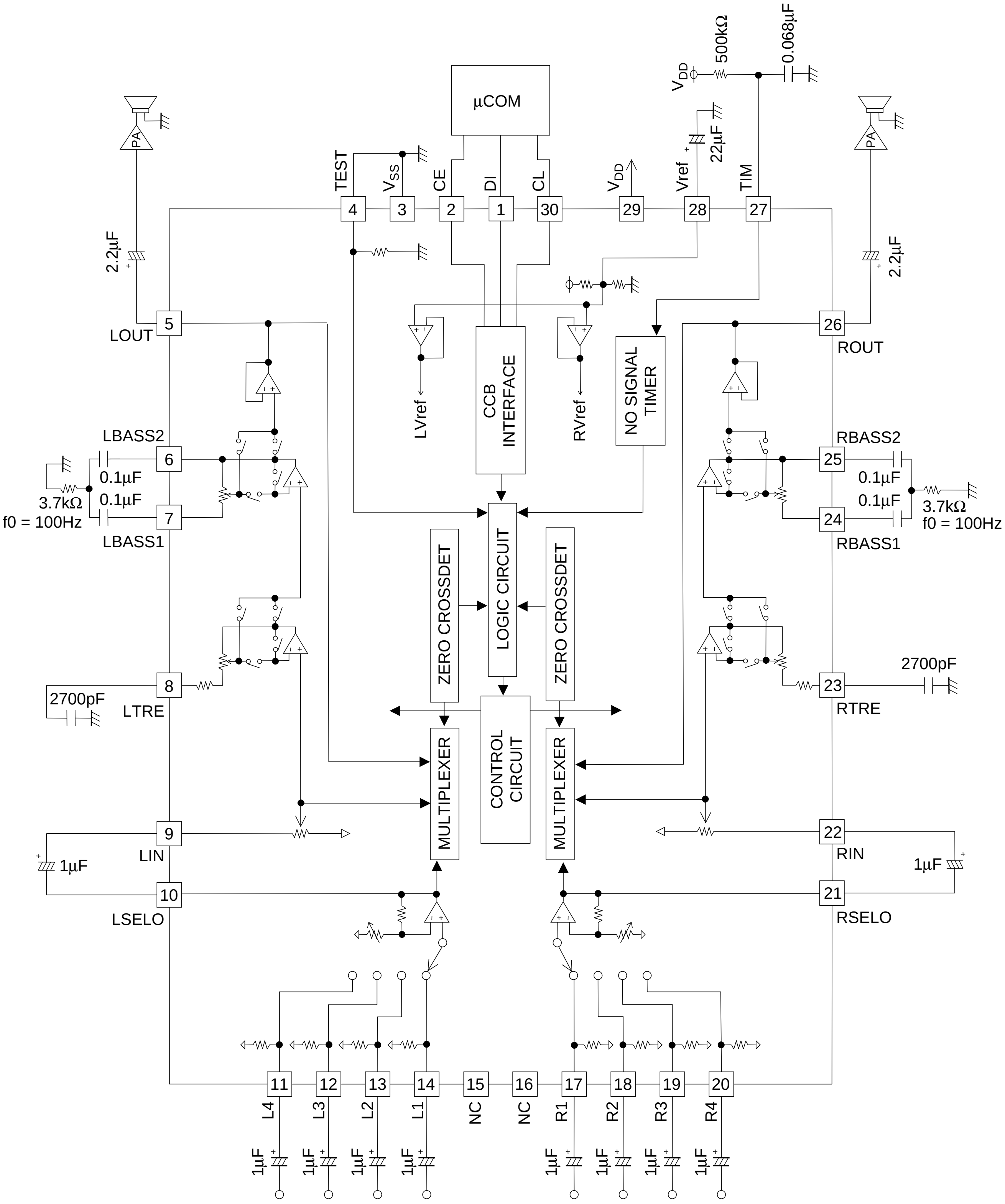
Allowable Operating Ranges at Ta = –30 to +75°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		10	V
High-level input voltage	V_{IH}	CL, DI, CE	2.7		10	V
Low-level input voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CE, DI, CL, L1 to L4, R1 to R4, LIN, RIN	V_{SS}		V_{DD}	Vp-p
Input pulse width	tøW	CL	1			µs
Setup time	tsetup	CL, DI, CE	1			µs
Hold time	thold	CL, DI, CE	1			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 9 V, V_{SS} = 0 V

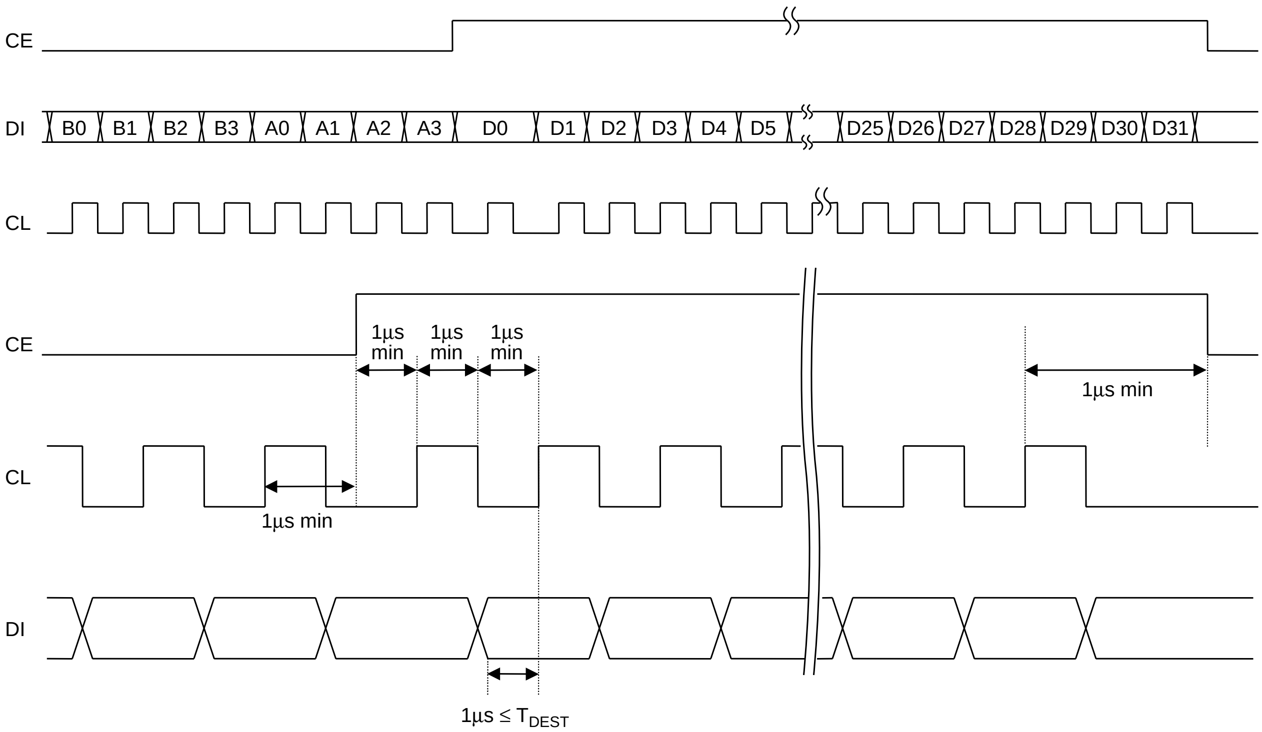
Parameter	Symbol	Pin name	Conditions	Ratings			Unit
				min	typ	max	
[Input Block]							
Maximum input gain	Gin max				30		dB
Step resolution	Gstep				2		dB
Input resistance	Rin	L1, L2, L3, L4, R1, R2, R3, R4			50		kΩ
Clipping level	Vcl	LSELO, RSELO	THD = 1.0%, f = 1 kHz		2.50		Vrms
Output load resistance	Rl	LSELO, RSELO		10			kΩ
[Volume Control Block]							
Input resistance	Rin	LIN, RIN			50		kΩ
Step resolution	Vstep				1		dB
[Treble Band Equalizer Control Block]							
Control range	Geq		max. boost/cut	±8	±10	±12	dB
Step resolution	Estep			1	2	3	dB
Internal feedback resistance	Rfeed				51.7		kΩ
[Bass Band Equalizer Control Block]							
Control range	Geq		max. boost/cut	±18	±20	±22	dB
Step resolution	Estep			1	2	3	dB
Internal feedback resistance	Rfeed				66.6		kΩ
[Overall Characteristics]							
Total harmonic distortion	THD		V_{IN} = 1 Vrms, f = 1 kHz, All controls flat overall			0.01	%
Crosstalk	CT		V_{IN} = 1 Vrms, f = 1 kHz, Rg = 1 kΩ All controls flat overall	80			dB
Output noise voltage	VN		All controls flat overall IHF – A		6		µV
Maximum attenuation	Vomin		All controls flat overall		–80		dB
Current drain	I_{DD}		V_{DD} – V_{SS} = +10 V		40		mA
High-level input current	I_{IH}		CL, DI, CE: V_{IN} = 10 V			10	µA
Low-level input current	I_{IL}		CL, DI, CE: V_{IN} = 0 V	–10			µA

Equivalent Circuit



Control System Timing and Data Format

The stipulated serial data must be input to the CL, DI, and CE pins to control the LC75348 and LC75348M. The data structure has a total of 40 bits, of which 8 bits are address and 32 bits are data.



- Address code (B0 to A3)
  The data has an 8-bit address code, which allows this IC to be used with the SANYO CCB serial bus.

Address code (LSB)

B0	B1	B2	B3	A0	A1	A2	A3
0	1	0	0	0	0	0	1

(82HEX)

- Control code allocation

Input switching control (L1, L2, L3, L4, R1, R2, R3, R4)

D0	D1	D2	D3	Operation
0	0	0	0	L1 (R1) ON
1	0	0	0	L2 (R2) ON
0	1	0	0	L3 (R3) ON
1	1	0	0	L4 (R4) ON

Input gain control

D4	D5	D6	D7	Operation
0	0	0	0	0 dB
1	0	0	0	+2 dB
0	1	0	0	+4 dB
1	1	0	0	+6 dB
0	0	1	0	+8 dB
1	0	1	0	+10 dB
0	1	1	0	+12 dB
1	1	1	0	+14 dB
0	0	0	1	+16 dB
1	0	0	1	+18 dB
0	1	0	1	+20 dB
1	1	0	1	+22 dB
0	0	1	1	+24 dB
1	0	1	1	+26 dB
0	1	1	1	+28 dB
1	1	1	1	+30 dB

Volume control

D8	D9	D10	D11	D12	D13	D14	D15	Operation
0	0	0	0	0	0	0	0	0 dB
1	0	0	0	0	0	0	0	–1 dB
0	1	0	0	0	0	0	0	–2 dB
1	1	0	0	0	0	0	0	–3 dB
0	0	1	0	0	0	0	0	–4 dB
1	0	1	0	0	0	0	0	–5 dB
0	1	1	0	0	0	0	0	–6 dB
1	1	1	0	0	0	0	0	–7 dB
0	0	0	1	0	0	0	0	–8 dB
1	0	0	1	0	0	0	0	–9 dB
0	1	0	1	0	0	0	0	–10 dB
1	1	0	1	0	0	0	0	–11 dB
0	0	1	1	0	0	0	0	–12 dB
1	0	1	1	0	0	0	0	–13 dB
0	1	1	1	0	0	0	0	–14 dB
1	1	1	1	0	0	0	0	–15 dB
0	0	0	0	1	0	0	0	–16 dB
1	0	0	0	1	0	0	0	–17 dB
0	1	0	0	1	0	0	0	–18 dB
1	1	0	0	1	0	0	0	–19 dB
0	0	1	0	1	0	0	0	–20 dB
1	0	1	0	1	0	0	0	–21 dB
0	1	1	0	1	0	0	0	–22 dB
1	1	1	0	1	0	0	0	–23 dB
0	0	0	1	1	0	0	0	–24 dB
1	0	0	1	1	0	0	0	–25 dB
0	1	0	1	1	0	0	0	–26 dB
1	1	0	1	1	0	0	0	–27 dB
0	0	1	1	1	0	0	0	–28 dB
1	0	1	1	1	0	0	0	–29 dB
0	1	1	1	1	0	0	0	–30 dB
1	1	1	1	1	0	0	0	–31 dB
0	0	0	0	0	1	0	0	–32 dB
1	0	0	0	0	1	0	0	–33 dB
0	1	0	0	0	1	0	0	–34 dB
1	1	0	0	0	1	0	0	–35 dB
0	0	1	0	0	1	0	0	–36 dB
1	0	1	0	0	1	0	0	–37 dB
0	1	1	0	0	1	0	0	–38 dB
1	1	1	0	0	1	0	0	–39 dB
0	0	0	1	0	1	0	0	–40 dB
1	0	0	1	0	1	0	0	–41 dB
0	1	0	1	0	1	0	0	–42 dB
1	1	0	1	0	1	0	0	–43 dB
0	0	1	1	0	1	0	0	–44 dB
1	0	1	1	0	1	0	0	–45 dB
0	1	1	1	0	1	0	0	–46 dB
1	1	1	1	0	1	0	0	–47 dB
0	0	0	0	1	1	0	0	–48 dB
1	0	0	0	1	1	0	0	–49 dB
0	1	0	0	1	1	0	0	–50 dB

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D8	D9	D10	D11	D12	D13	D14	D15	Operation
1	1	0	0	1	1	0	0	–51 dB
0	0	1	0	1	1	0	0	–52 dB
1	0	1	0	1	1	0	0	–53 dB
0	1	1	0	1	1	0	0	–54 dB
1	1	1	0	1	1	0	0	–55 dB
0	0	0	1	1	1	0	0	–56 dB
1	0	0	1	1	1	0	0	–57 dB
0	1	0	1	1	1	0	0	–58 dB
1	1	0	1	1	1	0	0	–59 dB
0	0	1	1	1	1	0	0	–60 dB
1	0	1	1	1	1	0	0	–61 dB
0	1	1	1	1	1	0	0	–62 dB
1	1	1	1	1	1	0	0	–63 dB
0	0	0	0	0	0	1	0	–64 dB
1	0	0	0	0	0	1	0	–65 dB
0	1	0	0	0	0	1	0	–66 dB
1	1	0	0	0	0	1	0	–67 dB
0	0	1	0	0	0	1	0	–68 dB
1	0	1	0	0	0	1	0	–69 dB
0	1	1	0	0	0	1	0	–70 dB
1	1	1	0	0	0	1	0	–71 dB
0	0	0	1	0	0	1	0	–72 dB
1	0	0	1	0	0	1	0	–73 dB
0	1	0	1	0	0	1	0	–74 dB
1	1	0	1	0	0	1	0	–75 dB
0	0	1	1	0	0	1	0	–76 dB
1	0	1	1	0	0	1	0	–77 dB
0	1	1	1	0	0	1	0	–78 dB
1	1	1	1	0	0	1	0	–79 dB
0	0	0	0	1	0	1	0	–∞

Treble control

D16	D17	D18	D19	Operation
1	0	1	0	+10 dB
0	0	1	0	+8 dB
1	1	0	0	+6 dB
0	1	0	0	+4 dB
1	0	0	0	+2 dB
0	0	0	0	0 dB
1	0	0	1	–2 dB
0	1	0	1	–4 dB
1	1	0	1	–6 dB
0	0	1	1	–8 dB
1	0	1	1	–10 dB

Bass control

D20	D21	D22	D23	D24	Operation
0	1	0	1	0	+20 dB
1	0	0	1	0	+18 dB
0	0	0	1	0	+16 dB
1	1	1	0	0	+14 dB
0	1	1	0	0	+12 dB
1	0	1	0	0	+10 dB
0	0	1	0	0	+8 dB
1	1	0	0	0	+6 dB
0	1	0	0	0	+4 dB
1	0	0	0	0	+2 dB
0	0	0	0	0	0 dB
1	0	0	0	1	–2 dB
0	1	0	0	1	–4 dB
1	1	0	0	1	–6 dB
0	0	1	0	1	–8 dB
1	0	1	0	1	–10 dB
0	1	1	0	1	–12 dB
1	1	1	0	1	–14 dB
0	0	0	1	1	–16 dB
1	0	0	1	1	–18 dB
0	1	0	1	1	–20 dB

Zero cross control

D25	Operation
0	Data is written according to zero cross detection.
1	Zero cross detection operation is stopped. (Data is acquired on the falling edge of the CE signal.)

Channel selection

D26	D27	Operation
0	0	
1	0	RCH
0	1	LCH
1	1	Left and right channels at the same time

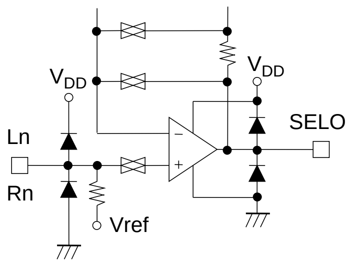
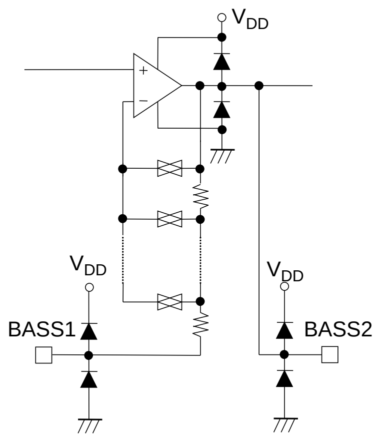
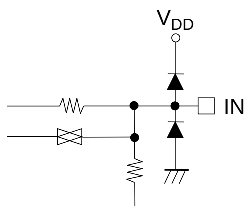
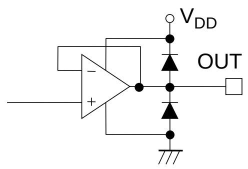
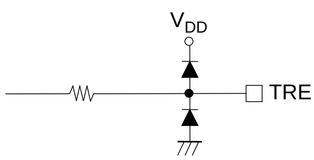
Zero cross signal detection block control

D28	D29	Operation
0	0	Selector
1	0	Volume
0	1	Tone

Test mode

D30	D31	Operation
0	0	
These bits select the IC test modes and must be set to 0 during normal operation.		

Pin Functions

Pin No.	Pin	Function	Notes
14 13 12 11 17 18 19 20	L1 L2 L3 L4 R1 R2 R3 R4	• Audio signal inputs	
10 21	LSELO RSELO	• Input selector outputs	
7 6 24 25	LBASS1 LBASS2 RBASS1 RBASS2	• Connections for the capacitors and resistors that form the bass band filters	
9 22	LIN RIN	• Volume and equalizer inputs	
5 26	LOUT ROUT	• Volume and equalizer outputs	
8 23	LTRE RTRE	• Connections for the capacitors that form the treble band filters	

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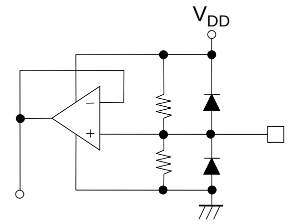
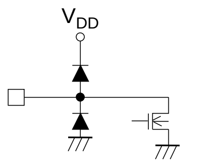
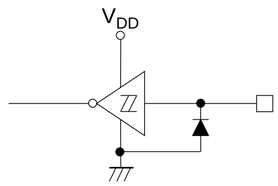
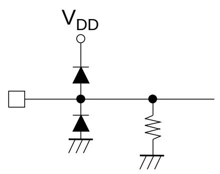
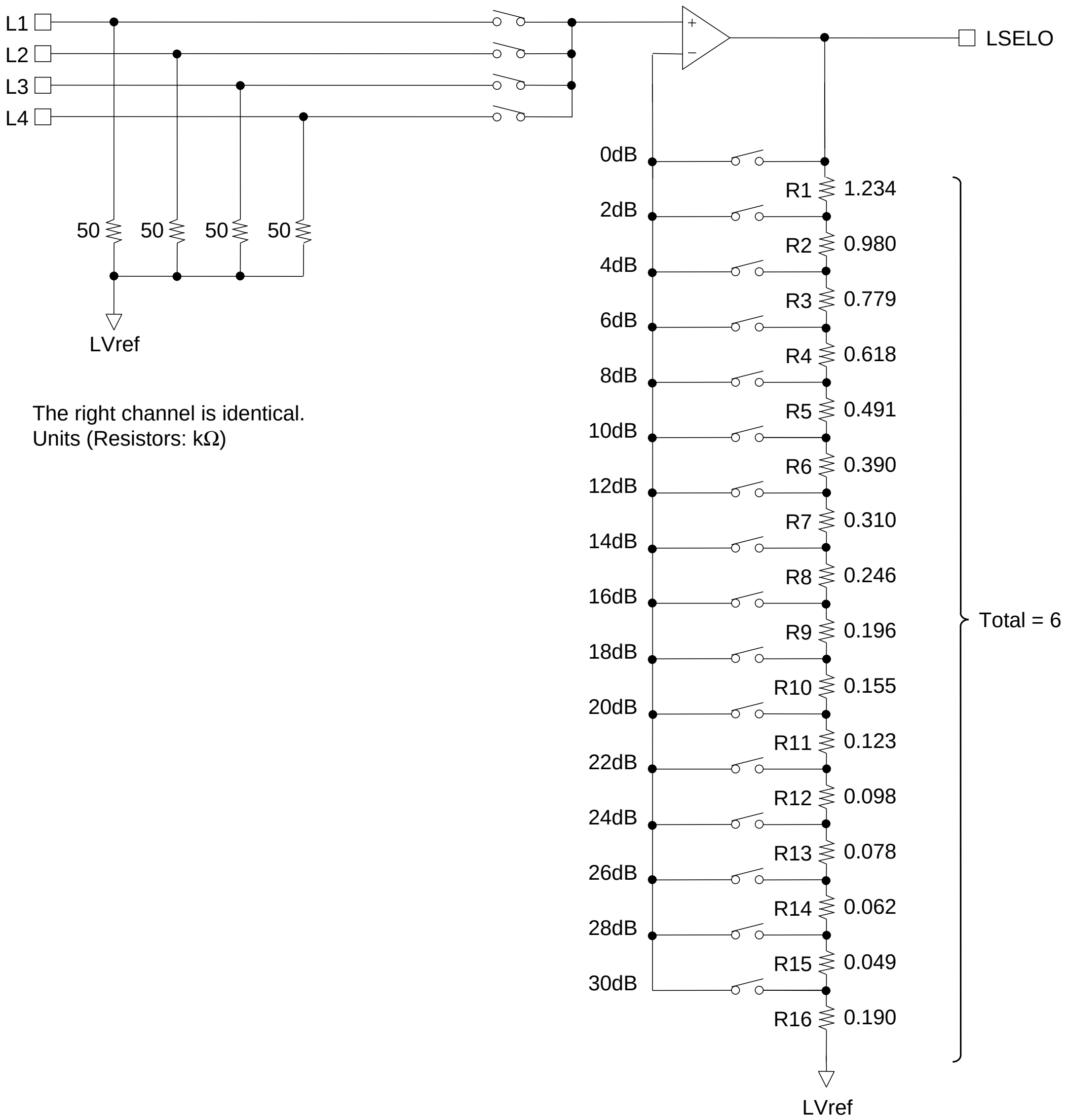
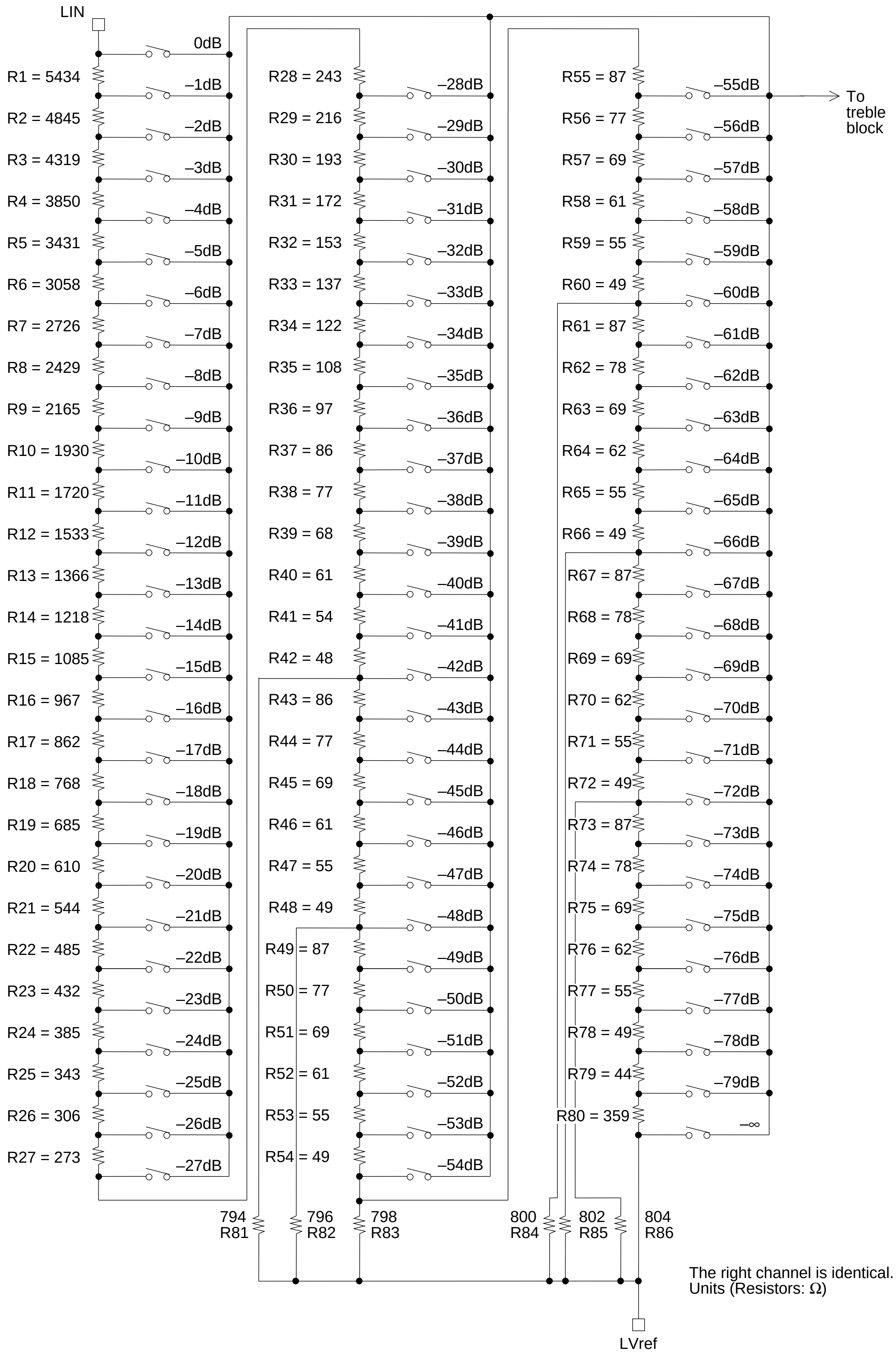
Pin No.	Pin	Function	Notes
28	Vref	• 1/2 V_{DD} voltage generator used for the analog system ground A capacitor of about 10 µF must be connected between Vref and AV_{SS} (V_{SS}) to minimize power supply ripple.	
3	V_{SS}	• Ground	
29	V_{DD}	• Power supply	
27	TIM	• Time setting for the zero cross circuit no signal state time. If no zero cross is recognized between the time the data is stored and the time this timer completes, the data is acquired forcibly.	
2	CE	• Chip enable Data is written to the internal latch and the analog switches operate when this pin goes from high to low. Data transfers are enabled when this pin is high.	
1 30	DI CL	• Inputs for the clock and serial data signals used to control this IC	
4	TEST	• Electronic volume control test pin. This pin must be tied to the V_{SS} level.	
15 16	NC	• Unused (no connection) pins. These pins must be either left open or tied to V_{SS}.	

Internal Equivalent Circuits

• Selector Block Equivalent Circuit

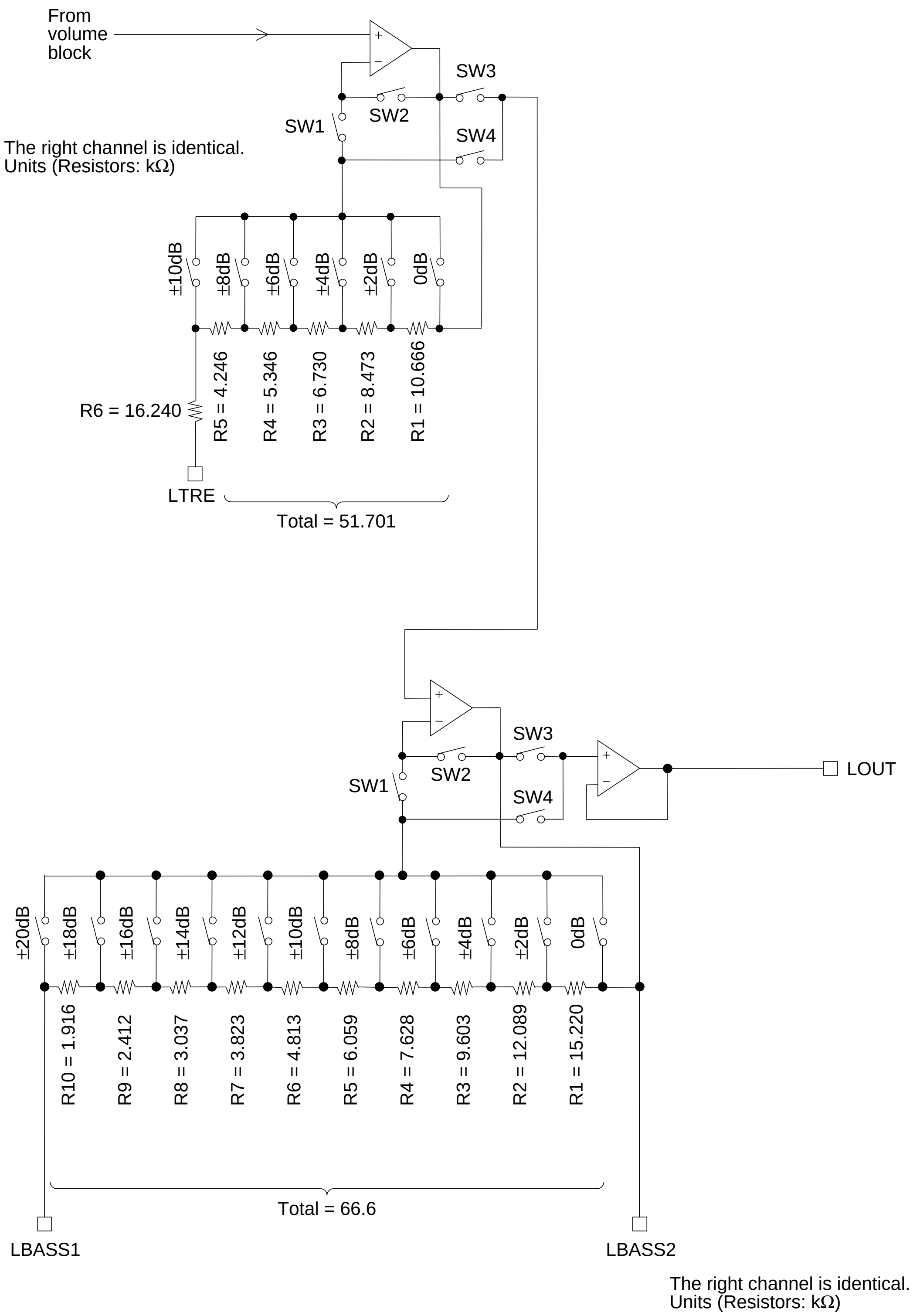


• Volume Control Block Internal Equivalent Circuit



The right channel is identical.
Units (Resistors: Ω)

• Treble/Bass Band Block Internal Equivalent Circuit

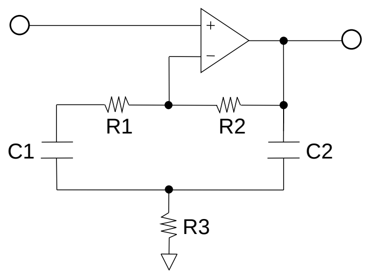


For boost, switches SW1 and SW3 are on, and for cut, switches SW2 and SW4 are on.
For 0 dB, the 0dBSW, SW2, and SW3 are on.

Bass Band Circuit

This section presents the equivalent circuit and the formulas for calculating the R and C values for a 100 Hz center frequency.

- Bass band equivalent circuit



- Sample calculation
  Specifications: Center frequency: f0 = 100 Hz
  Gain at maximum boost: G = 20 dB
  Assume R1 = 0, R2 = 66.6 kΩ, and C1 = C2 = C.

(1) Determine R3 from the G = 20 dB condition.

$$G_{+20dB} = 20 \times LOG_{10}\left(1 + \frac{R2}{2R3}\right)$$

$$R3 = \frac{R2}{2\left(10^{G+20dB/20} - 1\right)} = \frac{66000}{2 \times (10 - 1)} \cong 3.7k\Omega$$

(2) Determine C from the center frequency f0 = 100 Hz condition

$$f0 = \frac{1}{2\pi\sqrt{R3R2C1C2}}$$

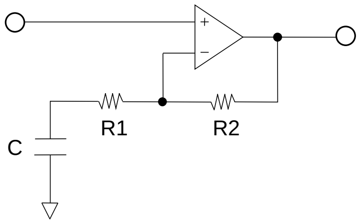
$$C = \frac{1}{2\pi f0\sqrt{R3R2}} = \frac{1}{2\pi \times 100\sqrt{66000 \times 3700}} \cong 0.1\mu F$$

(3) Determine Q

$$Q = \frac{R3R2}{2R3} \cdot \frac{1}{\sqrt{R3R2}} \cong 2.1$$

Treble Band Circuit

The treble band circuit can provide shelving characteristics.
This section presents the equivalent circuit for boost operation and the calculation formulas.



- Sample calculation
  Specifications: Set frequency: f = 26,000 Hz
  Gain at maximum boost: $G_{+10\ dB}$ = 10 dB
  Assume R1 = 16.240 KΩ, and R2 = 35.461 KΩ.

  The constants mentioned above are calculated as follows.

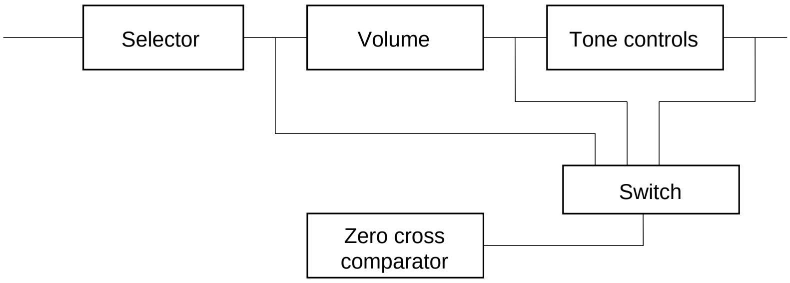
$$G = 20 \times LOG_{10}\left(1 + \frac{R2}{\sqrt{R1^2 + (1/\omega C)^2}}\right)$$

$$C = \frac{1}{2\pi f\sqrt{\left(\frac{R2}{10^{G/20} - 1}\right)^2 - R1^2}}$$

$$= \frac{1}{2\pi 26000\sqrt{\left(\frac{35461}{3.16 - 1}\right)^2 - 16240^2}} \cong 2700(pF)$$

Usage Notes

- The internal transistor states are undefined when power is first applied. Applications must mute the output until control data has been written to the IC.
- Operational description of the zero cross switching circuit
  The LC75348 and LC75348M provide a function that can switch the zero cross comparator signal detection point, allowing applications to select an optimal detection point for the block whose data is being updated. Basically, switching noise can be minimized if the signal immediately following the block whose data is updated is input to the zero cross comparator. This means that the detection point must be switched each time data is updated.



LC75348 and LC75348M Zero Cross Detection Circuit

- Zero cross switching control procedure
  The zero cross switching control procedure consists of three steps. First, set the zero cross control bit to zero cross detection mode (D25 = 0), then specify the block for detection (with bits D28 and D29), and finally transfer the data. Since these control bits are latched first, immediately after the data is transferred, i.e. on the CE falling edge, the mode can be set in a single data transfer operation when updating the volume control or other control block data. The figure below presents an example of the control used when updating the volume control block data.

D25	D28	D29
0	1	0

Zero cross detection mode setting (D25) — Volume control block setting (D28, D29)

- Zero cross timer setting

  If the input signal is lower than the zero cross comparator detection sensitivity, or if a low-frequency signal is input, the state in which the circuit cannot detect a zero cross may continue and the input data will not be latched during that period.

  The zero cross timer sets a time for the data to be latched forcibly in states such as this where a zero cross cannot be detected.

  For example, to set a 25 ms time:

  T = 0.69 CR

  Assume C = 0.068 µF. The R will be:

  $$R = \frac{25 \times 10^{-3}}{0.69 \times 0.068 \times 10^{-6}} \approx 530\ k\Omega$$

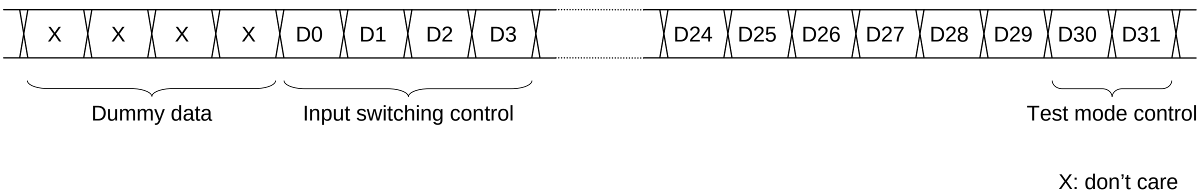
  Normally, a time in the range 10 to 50 ms is used.

- Notes on serial data transfer

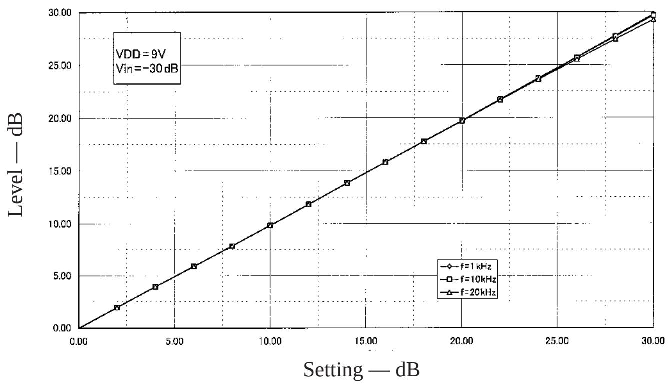
  (1) Cover the CL, DI, and CE signal lines with the ground pattern or use shielded lines to prevent the high-frequency digital signals carried by these lines from entering the analog signal system.

  (2) The LC75348 and LC75348M data format consists of 8 bits of address and 32 bits of data. When transmitting data as an even multiple of 8 bits (when transferring 36 bits of data), use the data format shown below.

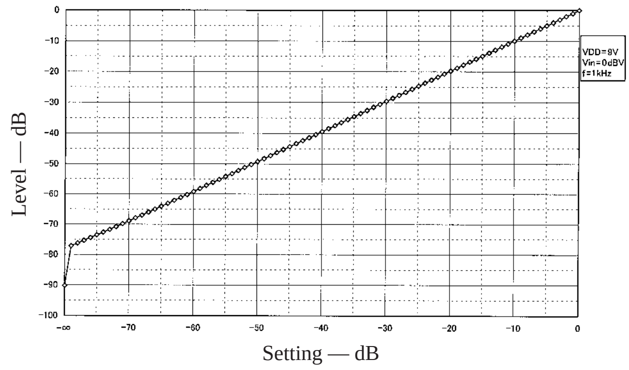
LC75348 and LC75348M Data Reception in Multiples of 8 Bits



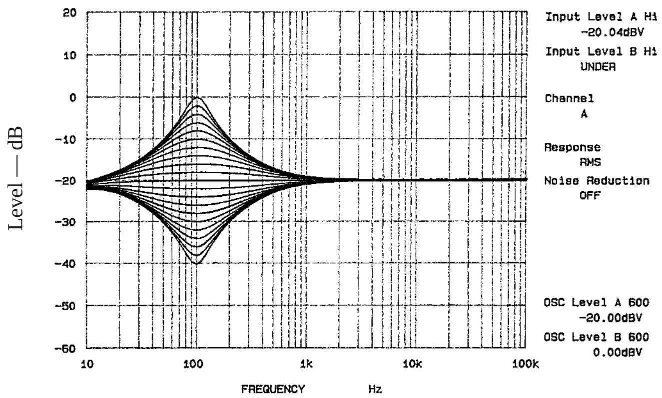
Input Gain Characteristics



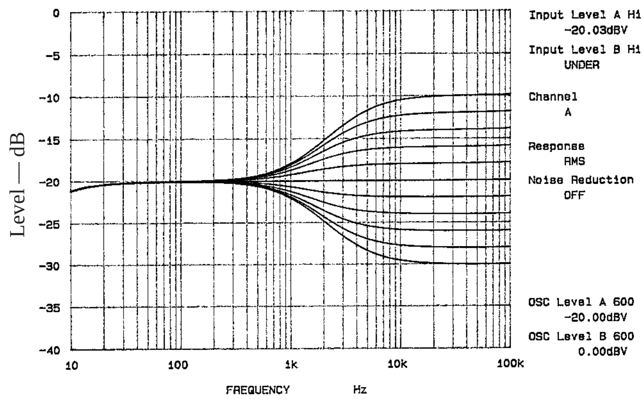
Volume Characteristics



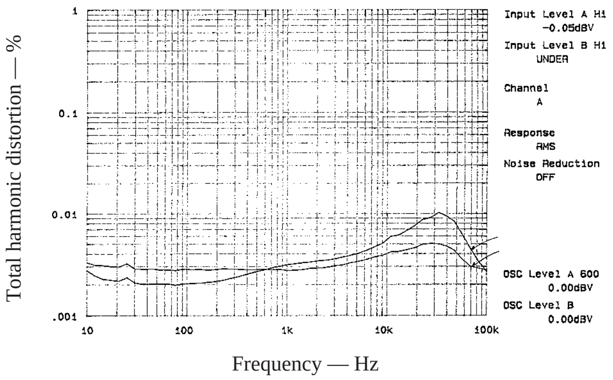
Bass Characteristics



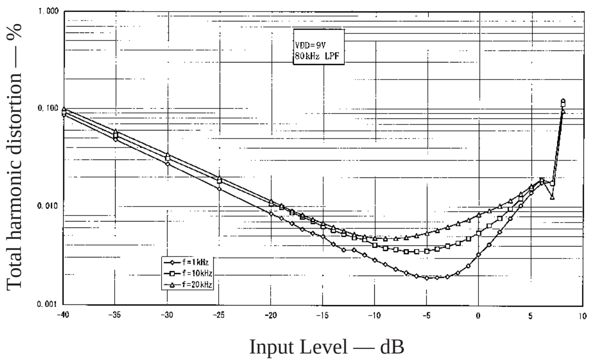
Treble Characteristics



THD – Frequency Characteristics



THD – Input Level Characteristics



THD – Supply Voltage Characteristics