

Leaded Varistors

HICAP; SHCV Series

Construction

- Combination of a multilayer ceramic capacitor and a multilayer varistor, leaded
- Coating: epoxy resin, flame-retardant to UL 94 V-0
- Terminals: tinned iron wire

Features

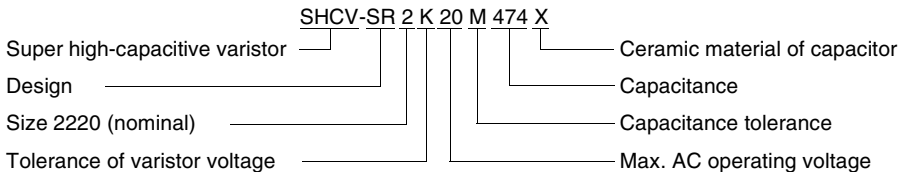
- High capacitance (up to 4,7 μF)
- Overvoltage protection and RFI suppression provided by a single component
- Load-dump withstand capability
- Jump-start strength
- PSpice models

Taping

- Upon request

Type designation

Detailed description of coding system on page 39, chapter "General Technical Information"



General technical data

Climatic category	X ¹⁾	40/85/56	in accordance with IEC 60068-1
	Z ²⁾	25/85/56	
LCT	X	– 40 °C	
	Z	– 25 °C	
UCT	X	+ 85 °C	in accordance with IEC 60068-2-3
	Z	+ 85 °C	
Damp heat, steady state (93 % r.h., 40 °C)		56 days	
Operating temperature (full load)	X	– 40 ... + 85 °C	in accordance with CECC 42 000
	Z	– 25 ... + 85 °C	
Storage temperature	X	– 40 ... + 125 °C	
	Z	– 25 ... + 85 °C	
Electric strength		≥ 1,0 kV _{RMS}	in accordance with CECC 42 000
Insulation resistance		≥ 1,0 GΩ	in accordance with CECC 42 000
Response time		< 25 ns	

1) Ceramic material: X = X7R

2) Ceramic material: Z = Z5U



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Maximum ratings ($T_A = 85\text{ }^{\circ}\text{C}$)

Type (untaped)	Ordering code	V_{RMS}	V_{DC}	i_{max} 8/20 μs	W_{max} (2 ms)	P_{max}	W_{LD} (10x)
SHCV-		V	V	A	J	W	J
SR1S14BM474X	B72587E3140S200	14	16	800	2,4	0,015	6
SR2S14BM474X	B72547E3140S200	14	16	1200	5,8	0,030	12
SR1S14BM105Z	B72588G3140S200	14	16	800	2,4	0,015	6
SR1S14BM155Z	B72588H3140S200	14	16	800	2,4	0,015	6
SR2S14BM105Z	B72548G3140S200	14	16	1200	5,8	0,030	12
SR2S14BM155Z	B72548H3140S200	14	16	1200	5,8	0,030	12
SR2S14BM475Z	B72548L3140S200	14	16	1200	5,8	0,030	12
SR1K20M474X	B72587E3200K000	20	26	800	3,0	0,015	6
SR2K20M474X	B72547E3200K000	20	26	1200	7,8	0,030	12
SR1K20M105Z	B72588G3200K000	20	26	800	3,0	0,015	6
SR1K20M155Z	B72588H3200K000	20	26	800	3,0	0,015	6
SR1K20M225Z	B72588J3200K000	20	26	800	3,0	0,015	6
SR2K20M105Z	B72548G3200K000	20	26	1200	7,8	0,030	12
SR2K20M155Z	B72548H3200K000	20	26	1200	7,8	0,030	12

Characteristics ($T_A = 25\text{ }^{\circ}\text{C}$)

Type (untaped)	V_{Jump} (5 min)	V_v (1 mA)	ΔV_v (1 mA)	Max. clamping voltage		$C \pm 20\%$ (1 kHz)	Derating curve	V/I char- acteristic
				v V	i A			
SHCV-	V	V	%	V	A	$\mu\text{F}^1)$	Page	Page
SR1S14BM474X	24,5	22	+ 23/- 0	40	5,0	0,47	244	272
SR2S14BM474X	24,5	22	+ 23/- 0	40	10,0	0,47	245	272
SR1S14BM105Z	24,5	22	+ 23/- 0	40	5,0	1,00	244	272
SR1S14BM155Z	24,5	22	+ 23/- 0	40	5,0	1,50	244	272
SR2S14BM105Z	24,5	22	+ 23/- 0	40	10,0	1,00	245	272
SR2S14BM155Z	24,5	22	+ 23/- 0	40	10,0	1,50	245	272
SR2S14BM475Z	24,5	22	+ 23/- 0	40	10,0	4,70	245	272
SR1K20M474X	26,0	33	± 10	58	5,0	0,47	244	270
SR2K20M474X	26,0	33	± 10	58	10,0	0,47	245	271
SR1K20M105Z	26,0	33	± 10	58	5,0	1,00	244	270
SR1K20M155Z	26,0	33	± 10	58	5,0	1,50	244	270
SR1K20M225Z	26,0	33	± 10	58	5,0	2,20	244	270
SR2K20M105Z	26,0	33	± 10	58	10,0	1,00	245	271
SR2K20M155Z	26,0	33	± 10	58	10,0	1,50	245	271

1) at 0,5 V

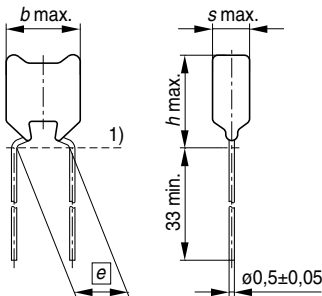


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Notes

- If the maximum loads specified for load dump and jump start are fully utilized, subsequent polarity reversal of the AUTO varistors are inadmissible.
- If the load remains under the maximum ratings, polarity reversal may be admissible. Contact EPCOS for consultancy on this kind of problem.
- Load dump or jump start can decrease the varistor voltage in load direction by max. 15 %.
- Load dump: min. time of energy input 40 ms, interval 60 s.



$e = 5,0 \pm 1$

Offset = $0,0 \pm 1$

1) Seating plane according to IEC 60717

VAR0394B

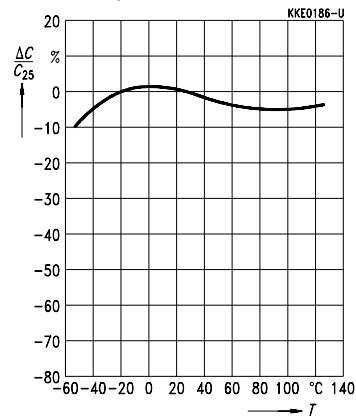
Weight:
approx. 1 g

Dimensions

Type	$b_{\max}$ mm	$s_{\max}$ mm	$h_{\max}$ mm
SHCV-SR1 ... 474X	7,3	3,7	7,8
SHCV-SR1 ... 105Z	7,3	3,7	7,8
SHCV-SR1 ... 155Z	7,3	3,7	7,8
SHCV-SR1 ... 225Z	7,3	4,1	7,8
SHCV-SR2 ... 474X	7,8	3,6	9,0
SHCV-SR2 ... 105Z	7,8	4,1	9,0
SHCV-SR2 ... 155Z	7,8	4,1	9,0
SHCV-SR2 ... 475Z	7,8	4,1	9,0

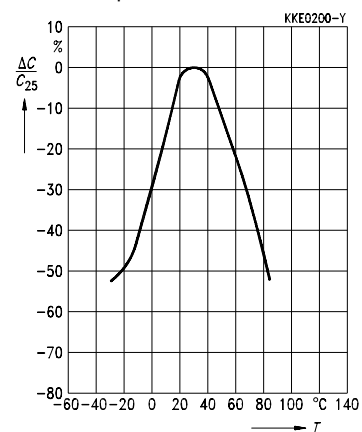
Typical characteristics of X7R-MLCC²⁾

Capacitance change $\Delta C/C_{25}$
versus temperature T



Typical characteristics of Z5U-MLCC²⁾

Capacitance change $\Delta C/C_{25}$
versus temperature T



2) MLCC: Multilayer chip capacitors

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