QLogic Corporation

FAS566 Fast Architecture SCSI Processor

Data Sheet

Features Summary

- Compliance with *Information Technology – Small Computer System Interface*, X3.131-1994 (SCSI-2)
- Compliance with *SCSI Parallel Interface* (SCSI-3), X3T10-855D (SCAM)
- Compliance with *Information Technology – Small Computer System Interface*, X3T10/1071D (Fast-20)
- Compliance with *Information Technology – SCSI Parallel Interface-2* (SPI-2), X3T10/1142D (Fast-40)
- Compliance with *Information Technology – SCSI Parallel Interface-3* (SPI-3), X3T10/1302D (Fast-80)
- SCSI synchronous data transfer rates up to:
  - ❒ 160 Mbytes/sec (wide, 16-bit Fast-80)
  - ❒ 80 Mbytes/sec (wide, 16-bit Fast-40)
  - ❒ 40 Mbytes/sec (narrow, eight-bit Fast-40)
- On-chip low voltage differential (LVD) drivers
- Versatile 40 million instructions per second (MIP) microcontroller
- Programmable microcontroller to automate SCSI protocol handling
- Programmable filtering on select SCSI signals
- Programmable slew-rate control
- Supports initiator and target modes
- DMA interface with late transfer tolerant design that provides 160 Mbytes/sec sustained transfers
- Buffer controller for external SRAM
- Expanded 128-word DMA FIFO
- On-chip phase lock loop (PLL) for high frequency clock synthesis

Product Description

The FAS566 device incorporates an enhanced high-performance SCSI engine derived from the triple embedded controller (TEC) family (see figure 1).

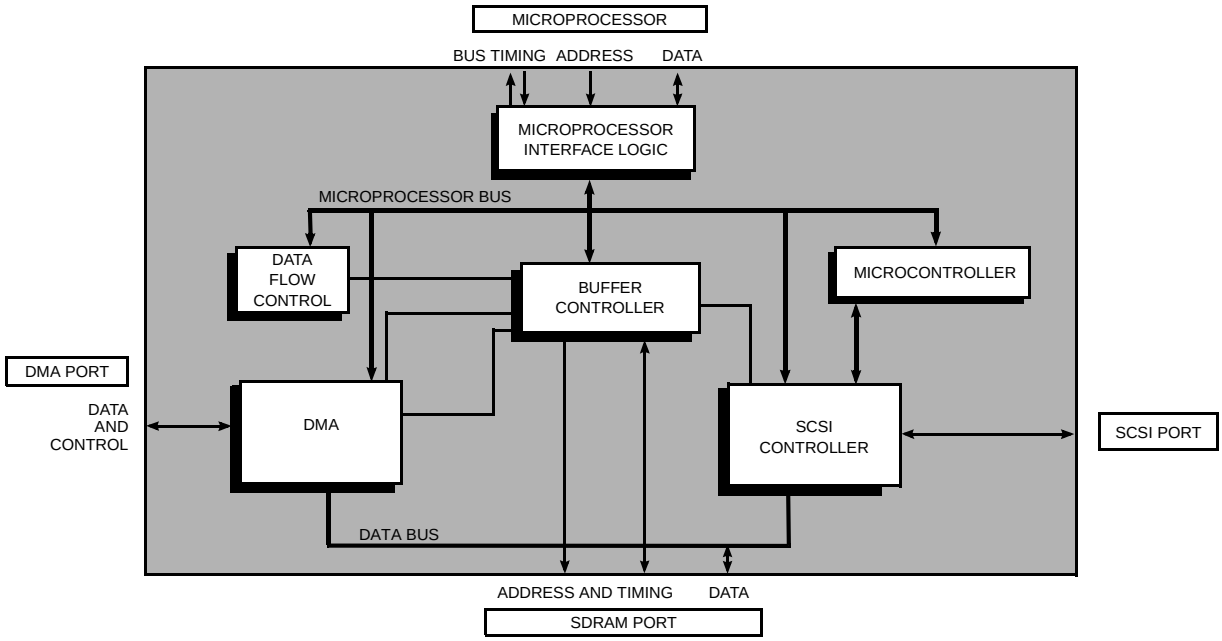

Figure 1. FAS566 Block Diagram

The FAS566 provides Fast-80 SCSI synchronous transfer rates. The highly integrated SCSI core provides advanced SCAM level 1 and level 2 support. The core includes a microcontroller to provide the user with a flexible, programmable means to coordinate SCSI sequences.

SCSI Controller

The following list highlights the FAS566 SCSI controller features.

- Asynchronous data transfers greater than 5 Mtransfers/sec
- Synchronous data transfers (5 Mtransfers/sec)
- Fast synchronous data transfers (10 Mtransfers/sec)
- Fast-20 synchronous data transfers (20 Mtransfers/sec)
- Fast-40 synchronous data transfers (40 Mtransfers/sec)
- Fast-80 synchronous data transfers (80 Mtransfers/sec)
- 8-bit (narrow) and 16-bit (wide) SCSI bus widths
- SCAM levels 1 and 2

The SCSI controller provides powerful and flexible low-level hardware assistance for SCSI protocol handling. The FAS566 microcontroller, SCSI FIFO, and SCSI controller perform frequently used SCSI operations with low firmware overhead at performance levels ranging from asynchronous SCSI to Fast-80.

The core of the FAS566 SCSI processor, with enhanced initiator support, is derived from the proven TEC480 SCSI disk controller.

Microcontroller

The following list highlights the FAS566 SCSI microcontroller features.

- Maximum 40 MIPS with a 25-ns instruction cycle (except for branch)
- 64 single-word instructions
- 16-bit wide instructions
- Eight-bit wide data path
- 1024x16 static random access memory (SRAM) program memory
- 16x8 dual-port, general purpose registers; 32 mailbox registers
- Five-level deep hardware stack
- Direct, indirect, and absolute addressing modes
- Two firmware interrupt sources
- Two hardware interrupts; one with four-bit, automatic interrupt vector and status
- Full chip access through the microprocessor bus

The FAS566 provides a microcontroller with separate program and data memory. The result is improved bandwidth over traditional Von Neuman architecture where program and data share the same memory. Separating program and data memory allows independent widths for instruction and data. All instructions are 16 bit wide, single word.

The four operations for each instruction cycle are fetch, decode, execute, and write back. A three-stage pipeline allows overlaps between fetch and write-back cycles with decode and execute cycles. Consequently, all instructions execute in one instruction cycle or two clock periods (25 ns at 80 MHz) except for program branches, which require two instruction cycles.

The microcontroller is composed of a 1024x16 program memory, a 32x8 register file, a 5x8 stack, an integer ALU, 32 mailbox registers, and other special purpose registers. The microcontroller has direct access to addresses in the register files or in data memory. The first 16 bytes of the external SCSI FIFO is mapped directly into data memory locations 90h-9Fh. The microcontroller can monitor the FIFO contents (one byte at a time) without removing it. The microcontroller accesses external registers through the external access read (EARD) instruction or the external access write (EAWR) instruction.

Buffer Controller

The FAS566 buffer management is provided by a multiple-channel, high-speed, bursting DMA controller. The buffer controller connects the buffer SDRAM to the disk channel, SCSI channel, and the microprocessor bus. The buffer controller regulates all data movement into and out of SDRAM buffer memory. Each DMA channel supports DMA bursting to maintain optimal bandwidth. The DMA, microprocessor, and SCSI channels each have a FIFO. Each DMA channel has associated control, configuration, and buffer memory address registers.

The buffer controller also provides round-robin arbitration for the buffer resource, a four-byte buffer cyclical redundancy check (BCRC), Data Flow control, and automatic SDRAM refresh control.

The buffer controller table search tool compares 16 or 32 bit-based tables of numbers, such as an LBA, to provide high-speed lookups for cache, zone, defect, and other system searches.

To support the SCSI-3 RAID commands in the FAS566, an exclusive or (XOR) engine running at DMA speeds generates an XOR of two data buffers.

DMA Interface

The FAS566 has an improved DMA interface with an expanded 128-word FIFO that provides transfer rates up to 160 Mbytes/sec. The FAS566 supports 16-bit wide data strobe transfers of up to 80 MHz with 160 Mbytes/sec data throughput. The internal FIFO provides programmable threshold logic for determining FIFO full and empty conditions.

Microprocessor Interface

The FAS566 microprocessor interface provides the interface between the internal modules (SCSI controller, FIFO, microcontroller, and DMA engine) and an external microprocessor.

Interfaces

The FAS566 interfaces consist of SCSI, microprocessor, DMA, buffer controller, and differential mode support. Pins that support these interfaces and other chip operations are shown in figure 2.

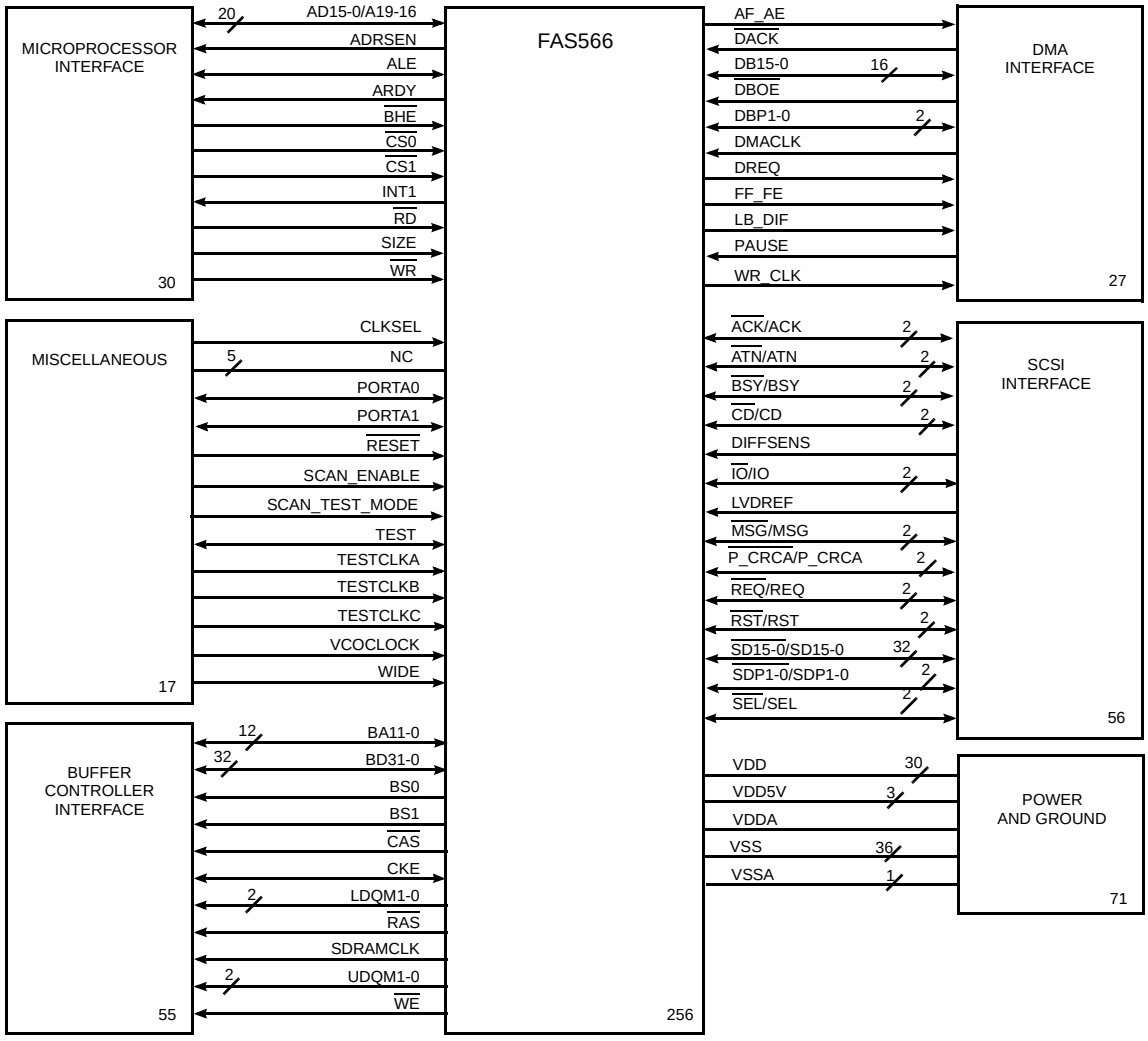

Figure 2. FAS566 Functional Signal Grouping

Specifications are subject to change without notice.

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