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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK3233

Silicon N Channel MOS FET High Speed Power Switching

RENESAS

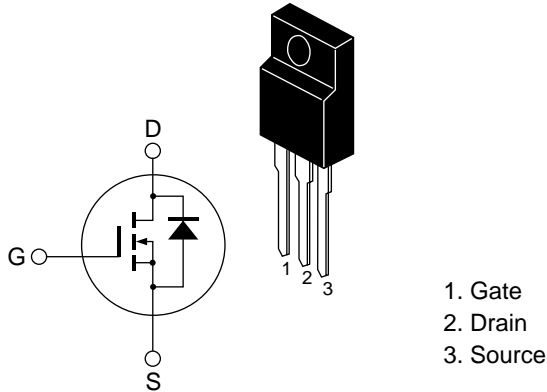
ADE-208-1369 (Z)
1st. Edition
Mar. 2001

Features

- Low on-resistance: $R_{DS(on)} = 1.1 \Omega$ typ.
- Low leakage current: $IDSS = 1 \mu A$ max (at $V_{DS} = 500 V$)
- High speed switching: $t_f = 15 ns$ typ (at $V_{GS} = 10 V$, $V_{DD} = 250 V$, $I_D = 2.5 A$)
- Low gate charge: $Q_g = 15 nC$ typ (at $V_{DD} = 400 V$, $V_{GS} = 10 V$, $I_D = 5 A$)
- Avalanche ratings

Outline

TO-220CFM



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	5	A
Drain peak current	$I_{D (pulse)}^{Note1}$	20	A
Body-drain diode reverse drain current	I_{DR}	5	A
Body-drain diode reverse drain peak current	$I_{DR (pulse)}^{Note1}$	20	A
Avalanche current	I_{AP}^{Note3}	5	A
Channel dissipation	P_{ch}^{Note2}	30	W
Channel to case Thermal Impedance	θ_{ch-c}	4.17	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. Value at $T_c = 25^\circ C$

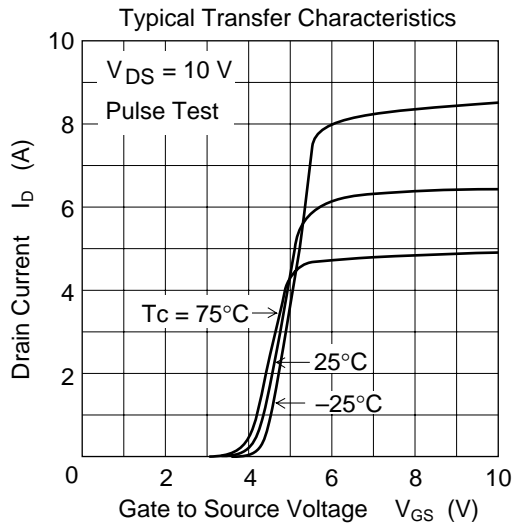
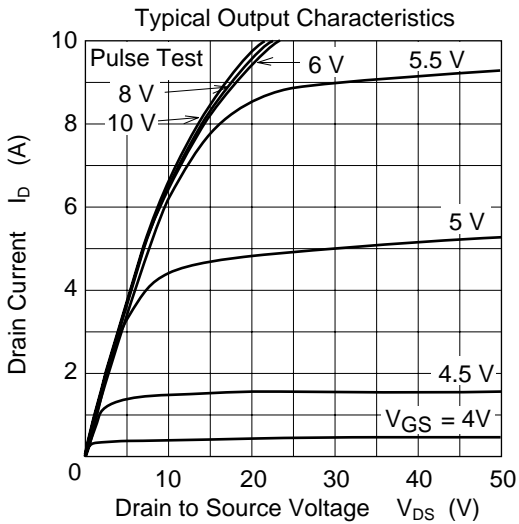
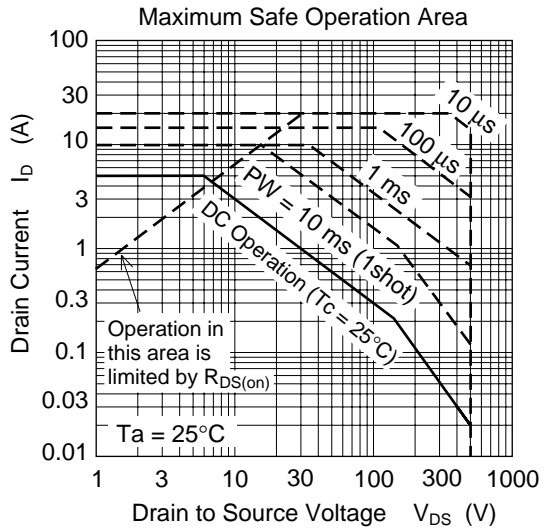
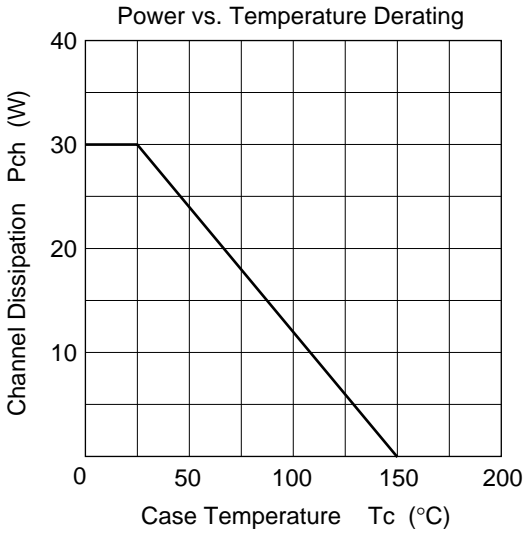
3. $T_{ch} \leq 150^\circ C$

Electrical Characteristics (Ta = 25°C)

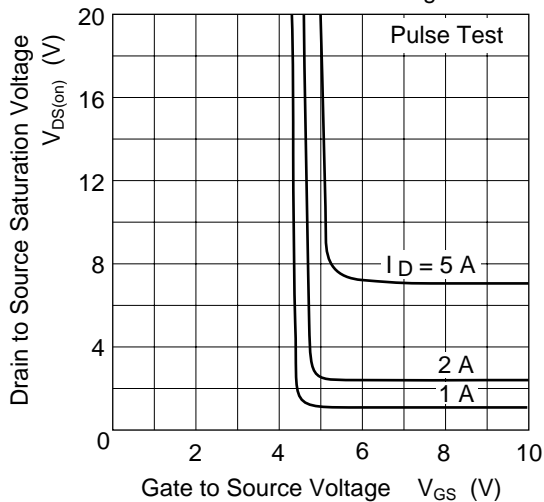
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.0	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.1	1.5	Ω	$I_D = 2.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	3.0	4.5	—	S	$I_D = 2.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	580	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	70	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	13	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$I_D = 2.5 \text{ A}$
Rise time	t_r	—	15	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	65	—	ns	$R_L = 100 \Omega$
Fall time	t_f	—	15	—	ns	$R_g = 10 \Omega$
Total gate charge	Q_g	—	15	—	nC	$V_{DD} = 400 \text{ V}$
Gate to source charge	Q_{gs}	—	3	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	8	—	nC	$I_D = 5 \text{ A}$
Body-drain diode forward voltage	V_{DF}	—	0.85	1.3	V	$I_F = 5 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	400	—	ns	$I_F = 5 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery charge	Q_{rr}	—	1.5	—	μC	$diF/dt = 100 \text{ A}/\mu\text{s}$

Note: 4. Pulse test

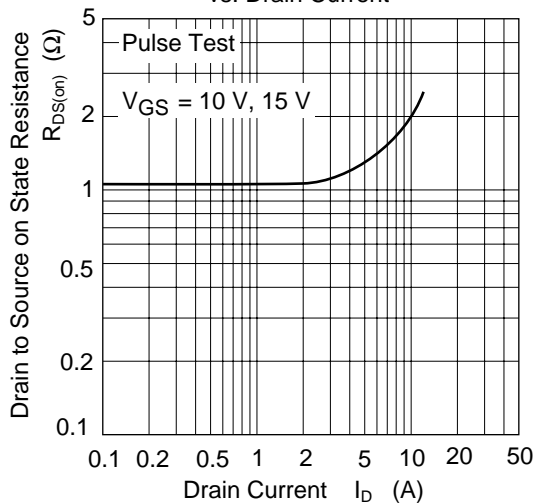
Main Characteristics



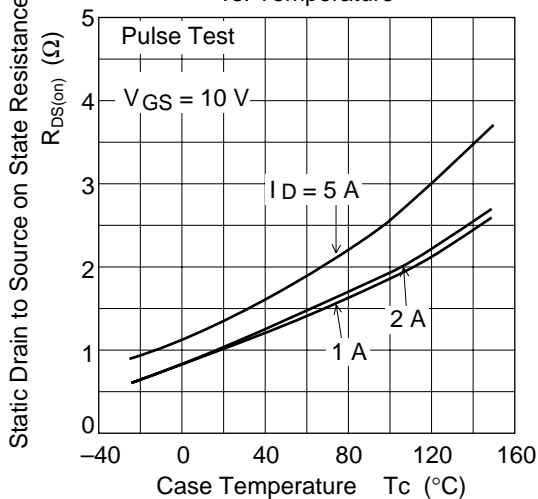
Drain to Source Saturation Voltage vs. Gate to Source Voltage



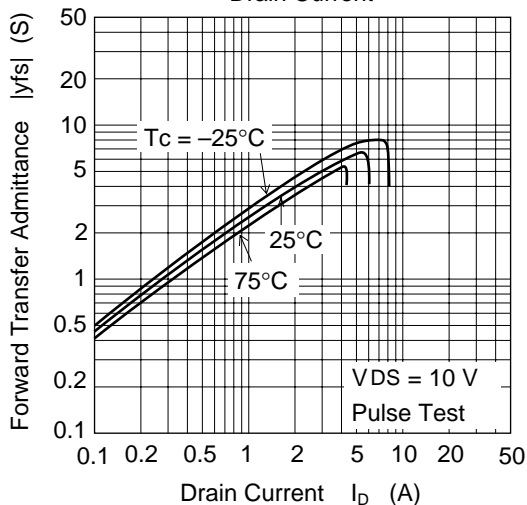
Static Drain to Source on State Resistance vs. Drain Current



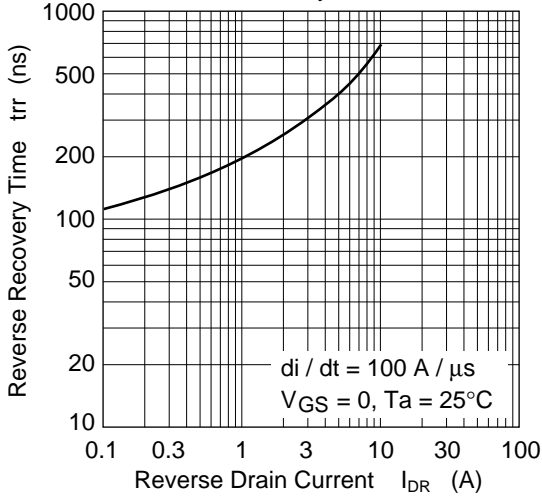
Static Drain to Source on State Resistance vs. Temperature



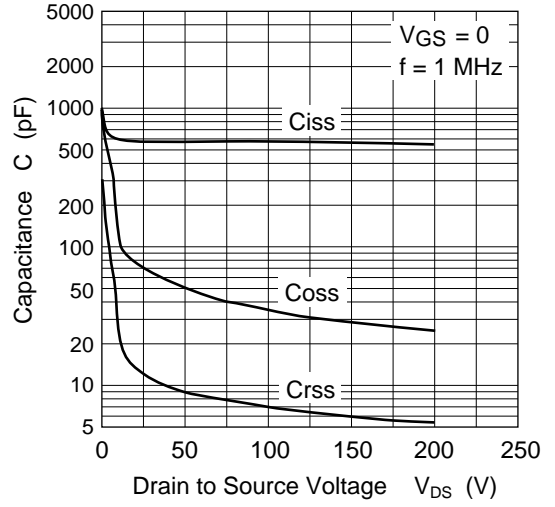
Forward Transfer Admittance vs. Drain Current



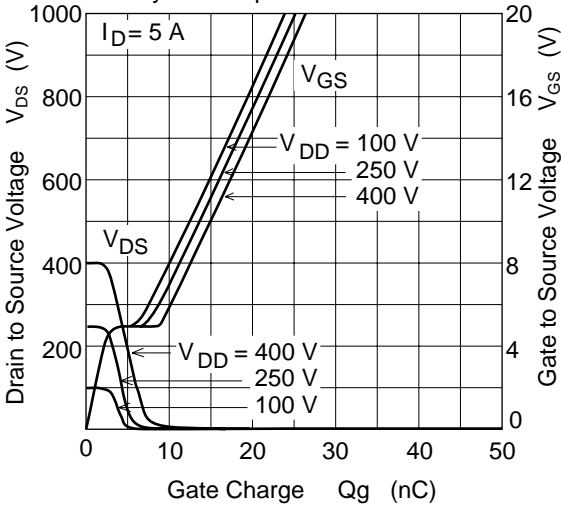
Body-Drain Diode Reverse Recovery Time



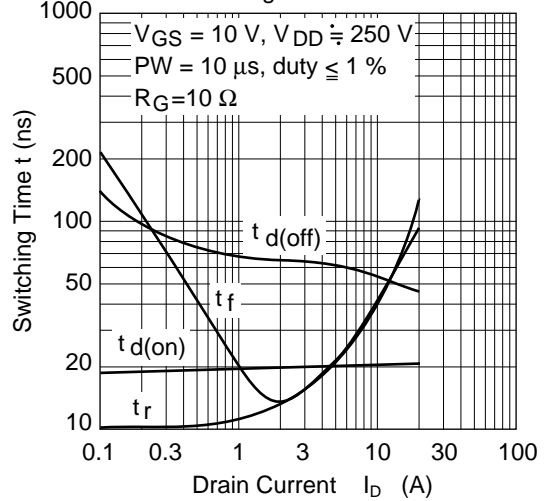
Typical Capacitance vs. Drain to Source Voltage

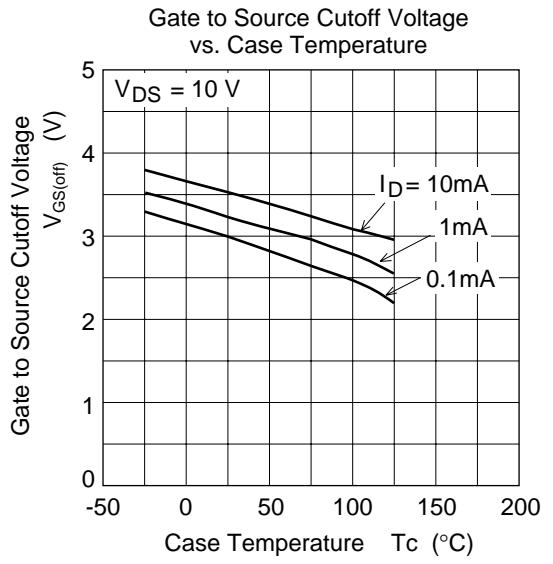
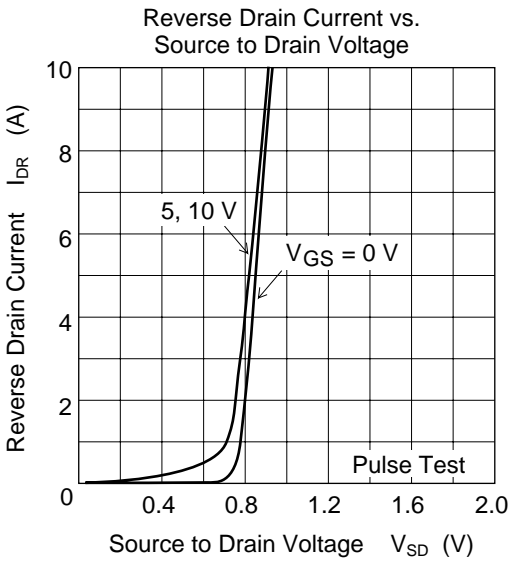


Dynamic Input Characteristics

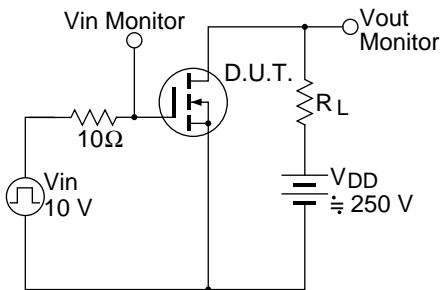


Switching Characteristics

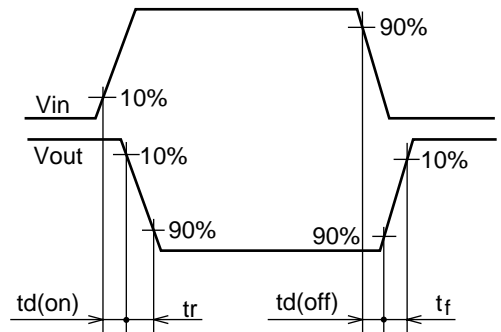


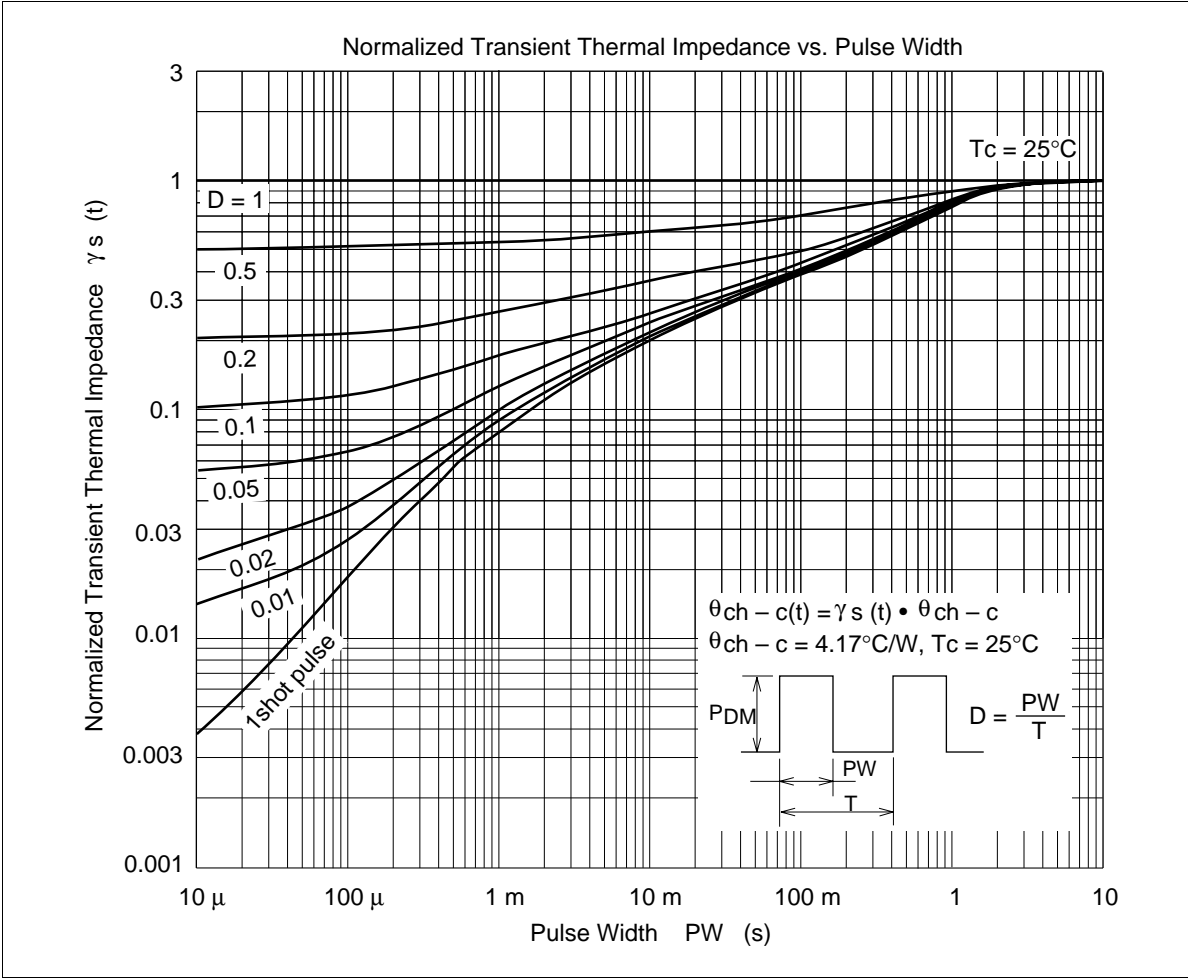


Switching Time Test Circuit



Waveform

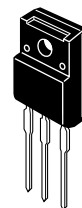
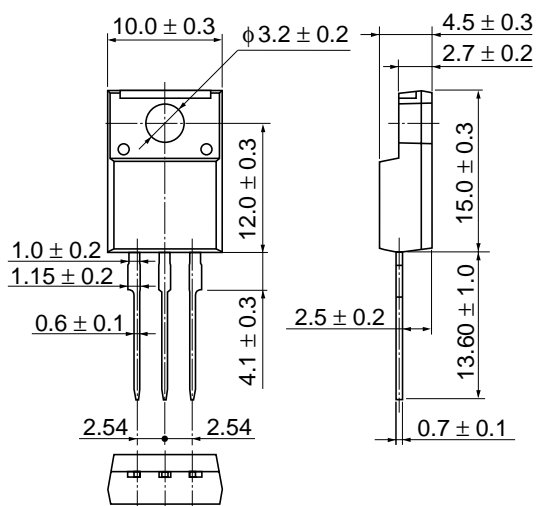




Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	TO-220CFM
JEDEC	—
EIAJ	—
Mass (reference value)	1.9 g

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