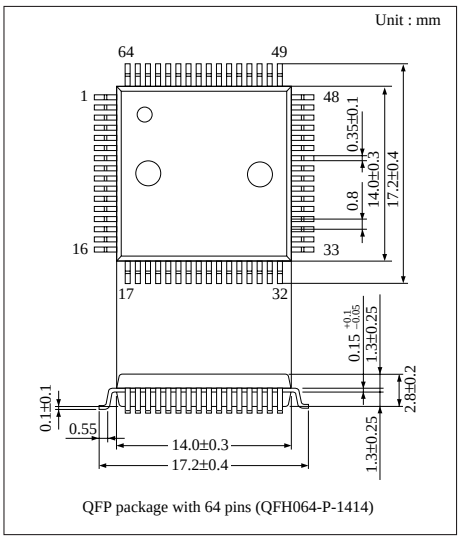
AN6472NFBP

Cordless Telephone Speech Network IC Incorporating Cross-Point Switch

■ Overview

The AN6472NFBP is a speech network IC which includes a receiver noise reducing function and is most suitable for quality cordless telephones. It incorporates a cross-point switch controlled by serial input. It allows speech path switching and mixing, and provides for three- or four-person communication and other sophisticated functions. It also incorporates REC/PLAY amplifiers with VOX circuits.

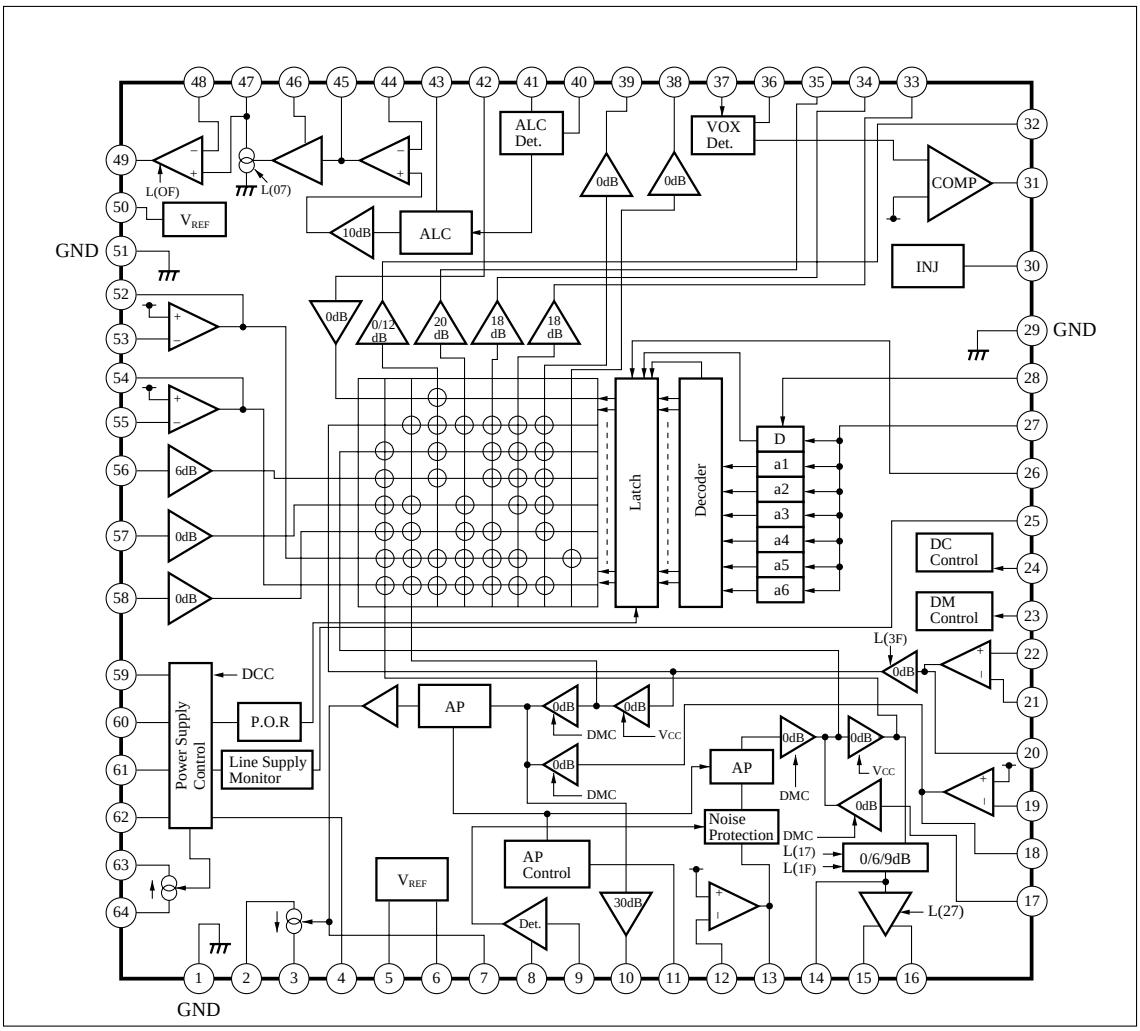


QFP package with 64 pins (QFH064-P-1414)

■ Features

- The speech block can operate on line voltage, with no external power supply, and is operational even during a commercial power failure.
- Incorporates a receiver noise reducing function to improve the handset's howling margin.
- Incorporates auto. PAD, dial mute, DC voltage regulation, and other basic speech functions.
- The cross-point switch can be operated independently.
- Each output of the cross-point switch can correspond to multiple inputs, allowing three- or four-person communication.
- The REC/PLAY amplifiers incorporate ALC and VOX circuits.
- Receiver volume can be increased by 6 dB or 9 dB.

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Ground	33	RF2 link output
2	Line power (+) input	34	RF1 link output
3	Side-tone adjustment	35	Intercom link output
4	Line voltage control (1)	36	VOX detection control
5	Int. ref. voltage output (2)	37	VOX amp. input
6	Int. ref. voltage output (1)	38	Time stamp link output
7	Trans. preamp. output	39	Recording link output
8	Noise reduction detection output	40	ALC input
9	Noise reduction detection input	41	ALC detection control
10	Noise reduction amp. output	42	Loudspeaker link input
11	Auto. PAD control	43	Recording input
12	Rec. preamp. input	44	Recording inverse input
13	Rec. preamp. output	45	Recording preamp. output
14	Rec. amp. input	46	Recording bias current control
15	Rec. amp. output (1)	47	To recording head
16	Rec. amp. output (2)	48	EQ amp. inverse input
17	BT signal input	49	EQ amp. output
18	DTMF preamp. output	50	REC/PLAY int. ref. voltage output
19	DTMF signal input	51	Ground
20	MIC preamp. output	52	MIX preamp. output
21	MIC preamp. input (1)	53	MIX link input
22	MIC preamp. input (2)	54	AUX preamp. output
23	Dial mute control	55	AUX link input
24	Line voltage control	56	Intercom link input
25	Line interruption detector output	57	RF1 link input
26	Strobe signal input	58	RF2 link input
27	Clock signal input	59	Power-ON reset control
28	Data input	60	External supply voltage input
29	Ground	61	Internal supply voltage output
30	Logic power supply input	62	Circuit voltage control (2)
31	VOX detector output	63	Line current bypass (2)
32	SP link output	64	Line current bypass (1)

■ Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	7.0	V
Supply current (1)	I_{CC}	50	mA
Supply voltage (2)	V_L	12.0	V
Supply current (2)	I_L	135	mA
Power dissipation*1	P_D	640	mW
Operating ambient temperature	T_{opr}	–20 to+75	˚C
Storage temperature	T_{stg}	–55 to+150	˚C

*1 In a free-air condition with Ta=75˚C

■ Recommended Operating Range

Parameter	Symbol	Range
Operating supply voltage range (1)	V_{CC}	4.5V to 5.5V
Operating supply voltage range (2)	V_L	3.0V to 11.0V

■ Recommended Operating Conditions (Ta =20 to +75˚C)

Parameter		Symbol	Condition	min	typ	max	Unit
Supply voltage		V_{CC}		4.5	5	5.5	V
Clock frequency		f_{CLK}	Input Duty 40% to 50%	—	—	250	kHz
Input pulse width	CLK	t_W		1.6	—	—	µs
	STB			1.2	—	—	µs
Setup time	DATA	t_{su}		1.6	—	—	µs
	STB			0.8	—	—	µs
Hold time	DATA	t_h		1.6	—	—	µs
	STB			1.2	—	—	µs
Input pulse width (high)		t_{wh}		0.8	—	—	µs
Input pulse width (low)		t_{wl}		0.8	—	—	µs
Clock pulse rise time		t_r		—	—	20	µs
Clock pulse fall time		t_r		—	—	20	µs
Input voltage		V_i		0	—	V_{CC}	V

■ Electrical Characteristics (Ta=25±2˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Power Supply Characteristics During Power Failure						
Line DC voltage (I-1)	V_{L-I1}	V–DCC=HIGH, I_L=20mA, V_{CC}=0V	3.2	3.5	3.8	V
Line DC voltage (I-2)	V_{L-I2}	V–DCC=HIGH, I_L=60mA, V_{CC}= 0V	4.5	4.8	5.2	V
Line DC voltage (I-3)	V_{L-I3}	V–DCC=HIGH, I_L=120mA, V_{CC}= 0V	6.6	7.0	7.5	V
Line DC voltage H (I-1)	V_{LH-I1}	V–DCC= LOW, I_L=30mA, V_{CC}= 0V	4.5	5.0	5.5	V
Line DC voltage H (I-2)	V_{LH-I2}	V–DCC= LOW, I_L= 60mA, V_{CC}= 0V	5.7	6.2	6.7	V
Line DC voltage H (I-3)	V_{LH-I3}	V–DCC= LOW, I_L=120mA, V_{CC}= 0V	7.9	8.5	9.2	V
Internal supply voltage (I)	V_{reg-I}	V– DCC=HIGH, I_L=20mA, V_{CC}= 0V	1.8	2.0	2.2	V
Internal ref. supply voltage (I)	V_{ref-I}	V–DCC=HIGH, I_L=20mA, V_{CC}= 0V	0.9	1.0	1.1	V
Normal power supply characteristics						
Line DC voltage (E-1)	V_{L-E1}	V– DCC=HIGH, I_L=20mA, V_{CC}=5V	3.1	3.4	3.8	V
Line DC voltage (E-2)	V_{L-E2}	V–DCC=HIGH, I_L=20mA, V_{CC}=5V	4.3	4.7	5.1	V
Line DC voltage (E-3)	V_{L-E3}	V–DCC=HIGH, I_L=20mA, V_{CC}=5V	6.3	6.8	7.3	V
Line DC voltage H (E-1)	V_{LH-E1}	V–DCC=HIGH, I_L=20mA, V_{CC}=5V	4.3	4.85	5.4	V

■ Electrical Characteristics (cont.) (Ta=25±2˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Line DC voltage H (E-2)	V_{LH-E2}	V–DCC=LOW, I_L=60mA, V_{CC}=5V	5.3	5.95	6.6	V
Line DC voltage H (E-3)	V_{LH-E3}	V–DCC=LOW, I_L=120mA, V_{CC}=5V	7.55	8.2	8.9	V
Internal supply voltage (E)	V_{reg-E}	V–DCC=HIGH, I_L=20mA, V_{CC}=5V	4.6	4.85	5.0	V
Internal ref. supply voltage (E)	V_{ref-E}	V–DCC=HIGH, I_L=20mA, V_{CC}=5V	2.25	2.5	2.7	V
Total circuit current	I_{total}	V–DCC=HIGH, I_L=20mA, V_{CC}=5V	17	27	35	mA
Power interruption detection (1)	V_{-HIT1}	V_L=2.7V, V_{CC}=5V	0	0.1	0.6	V
Power interruption detection (2)	V_{-HIT2}	V_L=1.5V, V_{CC}=5V	4.4	4.95	5	V
Receiver During Power Failure						
Rec. gain (I-1)	G_{V-IR1}	I_L=30mA, V_{CC}= 0V V_{in}= – 42dBm	30.5	32.5	34.5	dB
Rec. gain (I-2)	G_{V-IR2}	I_L= 80mA, V_{CC}= 0V V_{in}= –42dBm	27	29	31	dB
Rec. auto. PAD width (I)*1	A_{P-IR}	I_L=30mA– 80mA, V_{CC}= 0V, V_{in}= – 42dBm	2.5	3.5	5	dB
Rec. max. output (I)	V_{O-IR}	With I_L=30mA, V_{CC}= 0V, and THD=5%	0	4	—	dBm
Rec. noise reduction (I)	N_{L-IR}	I_L=30mA, V_{CC}= 0V, V_{in}= –42dBm V_{in}–M= –65/–50dBm	4	6	8	dB
BT amp. gain (I)	G_{V-IBT}	I_L=30mA, V_{CC}= 0V, V–DMC=LOW, V_{in}= –30dBm	19	21	23	dB
Receiver On External Power Supply						
Rec. gain (E-1)	G_{V-ER1}	I_L=30mA, V_{CC}=5V V_{in}= –42dBm	30.5	32.5	34.5	dB
Rec. gain (E-2)	G_{V-ER2}	I_L=30mA, V_{CC}=5V V_{in}= –42dBm	26.8	28.8	30.8	dB
Rec. auto. PAD width (E)*1	A_{P-ER}	I_L=30mA–80mA, V_{CC}=5V V_{in}= –42dBm	2.5	3.7	5	dB
Rec. max. output (E)	V_{O-ER}	With I_L=30mA, V_{CC}=5V, and THD=5%	4	12	—	dBm
Rec. noise reduction (E)	N_{L-ER}	I_L=30mA, V_{CC}=5V, V_{in}= –42dBm V_{in}–M= –65/–65dBm	6	8	10	dB
Rec. digital volume (1)*2	G_{V-DV1}	I_L=30mA, V_{CC}=5V, V_{in}= –42dBm, DV–1 ON	5	6	7	dB
Rec. digital volume (2)*2	G_{V-DV2}	I_L=30mA, V_{CC}=5V, V_{in}= –42dBm, DV–2 ON	7.5	9	10.5	dB
BT amp. gain (E)	G_{V-EBT}	I_L=30mA, V_{CC}=5V, V–DMC=LOW, V_{in}= –30dBm	19.5	21.5	23.5	dB
Rec. gain difference	DG–R	For V_{CC}=0V and 5V(between Gv–IR1 and Gv–ER1)	–1.2	– 0.1	1.2	dB
Transmitter Amp. During Power Failure						
Trans. gain (I-1)	G_{V-IM1}	R=27Ω(Pin3), I_L=30mA, V_{CC}=0V, V_{in}= –38dBm	28.2	30.2	32.2	dB
Trans. gain (I-2)	G_{V-IM2}	I_L=80mA, V_{CC}=0V, V_{in}= –38dBm	24.4	26.4	28.4	dB
Trans. auto. PAD width (I)*1	A_{P-IM}	I_L=30mA–80mA, V_{CC}=0V, V_{in}= –38dBm	2.5	3.8	5	dB

Note) Unless otherwise specified, input signal Fin =1kHz, control voltage V-DOC = high, and control voltage V-DMC = high.

*1 Gain decrease when line current I_L is changed from 30 to 80 mA. If pin 11 (auto. PAD control)is connected to pin 61 (int. supply voltage output), the gain will not change.

*2 Gain increase from receiver gain (E-1).

■ Electrical Characteristics (cont.) (Ta=25±2˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Trans. max. output (I-1)	V_{O-IM1}	With I_L=30mA, V_{CC}= 0V and HD=5%	0	3.5	—	dBm
Trans. max. output (I-2)	V_{O-IM2}	With I_L=30mA, V_{CC}= 0V, THD=5% and V–DCC=LOW	0	3.5	—	dBm
DTMF gain (I-1)	G_{V-ID1}	I_L=30mA, V_{CC}= 0V, V–DMC= LOW, V_{in}= –30dBm	17.5	19.5	21.5	dB
DTMF gain (I-2)	G_{V-ID2}	I_L=80mA, V_{CC}= 0V, V–DMC=LOW, V_{in}= –30dBm	13.7	15.7	17.7	dB
DTMF auto. PAD width (I)*1	A_{P-IDT}	I_L=30mA–80mA, V_{CC}= 0V, V–DMC= LOW, V_{in}= –30dBm	2.5	3.8	5	dB
DTMF max. output (I-1)	V_{O-ID1}	I_L=30mA, V_{CC}=0V, V–DMC=LOW, THD=5%	0	3.8	—	dBm
DTMF max. output (I-2)	V_{O-ID2}	I_L=30mA, V_{CC}= 0V, THD=5%, V–DMC=LOW, V–DCC=LOW	0	3.5	—	dBm
Transmitter Amp. On External Power Supply						
Trans. gain (E-1)	G_{V-EM1}	I_L=30mA, V_{CC}= 0V, V_{in}= –38dBm	28.6	30.6	32.6	dB
Trans. gain (E-2)	G_{V-EM2}	I_L=80mA, V_{CC}=5V, V_{in}= –38dBm	25.0	27.0	29.0	dB
Trans. auto. PAD width (E)*1	A_{P-EM}	I_L=30mA–80mA, V_{CC}=5V, V_{in}= –38dBm	2.5	4	5	dB
Trans. max. output (E-1)	V_{O-EM1}	With I_L=30mA, V_{CC}=5V and THD=5%	2	6	—	dBm
Trans. max. output (E-2)	V_{O-EM2}	I_L=30mA, V_{CC}=5V, THD=5%, V–DCC=LOW	2	6	—	dBm
DTMF gain (E-1)	G_{V-ED1}	I_L=30mA, V_{CC}=5V, DM=ON, Vin= –30dBm	18.1	20.1	22.1	dB
DTMF gain (E-2)	G_{V-ED2}	I_L=80mA, V_{CC}=5V, V–DMC=LOW, V_{in}= –30dBm	14.5	16.5	18.5	dB
DTMF auto. PAD width (E)*1	A_{P-EDT}	I_L=30mA–80mA, V_{CC}=5V, V–DMC=LOW, V_{in}= –30dBm	2.5	4.1	5.5	dB
DTMF max. output (E-1)	V_{O-ED1}	I_L=30mA, V_{CC}=5V, V–DMC=LOW, THD=5%	2	6	—	dBm
DTMF max. output (E-2)	V_{O-ED2}	I_L=30mA, V_{CC}=5V, DM=ON, V–DMC=LOW, THD=5%	2	6	—	dBm
Trans. gain difference	DG – M	For V_{CC}= 0V and V_{CC}=5V (between Gv–IM1 and Gv–EM1)	–1.8	–0.8	0.7	dB
DTMF gain difference	DG – MF	For V_{CC}= 0V and 5V (between Gv–ID1 and Gv–ED1)	–2.3	–1.3	0.2	dB

Note) Unless otherwise specified, input signal Fin=1 kHz, control voltage V-DOC=high, and control voltage V-DMC=high.

*1 Gain decrease when line current I_L is changed from 30 to 80 mA. If pin 11 (auto. PAD control) is connected to pin 61(int. supply voltage output) , the gain will not change.

■ Electrical Characteristics (cont.) (Ta=25±2˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Recording Preamplifiers						
Rec. preamp. gain	G_{V-Rp}	V_{in}= – 60dBm, Rin=0Ω	43	45	47	dB
Rec. preamp. output	V_{O-RP}	V_{in}= – 45dBm, Rin=10Ω	–13.4	–11.4	–9.4	dBm
Rec. preamp. output noise voltage*1	V_{no-RP}	DIN/AUDIO, Rg=10kΩ	—	0.8	2.5	mVrms
Recording Amplifier						
Head bias current	I_{-REC}	L–SW (h07)= ON	145	180	215	μA
Head output	G_{V-REC}	L–SW (h07)= ON, V_{in}= –15dBm, RL=1kΩ	40.0	50.0	63.0	mVrms
Playing EQ Amplifier						
EQ amp. gain	G_{V-EQ}	L–SW (h07)= ON, V_{in}= – 40dBm	27.8	29.8	31.8	dB
EQ amp. output noise voltage	V_{no-EQ}	L–SW (h07)= ON, DIN/AUDIO, RL=1kΩ	—	0.45	1.2	mVrms
VOX Detector						
VOX sensitivity (1)	VS1	I–VOX=12.5μA	3.5	4.8	—	V
VOX sensitivity (2)	VS2	I–VOX=24.5μA	—	0.025	0.5	V
Link SW Input Amplifier						
MIX amp. gain	G_{V-MIX}	V_{in}= – 36dBm	5	6	7	dB
AUX amp. gain	G_{V-AUX}	V_{in}= – 36dBm	5	6	7	dB
Link SW Output Amplifier						
SP output gain (1)*1	G_{V-SPO1}	Input AUX IN, V_{in}= – 36dBm, L–SW (h3A) = ON	11	12	13	dB
SP output gain (2)*1	G_{V-SPO2}	Input AUX IN, V_{in}= – 36dBm, L–SW (h3A&h2F) = ON	–1.5	– 0.5	0.5	dB
Intercom output gain*1	G_{V-DHO}	Input AUX IN, V_{in}= – 36dBm, L–SW (h3B) = ON	18.5	20	21.5	dB
RF1 output gain*1	G_{V-RF10}	Input AUX IN, V_{in}= – 36dBm, L–SW (h3C) = ON	16.5	18	19.5	dB
RF2 output gain*1	G_{V-RF20}	Input AUX IN, V_{in}= – 36dBm, L–SW (h3D) = ONΩ	16.5	18	19.5	dB
Recording output gain*1	G_{V-RECO}	Input AUX IN, V_{in}= – 36dBm, L–SW (h3E) = ON	–1.0	0	1.0	dB
Recording output gain*1	G_{V-RO}	Input AUX IN, V_{in}= – 36dBm, L–SW (h38) = ON	19.9	21.4	22.9	dB
Line output gain*1	G_{V-TO}	Input AUX IN, V_{in}= – 36dBm, L–SW (h39) = ON	17.7	19.2	20.7	dB
Rec. output gain difference*2	GD_{-RO}	Input AUX IN, V_{in}= – 36dBm, L–SW (h30) = ON	–1.0	0	1.0	dB
Time stamp output gain*1	G_{V-TSO}	Input AUX IN, V_{in}= – 36dBm, L–SW (h37) = ON	–1.0	0	1.0	dB

Note) Unless otherwise specified, external supply voltage V_{CC}=5V, line current I_L= 0mA, input signal frequency=1 kHz, control voltage V-DOC=high, and control voltage V-DMC = high.

*1 Each amp. gain is measured from AUX OUT or MIX OUT to its output (the AUX or MIX preamp. gain is not included in the calculation).

*2 The difference from the receiver output gain (Gv-RO).

■ Electrical Characteristics (cont.) (Ta=25±2˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Link SW Input						
MIC input gain*1	G_{v-MI}	V_{in}= –38dBm, rec. output L –SW(h0E)= ON	–1	0	1	dB
Rec. input gain*1	G_{v-RI}	V_{in}= –42dBm, rec. output L–SW (h16)= ON	–1	0	1	dB
Intercom input gain	G_{v-DHI}	V_{in}= –30dBm, rec. output L–SW (h1E)= ON	5	6	7	dB
RF1 input gain	G_{v-RF1I}	V_{in}= –30dBm, rec. output L–SW (h26)= ON	–1	0	1	dB
RF2 input gain	G_{v-RF2I}	V_{in}= –30dBm, rec. output L–SW (h2E)= ON	–1	0	1	dB
SP link input gain	G_{v-SPI}	V_{in}= –30dBm, SP rec. output L–SW (h02)= ON	11	12	13	dB
Link Maximum Output						
SP OUT max. output	V_{o-SP}	Input L–SP IN, THD=5% L–SW (h02)= ON	0	4	—	dBm
DH OUT max. output	V_{o-DH}	Input RF1 IN, THD=5% L–SW (h23)= ON	0	4	—	dBm
RF1 OUT max. output	V_{o-RF1}	Input RF2 IN, THD=5% L–SW (h25) = ON	0	4	—	dBm
RF2 OUT max. output	V_{o-RF2}	Input RF1 IN, THD=5% L–SW (h2C)= ON	0	4	—	dBm
L-REC OUT max. output	V_{o-LR}	Input AUX IN, THD=5% L–SW (h3E)= ON	0	4	—	dBm

Note) Unless otherwise specified, external supply voltage V_{CC}=5V, line current I_L= 0mA, input signal frequency=1 kHz, control voltage V-DOC= high, and control voltage V-DMC= high.
*1 Each amp. gain is measured from MIC OUT or R PRE OUT to its output.

■ Electrical Characteristics (cont.) (Ta=25±2˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Controls						
Dial mute high level voltage	V_{DMC-H}		2	—	V_{CC} + 0.2	V
Dial mute high level control current	I_{DMC-H}	V– DMC = 5V	15	38	80	µA
Dial mute low level voltage	V_{DMC-L}		– 0.2	—	0.3	V
Dial mute low level control current	I_{DMC-L}	V– DMC= 0V	– 40	–20	–10	µA
DC voltage control high level voltage	V_{DCC-H}		2	—	V_{CC} + 0.2	V
DC voltage control high level control current	I_{DCC-H}	V – DCC= 5V	10	25	50	µA
DC voltage control low level voltage	V_{DCC-L}		– 0.2	—	0.4	V
DC voltage control low level control current	I_{DCC-L}	V– DCC= 0V	–2	– 0.1	—	µA

Note) Unless otherwise specified, V_{CC}=5V, and I_L = 20 mA.

■ Electrical Characteristics (cont.) (Ta=25±2˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Data input high level voltage	V_{DIN-H}		2	—	V_{CC} + 0.2	V
Data input high level control current	I_{DIN-H}	V– DIN=5V	70	160	250	µA
Data input low level voltage	V_{DIN-L}		– 0.2	—	0.3	V
Data input low level control current	I_{DIN-L}	V– DIN = 0V	–1	– 0.1	—	µA
Power Supply Block						
AC impedance (I)	Z_{AC-I}	I_L=80mA, V_{CC}= 0V, V_{in}=200mVrms, Fin=1kHz	450	570	750	Ω
AC impedance (E)	Z_{AC-E}	I_L=80mA, V_{CC}=5V, V_{in}=200mVrms, Fin=1kHz	450	580	750	Ω
Input impedance						
BT amp. input impedance	Z_{in-BT}	Pin 17 Input	8.7	9.5	10.7	kΩ
ALC amp. input impedance	Z_{in-ALC}	Pin 40 Input	8.5	9.5	10.5	kΩ
Intercom preamp. input impedance	Z_{in-DH}	Pin 56 Input	8.5	9.5	10.5	kΩ
RF1 preamp. input impedance	Z_{in-RF1}	Pin 57 Input	8.5	9.5	10.5	kΩ
RF2 preamp. input impedance	Z_{in-RF2}	Pin 58 Input	8.5	9.5	10.5	kΩ
SP input impedance	Z_{in-SP}	Pin 42 Input	37.5	50.0	62.5	kΩ

■ Electrical Characteristics (Design Values for Reference) (Ta=25±2˚C)

The following are design values for reference, not guaranteed values.

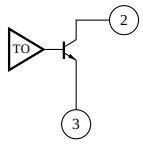
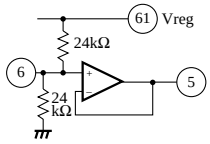
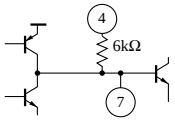
Parameter	Symbol	Condition	min	typ	max	Unit
Speech Block						
Rec. output noise voltage (I)	V_{n-IR}	I_L=30mA, V_{CC}=0V, DIN/AUDIO	—	0.3	—	mVrms
Rec. output noise voltage (E)	V_{n-ER}	I_L=30mA, V_{CC}=5V, DIN/AUDIO	—	0.3	—	mVrms
Trans. output noise voltage (I)	V_{n-IT}	I_L=30mA, V_{CC}=0V, DIN/AUDIO	—	0.3	—	mVrms
Trans. output noise voltage (E)	V_{n-ET}	I_L=30mA, V_{CC}=5V, DIN/AUDIO	—	0.3	—	mVrms
Dial mute trans. amp. mute attenuation	M_{-TDM}	I_L=30mA, V_{CC}=5V, V_{in}= –30dBm, V– DBM–H/L	—	75	—	dB
Trans. preamp. mute attenuation	M_{-TM}	I_L=30mA, V_{in}= –30dBm, V_{CC}=5V, Lsw (h3F)=OFF/ON	—	70	—	dB
Rec. output mute attenuation	M_{-RO}	I_L=30mA, V_{in}= –30dBm, V_{CC}=5V, Lsw (h27)= OFF/ON	—	50	—	dB
Rec. preamp. input impedance	Z_{in-R}	Pin 12 Input	—	500	—	kΩ
MIC preamp. input impedance	Z_{in-M}	Pin 21 and 22 Input	—	500	—	kΩ
REC/PLAY Block						
ALC amp. ALC width	W_{-ALC}	I_L= 0mA, V_{CC}=5V, and ALC output distortion≤2%	—	40	—	dB
ALC amp. ALC effect	DALC	I_L=0mA, V_{CC}=5V, and V_{in}= –45dBm to –20dBm	—	1	—	dB
Rec. amp. mute attenuation	M_{-REC}	V_{CC}=5V, V_{in}= –10dBm I_L= 0mA, and LSW (h07)= ON/OFF	—	80	—	dB

■ Electrical Characteristics (Cont.) (Design Values for Reference) (Ta=25±2˚C)

The following are design values for reference, not guaranteed values.

Parameter	Symbol	Condition	min	typ	max	Unit
EQ amp. mute attenuation	M_{-EQ}	V_{CC}=5V, V_{in}= –30dBm I_L= 0mA, LSW(h0F)=ON/OFF	—	80	—	dB
Rec. preamp. input impedance	Z_{in-REC}	Pin 43 input	—	10	—	kΩ
EQ amp. input impedance	Z_{in-EQ}	Pins 47 and 48 input	—	500	—	kΩ
VOX amp. input impedance	Z_{in-VOX}	Pin 47 input	—	500	—	kΩ
Link Switch						
Link SW mute attenuation	M_{-LS}	V_{CC}=5V, I_L=30mA, AC output measured at link ON/OFF	—	75	—	dB
MIX preamp. input impedance	Z_{in-MIX}	Pin 53 input	—	500	—	kΩ
AUX preamp. input impedance	Z_{in-AUX}	Pin 55 input	—	500	—	kΩ
CPC output impedance	$Z_{out-CPC}$	Pin 25 input	—	100	—	kΩ
Noise reduction amp. input impedance	Z_{in-NL}	Pin 9 input	—	45	—	Ω
VOX cross talk	V_{OX-CT}	V_{CC}=5V, I_L=30mA, cross talk to line during VOX	—	–70	—	dBm

■ Pin Descriptions

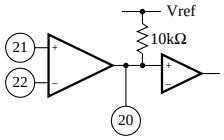
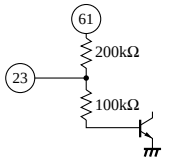
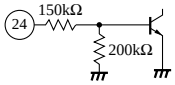
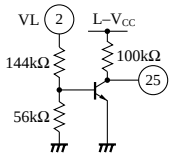
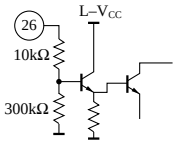
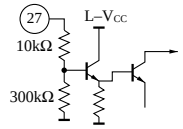
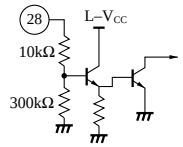
Pin No.	Pin name	I/O	Waveform	Description	Equivalent circuit	Remarks
1	GND	—	0V	Ground : •This is the ground pin for the speech network.	GND for REC/PLY, VREG, SPEECH and LINK	———
2	VL	I	DC 3 ~10V	Line power input: •Connects to the positive output of the diode bridge.		The line drive gain (G) is : $G = \frac{Z_{Line}//Z_{Tel}}{R_1}$ Also assuming $Z_{Line} \approx 600\Omega$ $Z_{Tel} \approx 600\Omega$ $R_1 = 27\Omega$ $G = 20\log\frac{300}{27} = 20.9db$
3	ST	O	DC 0.3V	Side-tone adjustment: •Grounded through R1 (27Ω) •Connects to the side-tone adjusting circuit to adjust side tone and receiver level.		
4	VL–CONT	I	DC1V	Line voltage control (1) :	———	C2 and the internal resistance determine the f. characteristics.
5	Vref–SN	O	1V (Const)	Int. ref. voltage output (2) : •Output impedance=50Ω		———
6	Vref	O	1V (Const)	Int. ref. voltage output (1) : •Outputs half the Vreg reference voltage.		Grounded through a 0.01μF capacitor.
7	T–FILTER	O	DC1V	Trans. preamp. output : •C7 as connected between this pin and the ground forms a low-pass filter.		———

Note) The symbols are the same as those used in the application circuit.

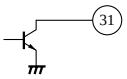
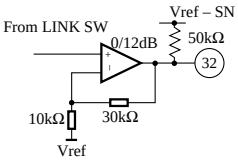
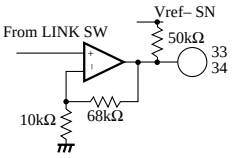
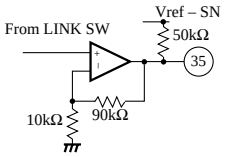
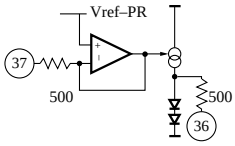
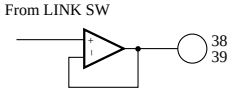
■ Pin Descriptions (cont.)

Pin No.	Pin name	I/O	Waveform	Description	Equivalent circuit	Remarks
8	VN DET	—	Pin 8 output: DC (with a capacitor); Input; Full-wave detection (with no capacitor)	•Noise reduction detection amp. output : A smoothing capacitor C6 and R5 connect to this pin to adjust the attack and recovery times of noise reduction.	Vref–SN; 95kΩ; 64kΩ; 3kΩ; 0.1µF; pins 10, 9, 8	•This pin must be grounded if noise reduction is not used. •The greater C7, the longer the attack time. The smaller R6, the shorter the recovery time. •Noise reduction detection amp. gain (G) is : $G = \frac{64K}{R6}$
9	VN DET– IN	I		•Noise reduction detection amp. input : Noise reduction amp. output is fed through C7 and R6 to this pin.		
10	VN OUT	O	V_{REF}	•Noise reduction amp. output : Connects to the noise reduction detection amp. input.		
11	APC	I	Vreg-R · I IL	Auto. PAD control : •Connects through a resistance to Pin 61(Vreg). If the resistance increases, the PAD operates closer to the near end. If the resistance decreases, the PAD operates closer to the far end.	pin 11; I; $I \propto I_L$	———
12	RV IN	I	V_{REF} – SN	Rec. preamp. input : •Receiver signals are input from the side-tone circuit to this pin. •R8 and C9 connected between Pin 13 and this pin determine the f. characteristics.	pins 12, 13	The receiver preamplifier gain (G) is : $G = -\frac{1}{\frac{1}{R9} + \frac{1}{j\omega C9}} \Big/ (R8 + j\omega C10)$
13	RV PREOUT	O	V_{REF} – SN	Rec. preamp. output : •R8 and C9 connected between Pin 12 and this pin determine the f. characteristics. •The output impedance is up to 1 kΩ.	10kΩ; pin 13	
14	RV FILTER	O	V_{REF} – SN	Rec. amp. input :		———
15 . 16	RV OUT (1) RV OUT (2)	O	V_{REF} – SN V_{REF} – SN	Rec. amp. outputs (1 and 2) : •A ceramic or dynamic receiver is connected. •The output circuit is a BTL configuration. •The output impedance is up to 50 Ω.	10kΩ; 30kΩ; pins 16, 13, 15	
17	BT– IN	I	V_{REF} – SN Signal input	BT signal input : •BT (beep tone) signals are input through C15 to this pin. •Input impedance is 10 kΩ.	Vref–SN; 10kΩ; pin 17	In the application circuit, MIC. IN (–) is input through a capacitor. This capacitor and R12-R14, and C15 and C16 determine the f. characteristics.
18	MF – OUT	O	V_{REF} – SN	DTMF preamp. output : •A C/R combination between Pin 19 and this pin determines the f. characteristics of the DTMF preamp.	pin 18	
19	MF – IN	I	V_{REF} – SN Signal input	DTMF signal input : •DTMF signals are input through a capacitor to this pin. •DTMF signals are enabled when DMC is low at Pin 40.	Vref–SN; 10kΩ; pins 19, 18	The 10 kΩ input impedance and C12 or C13 form a HPF.

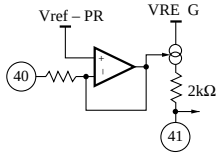
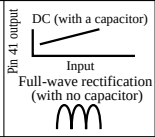
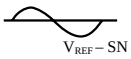
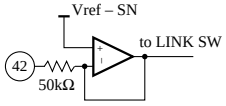
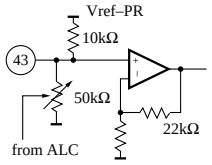
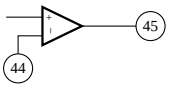
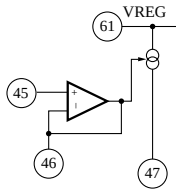
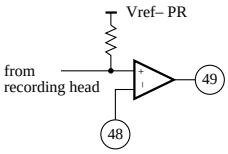
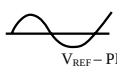
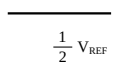
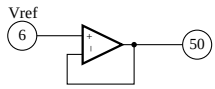
■ Pin Descriptions (cont.)

Pin No.	Pin name	I/O	Waveform	Description	Equivalent circuit	Remarks
20	MIC OUT	O	V_{REF} – SN	MIC preamp. output : •R12 and C14 connected between Pin 22 and this pin determine the f. characteristics. •The output impedance is up to 1 kΩ.		———
21	MIC IN (+)	I	V_{REF} – SN	MIC preamp. input (1) : •A bias resistor and a microphone connect to this pin.		
22	MIC IN (–)	I	V_{REF} – SN	MIC preamp. input (2) : •R12 and C14 connected between Pin 20 and this pin determine the f. characteristics.		
23	DMC	I		Dial mute control : •Normal speech mode when Pin 23 is high or open (MIC amp. ON and rec. amp. ON). •DTMF mode when Pin 23 is low (DTMF amp. ON and BT amp. ON).		———
24	DC – CONT	I	V_{CC} 0.2V Line DC voltage	Line voltage control : •Line voltage is normal when the input voltage at this pin is high. Line voltage increases by 1-1.5 V when the input voltage is low.		———
25	CPC	O	$L–V_{CC}$ 0.2V Line interruption	Line interruption detector output : •This is an open collector output to a microprocessor, requiring a pull-up resistor connected to the microprocessor's power supply. This pin goes low when line voltage is 3.0 V or more, and goes high when 1.5 V or less.		———
26	STR	I	5V 0V	Strobe signal input : •The strobe signal for serial control data is input to this pin. The rising edge of the strobe signal determines the timing at which internal control address or ON/OFF status is validated.		———
27	CLK	I	5V 0V	Clock signal input : •The clock signal for serial control data is input to this pin. The rising edge of the clock signal determines the timing at which data is read.		———
28	DATA	I	5V 0V	Data input : •Serial data is input to this pin. Data is read into the internal shift register in synchronization with clock signals.		———

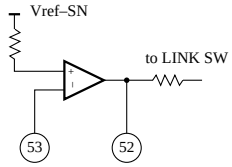
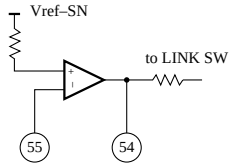
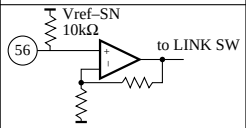
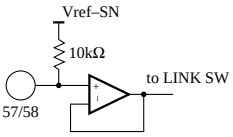
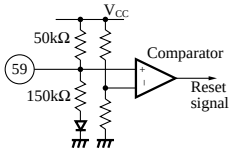
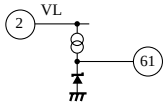
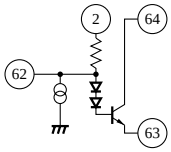
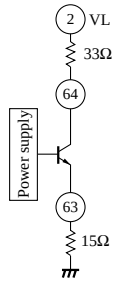
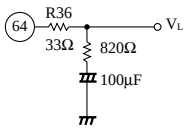
■ Pin Descriptions (cont.)

Pin No.	Pin name	I/O	Waveform	Description	Equivalent circuit	Remarks
29	GND	—		Ground : •This is the ground pin for the logic circuits.	———	———
30	L– V_{CC}	—		Logic power supply input :	———	———
31	VOX– OUT	O	L · V_{CC} 0V Voice ON	VOX detector output : •This is an open collector output. •This pin goes high when voice signals are input to Pin 37.		———
32	SP– OUT	O	V_{REF} – SN	Loudspeaker link output : •This is a link switch output to an external loudspeaker amplifier. •The output amplifier gain is selectable between 12 and 0 dB. •Output impedance is 50± 30Ω.		When address 2F of the cross-point switch is OFF, the output amplifier gain is set to 12 dB.
33	RF2– OUT	O	V_{REF} – SN	RF2 link output : •This is a link switch output. •Output impedance is 50Ω.		———
34	RF1– OUT	O	V_{REF} – SN	RF1 link output : •This is a link switch output. •Output impedance is 50Ω.		
35	DH– OUT	O	V_{REF} – SN	Intercom link output : •This is a link switch output to an intercom. •Output impedance is 50Ω.		———
36	VOX DET	O	DC (with a capacitor) Pin 36 output Pin 37 input Half-wave rectification (with no capacitor)	VOX detection control : •A smoothing capacitor (C18) and a resistor (R18) connect in parallel to this pin to adjust the attack and recovery times of the VOX detector.		VOX detection can be done in two ways : A) With small C18 (560 pF) and small R18 (39kΩ) VOX input VOX output B) With large C18 (22 µF) and large R18 (100 kΩ) VOX input VOX output
37	VOX IN	I		VOX amp. input : •VOX (voice detection) signals are input to this pin. •Input impedance is 500Ω.		
38	LTS– OUT	O	V_{REF} – SN	Time stamp link output : •This is a buffered link switch output. •Output impedance is 50Ω.		———
39	LRC– OUT	O	V_{REF} – SN	Recording link output : •This is a buffered link switch output. •Output impedance is 50Ω.		

■ Pin Descriptions (cont.)

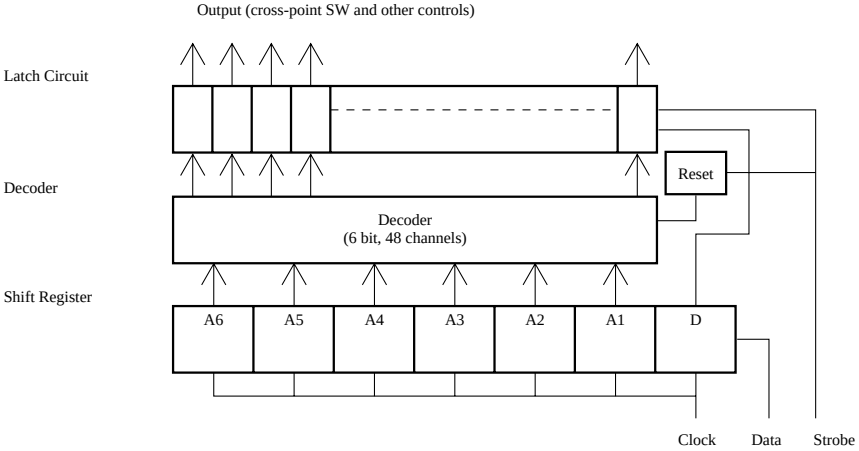
Pin No.	Pin name	I/O	Waveform	Description	Equivalent circuit	Remarks
40	ALC. IN	I		ALC input : •Pin 45 connects through a coupling capacitor to this pin. •Input impedance is 10kΩ.		•Ground Pin 41 if no ALC circuit is used. •The larger C20, the longer the attack time. The smaller R20, the shorter the recovery time
41	ALC. DET	O		ALC detection control : •A smoothing capacitor (C20) and a resistor (R20) connect in parallel to this pin to adjust the attack and recovery times of the ALC.		
42	SP – IN	I		Loudspeaker link input : •SP signals to this pin are output through a coupling capacitor to the link switch. •Input impedance is 50kΩ.		———
43	RD PRE – IN	I		Recording input : •Recording signals are input through a coupling capacitor to this pin. •Input impedance is normally 10kΩ. It decreases during ALC operation.		———
44	RD PRE – NF	I		Recording preamp. inverse input : •A/CR combination between Pin 45 and this pin determines the gain and f. characteristics of the recording preamplifier.		The gain (G) of the recording preamplifier is : $G = -\frac{R23}{R22+j\omega C23}$
45	REC PRE – OUT	O		Recording preamp. output : •Outputs amplified recording signals. •Output impedance is 50Ω.		
46	BIASS ADJ			Recording bias current control : •A C/R combination connected to this pin determines the recording bias current and gain of a recording head. •The smaller the resistance of the C/R combination, the greater the bias current and gain.		•Address 07 of the cross-point SW determines the ON/OFF status of the rec. preamp. •The bias current to the head is : $I_H = \frac{V_{REF}\text{-}^{PR}}{R25} \times 3$ $V_{REF}\text{-}^{PR} = \frac{1}{2} V_{reg}$
47	HEAD	I/O	Bias voltage 0V During recording 0V During playing	To recording head : •A recording head connects to this pin.		
48	EQ. NF	I		EQ amp. inverse input : •A C/R combination between Pin 49 and this pin determines the equalizer characteristics.		•The gain of the equalizer amp. is calculted the same way as the receiver preamp. •Address OF of the cross-point SW determines the ON/OFF status of the EQ amp.
49	EQ. OUT	O		EQ amp. output : •Outputs amplified equalizer signals. •Output impedance is 50Ω.		
50	V_{REF} – PR	O		REC/PLAY int. ref. voltage output : •The Pin 5 ref. voltage is buffered and output from this pin. •Output impedance is 50Ω		———
51	GND		———	Ground :	———	———

■ Pin Descriptions (cont.)

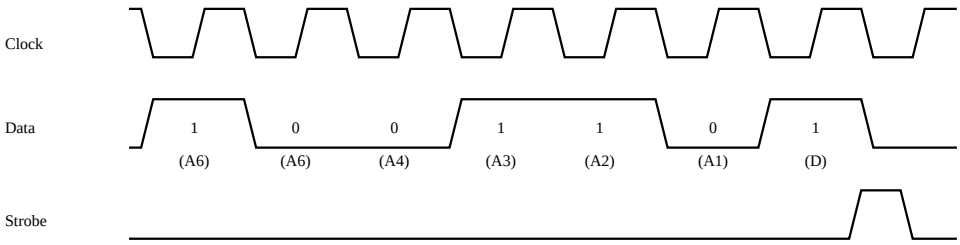
Pin No.	Pin name	I/O	Waveform	Description	Equivalent circuit	Remarks
52	MIX OUT	O	V_{REF} – SN	MIX preamp. output : • A C/R combination between Pin 53 and this pin determines the gain and f. characteristics of the MIX preamp. • Output impedance is 50Ω.		The gain of the MIX preamp. is calculated the same way as the rec. preamp.
53	MIX IN	I	———	MIX link input : • MIX signals are input through a coupling capacitor to this pin.		
54	AUX OUT	O	V_{REF} – SN	AUX preamp. output : • A C/R combination between Pin 55 and this pin determines the gain and f. characteristics of the AUX preamp. • Output impedance is 50Ω.		The gain of the AUX preamp. is calculated the same way as the rec. preamp.
55	AUT IN	I	———	AUX link input : • AUX signals are input through a coupling capacitor to this pin.		
56	DH IN	I	V_{REF} – SN	Intercom link input : • Intercom signals are input through a coupling capacitor C30 to this pin. • Input impedance is 10kΩ		The input impedance as illustrated left and C30, C31, or C32 form a HPF.
57	RF1 IN	I	V_{REF} – SN	RF1 link input : • RF1 signals are input through a coupling capacitor C31 to this pin. • Input impedance is 10kΩ.		
58	RF2 IN	I	V_{REF} – SN	RF2 link input : • Same as above.		
59	PR	I	———	Power-ON reset control : • C33 between this pin and GND determines the power-ON reset time of the logic circuits.		•The larger C33, the longer the power-ON reset time. • The power-ON reset signal is output when the supply voltage reaches 4V.
60	VCC	—	5V ±0.5V	External supply voltage input : • –5±0.5V power supply is input to this pin.	———	———
61	Vreg	O	V_{CC} to 0.2V DC 2V during power failure	Internal supply voltage output : • A power supply derived from line voltage is output from this pin to the internal speech network.		———
62	VLC	—	2 to 5 VDC depending on V_L	Circuit voltage control (2) : •This pin is grounded through C36.		C36 (typically 47µF) determines how the circuit voltage fluctuates.
63	PD2	O	DC 0 to 3 V depending on V_L	Line current bypass : •Line current is bypassed from this pin through R35 to GND. R35 must be 1/2 W or more.		Z_{Tel} is 1.5-2.0kΩ on the IC side. It must be adjusted to 600Ω by inserting a 820Ω resistor between VL and GND. 
64	PD1	I	DC Same as above V_L–33Ω × I_L	Line current bypass (1) : •Line current is bypassed from this pin through R36 to Pin 2. R36 must be 1/2 W or more.		

Logic Specifications

■ Basic Block Diagrams



■ Time Charts (Assuming the address h26 latch is to be set)



1. Data is read into the shift register in synchronization with a rising edge of the clock, with the higher data being shifted sequentially on a first-come highest-bit basis.
2. When the strobe is low, data is shifted sequentially on the sift register in synchronization with the clock. Data on the latch circuit will not change.
3. When the strobe goes high, the latched data whose address is represented by the highest six bits of the shift register is updated. Latched data is set when the least significant bit is 1, and reset when the bit is 0.
4. Referring to 3 above, if the address is h00 (the highest six bits of the shift register are all 0s), the latch circuit is cleared (all reset) regardless of the data content.
5. At power-on (VCC ON), the latch circuit is cleared (by power-ON reset).

■ Logic Circuits Address Specifications

1. Cross-point switch

Output / Input	Handset rec.	Line ouput	Loudspeaker	Intercom	RF1	RF2	Recording	Time stamp
Loudspeaker			02					
Microphone		09	0A	0B	0C	0D	0E	
Receiver	10		12		14	15	16	
Intercom	18		1A		1C	1D	1E	
RF1	20	21		23		25	26	
RF2	28	29		2B	2C		2E	
MIX	30	31	32	33	34	35		37
AUX	38	39	3A	3B	3C	3D	3E	

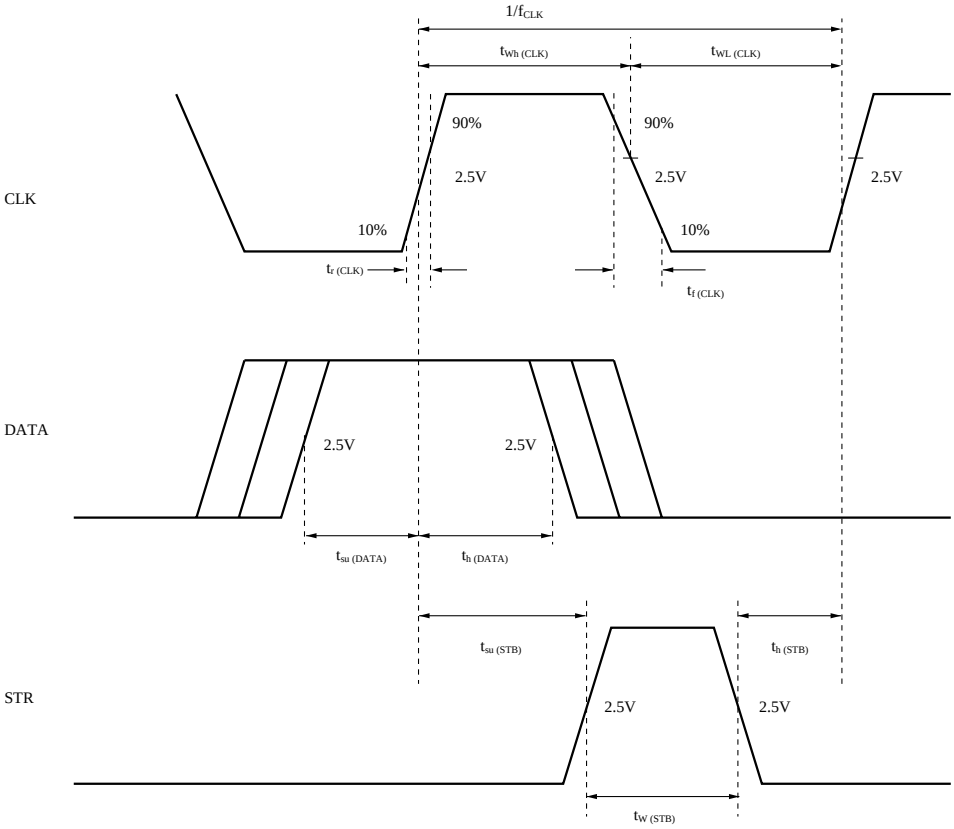
Note) Empty space means “not applicable.” Address is in hexadecimal.

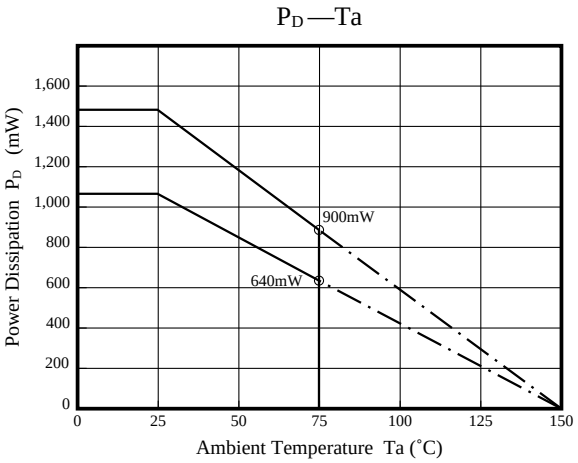
2. Other control switches

Address	Description
00	Cross-point SW all reset
07	Recording amp. ON
0F	Playing amp. ON
17	Receiver volume 6 dB up
1F	Receiver volume 9 dB up
27	Handset receiver amp. mute
2F	SP output amp. gain 12 dB down
3F	MIC preamp. mute
09, 21, 29	Receiver noise reduction is enabled.

Note) Address is in hexadecimal.

■ Timing Charts





■ AN6472NFBP Applicant Circuit