Dual 8-,10-,12-Bit, High Bandwidth Multiplying DACs with Parallel Interface

AD5428/AD5440/AD5447

FEATURES

10 MHz multiplying bandwidth
Fast parallel interface (58 MSPS write cycle)
AD7528 upgrade (AD5428)
AD7547 upgrade (AD5447)
2.5 V to 5.5 V supply operation
±10 V reference input
20- and 24-lead TSSOP packages
Dual 8-, 10-, and 12-bit current output DACs
Guaranteed monotonic
4-quadrant multiplication
Power-on reset
Readback function
0.5 µA typical current consumption

FUNCTIONAL BLOCK DIAGRAM

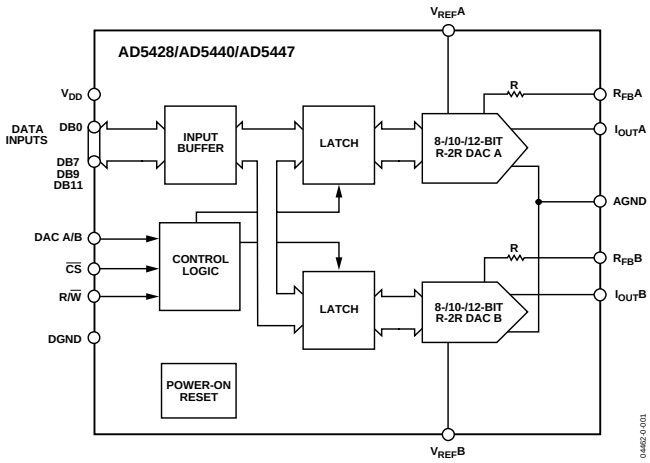

Figure 1. AD5428/AD5440/AD5447

APPLICATIONS

Portable battery-powered applications
Waveform generators
Analog processing
Instrumentation applications
Programmable amplifiers and attenuators
Digitally controlled calibration
Programmable filters and oscillators
Composite video
Ultrasound
Gain, offset, and voltage trimming

GENERAL DESCRIPTION

The AD5428/AD5440/AD5447[1] are dual CMOS 8-, 10-, and 12-bit current output digital-to-analog converters (DACs), respectively.

These devices operate from a 2.5 V to 5.5 V power supply, making them suited to battery-powered and other applications.

The DACs utilize data readback, allowing the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with zeros and the DAC outputs are at zero scale.

As a result of manufacture on a CMOS submicron process, they offer excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidths of up to 10 MHz.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external I-to-V precision amplifier.

The AD5428 is available in a small 20-lead TSSOP package, while the AD5440/AD5447 DACs are available in small 24-lead TSSOP packages.

[1] US Patent Number 5,689,257.

Rev. 0

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REVISION HISTORY

7/04—Revision 0: Initial Version

SPECIFICATIONS

Temperature range for Y version is –40°C to +125°C.

V_{DD} = 2.5 V to 5.5 V, $V_{REF}A = V_{REF}B$ = +10 V, AGND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. DC performance measured with OP1177, AC performance with AD8038, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
STATIC PERFORMANCE					
AD5428					
Resolution			8	Bits	
Relative Accuracy			±0.25	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
AD5440					
Resolution			10	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
AD5447					
Resolution			12	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			–1/+2	LSB	Guaranteed monotonic
Gain Error			±10	m V	
Gain Error Temp CoefficientT[1]		±5		ppm FSR/°C	
Output Leakage Current			±10	nA	Data = 0000_H, T_A = 25°C.
			±25	nA	Data = 0000_H.
REFERENCE INPUT[1]					
Reference Input Range		±10		V	
$V_{REF}A$, $V_{REF}B$ Input Resistance	8	10	12	k Ω	Input resistance TC = –50 ppm/°C
$V_{REF}A$ to $V_{REF}B$ Input Resistance Mismatch		1.6	2.5	%	Typ = 25°C, max = 125°C
$R_{FB}A$,$R_{FB}B$ Input Resistance	8	10	12	k Ω	Input resistance TC = –50 ppm/°C
Input Capacitance					
Code 0		3	6	pF	
Code 4095		5	8	pF	
DIGITAL INPUTS/OUTPUT[1]					
Input High Voltage, V_{IH}	1.7			V	V_{DD} = 2.5 V to 5.5 V
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
			0.7	V	V_{DD} = 2.5 V to 2.7 V
Input Leakage Current, I_{IL}			2	µA	
Input Capacitance		4	10	pF	
V_{DD} = 4.5 V to 5.5 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{DD} −1			V	I_{SOURCE} = 200 µA
V_{DD} = 2.5 V to 3.6 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{DD} − 0.5			V	I_{SOURCE} = 200 µA
DYNAMIC PERFORMANCE[1]					
Reference Multiplying BW		10		MHz	V_{REF} = ±3.5 V, DAC loaded all 1s
Output Voltage Settling Time					V_{REF} = ±10 V, R_{LOAD} = 100 Ω, C_{LOAD} = 15 pF
					DAC latch alternatively loaded with 0s and 1s
AD5428		30	60	ns	Measured to ±16 mV of FS
AD5440		35	70	ns	Measured to ±4 mV of FS
AD5447		80	120	ns	Measured to ±1 mV of FS

Parameter	Min	Typ	Max	Unit	Conditions
Digital Delay		20	40	ns	Interface delay time
10% to 90% Settling Time		15	30	Ns	Rise and fall time, V_{REF} = 10 V, R_{LOAD} = 100 Ω
Digital-to-Analog Glitch Impulse		2		nV-s	1 LSB change around major carry, V_{REF} = 0 V
Multiplying Feedthrough Error			–75	dB	DAC latches loaded with all 0s. Reference = 10 kHz
Output Capacitance					
$I_{OUT}2$		22	25	pF	DAC latches loaded with all 0s
		10	12	pF	DAC latches loaded with all 1s
$I_{OUT}1$		12	17	pF	DAC latches loaded with all 0s
		25	30	pF	DAC latches loaded with all 1s
Digital Feedthrough		1		nV−s	Feedthrough to DAC output with $\overline{CS}$ high and alternate loading of all 0s and all 1s
Total Harmonic Distortion		−81		dB	V_{REF} = 3.5 V p-p, all 1s loaded, f = 1 kHz
Output Noise Spectral Density		25		nV/√Hz	@ 1 kHz
SFDR Performance (Wideband)					AD5447, 65 k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz f_{OUT}		55		dB	
100 kHz f_{OUT}		63		dB	
50 kHz f_{OUT}		65		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		50		dB	
100 kHz f_{OUT}		60		dB	
50 kHz f_{OUT}		62		dB	
SFDR Performance (Narrow Band)					AD5447, 65 k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz f_{OUT}		73		dB	
100 kHz f_{OUT}		80		dB	
50k Hz f_{OUT}		87		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		70		dB	
100 kHz f_{OUT}		75		dB	
50 kHz f_{OUT}		80		dB	
Intermodulation Distortion					AD5447, 65 k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
f_1 = 400 kHz, f_2 = 500 kHz		65		dB	
f_1 = 40 kHz, f_2 = 50 kHz		72		dB	
Clock = 25 MHz					
f_1 = 400 kHz, f_2 = 500 kHz		51		dB	
f_1 = 40 kHz, f_2 = 50 kHz		65		dB	
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			0.6	µA	T_A = 25°C. Logic inputs = 0 V or V_{DD}
		0.5	10	µA	Logic inputs = 0 V or V_{DD}
Power Supply Sensitivity[1]			0.001	%/%	ΔV_{DD} = ±5%

[1] Guaranteed by design, not subject to production test.

TIMING CHARACTERISTICS

Temperature range for Y version is −40°C to +125°C. Guaranteed by design and characterization, not subject to production test.

All input signals are specified with tr = tf = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. Digital output timing measured with load circuit in Figure 3. V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
Write Mode			
t_1	0	ns min	R/$\overline{W}$ to $\overline{CS}$ setup time
t_2	0	ns min	R/$\overline{W}$ to $\overline{CS}$ hold time
t_3	10	ns min	$\overline{CS}$ low time
t_4	10	ns min	Address setup time
t_5	0	ns min	Address hold time
t_6	6	ns min	Data setup time
t_7	0	ns min	Data hold time
t_8	5	ns min	R/$\overline{W}$ high to $\overline{CS}$ low
t_9	7	ns min	$\overline{CS}$ min high time
Data Readback Mode			
t_{10}	0	ns typ	Address setup time
t_{11}	0	ns typ	Address hold time
t_{12}	5	ns typ	Data access time
	25	ns max	
t_{13}	5	ns typ	Bus relinquish time
	10	ns max	

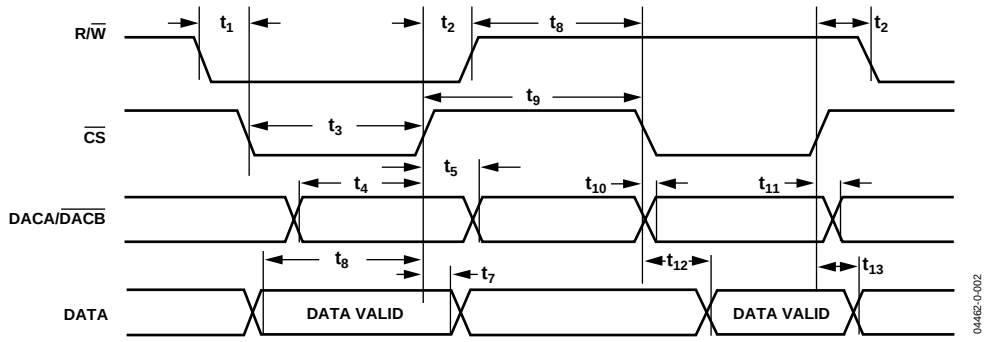


Figure 2. Timing Diagram

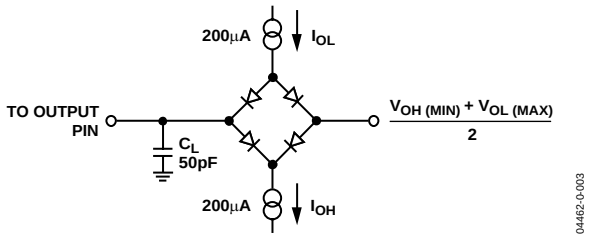


Figure 3. Load Circuit for Data Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	–0.3 V to +7 V
$V_{REF}A$, $V_{REF}B$, $R_{FB}A$, $R_{FB}B$ to DGND	–12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to DGND	–0.3 V to +7 V
Logic Inputs and Output[1]	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range Automotive (Y Version)	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
20-lead TSSOP θ_{JA} Thermal Impedance	143°C/W
24-lead TSSOP θ_{JA} Thermal Impedance	128°C/W
Lead Temperature, Soldering (10 seconds)	300°C
IR Reflow, Peak Temperature (< 20 seconds)	235°C

[1]Overvoltages at DBx, $\overline{CS}$, and $\overline{W}$/R are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

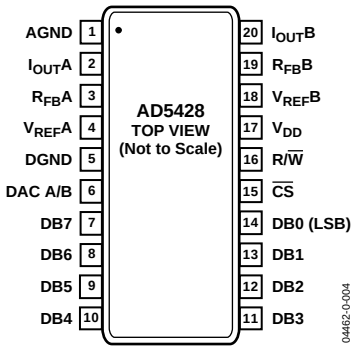


Figure 4. Pin Configuration 20-Lead TSSOP (RU-20)

Table 4. AD5428 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	AGND	DAC Ground Pin. Typically, this pin should be tied to the analog ground of the system, but may be biased to achieve single-supply operation.
2, 20	$I_{OUT}A$, $I_{OUT}B$	DAC Current Outputs.
3, 19	$R_{FB}A$, $R_{FB}B$	DAC Feedback Resistor Pins. Establish voltage output for the DAC by connecting to external amplifier output.
4, 18	$V_{REF}A$, $V_{REF}B$	DAC Reference Voltage Input Terminals.
5	DGND	Digital Ground Pin.
6	DAC A/B	Selects DAC A or B. Low selects DAC A, or, alternatively, high selects DAC B.
7 to14	DB7 to DB0	Parallel Data Bits 7 through 0.
15	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with R/W to load parallel data to the input latch or to read data from the DAC register.
16	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, used in conjunction with $\overline{CS}$ to read back contents of the DAC register.
17	V_{DD}	Positive Power Supply Input. This part can be operated from a supply of 2.5 V to 5.5 V.

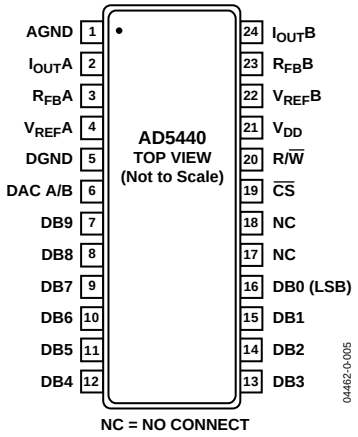


Figure 5. Pin Configuration 24-Lead TSSOP (RU-24)

Table 5. AD5440 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	AGND	DAC Ground pin. Typically, this pin should be tied to the analog ground of the system, but may be biased to achieve single-supply operation.
2, 24	$I_{OUT}A$, $I_{OUT}B$	DAC Current Outputs.
3, 23	$R_{FB}A$, $R_{FB}B$	DAC Feedback Resistor Pins. Establish voltage output for the DAC by connecting to external amplifier output.
4, 22	$V_{REF}A$, $V_{REF}B$	DAC Reference Voltage Input Terminals.
5	DGND	Digital Ground pPin.
6	DAC A/B	Selects DAC A or B. Low selects DAC A, or, alternatively, high selects DAC B.
7 to16	DB9 to DB0	Parallel Data Bits 9 through 0.
19	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register.
20	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, used in conjunction with $\overline{CS}$ to read back contents of the DAC register.
21	V_{DD}	Positive Power Supply Input. This part can be operated from a supply of 2.5 V to 5.5 V.

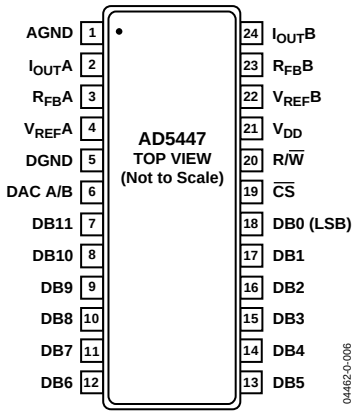


Figure 6. Pin Configuration 24-Lead TSSOP (RU-24)

Table 6. AD5447 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	AGND	DAC Ground pin. Typically, this pin should be tied to the analog ground of the system, but may be biased to achieve single-supply operation.
2, 24	$I_{OUT}A$, $I_{OUT}B$	DAC Current Outputs.
3, 23	$R_{FB}A$, $R_{FB}B$	DAC Feedback Resistor Pins. Establish voltage output for the DAC by connecting to external amplifier output.
4, 22	$V_{REF}A$, $V_{REF}B$	DAC Reference Voltage Input Terminals.
5	DGND	Digital Ground Pin.
6	DAC A/B	Selects DAC A or B. Low selects DAC A, or, alternatively, high selects DAC B.
7 to 18	DB11 to DB0	Parallel Data Bits 11 through 0.
19	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. When $\overline{CS}$ and R/$\overline{W}$ are held low, the latches are transparent; any changes on the data lines will be reflected on the relevant DAC output.
20	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, used in conjunction with $\overline{CS}$ to read back contents of DAC register. When $\overline{CS}$ and R/$\overline{W}$ are held low, the latches are transparent; any changes on the data lines are reflected on the relevant DAC output.
21	V_{DD}	Positive Power Supply Input. This part can be operated from a supply of 2.5 V to 5.5 V.

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is typically expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of −1 LSB max over the operating temperature range ensures monotonicity.

Gain Error
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} − 1 LSB. Gain error of the DACs is adjustable to zero with external resistance.

Output Leakage Current
Output leakage current flows in the DAC ladder switches when these are turned off. For the $I_{OUT}1$ terminal, it can be measured by loading all 0s to the DAC and measuring the $I_{OUT}1$ current. Minimum current flows in the $I_{OUT}2$ line when the DAC is loaded with all 1s.

Output Capacitance
Capacitance from $I_{OUT}1$ or $I_{OUT}2$ to AGND.

Output Current Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For these devices, it is specified with a 100 Ω resistor to ground.

Digital-to-Analog Glitch lmpulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the I_{OUT} pins and subsequently into the following circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1$ terminal, when all 0s are loaded to the DAC.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower-order harmonics are included, such as second to fifth.

$$THD = 20 \log \sqrt{\frac{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}{V_1}}$$

Digital Intermodulation Distortion
Second-order intermodulation distortion (IMD) measurements are the relative magnitude of the fa and fb tones generated digitally by the DAC and the second-order products at 2fa − ffb and 2fb − fa.

Spurious-Free Dynamic Range (SFDR)
SFDR is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of difference in amplitude between the fundamental and the largest harmonically- or nonharmonically-related spur from dc to full Nyquist bandwidth (half the DAC sampling rate, or fs/2). Narrow-band SFDR is a measure of SFDR over an arbitrary window size, in this case 50%, of the fundamental. Digital SFDR is a measure of the usable dynamic range of the DAC when the signal is digitally generated sine wave.

TYPICAL PERFORMANCE CHARACTERISTICS

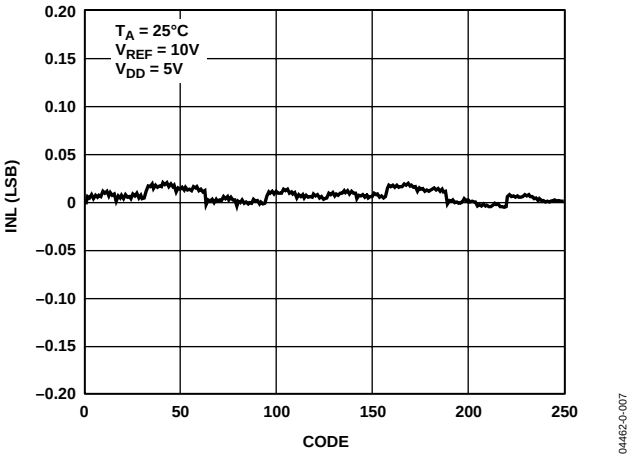


Figure 7. INL vs. Code (8-Bit DAC)

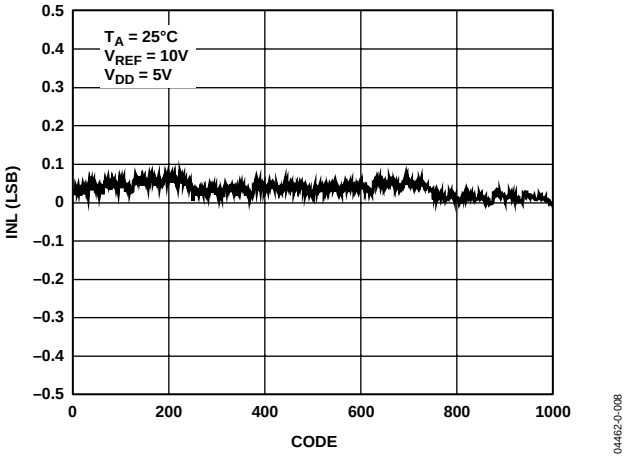


Figure 8. INL vs. Code (10-Bit DAC)

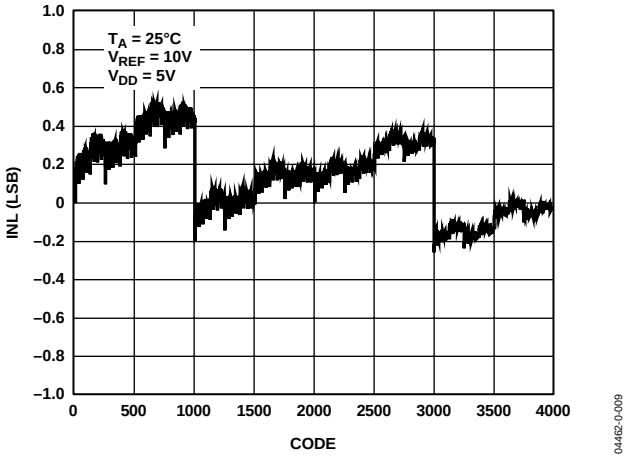


Figure 9. INL vs. Code (12-Bit DAC)

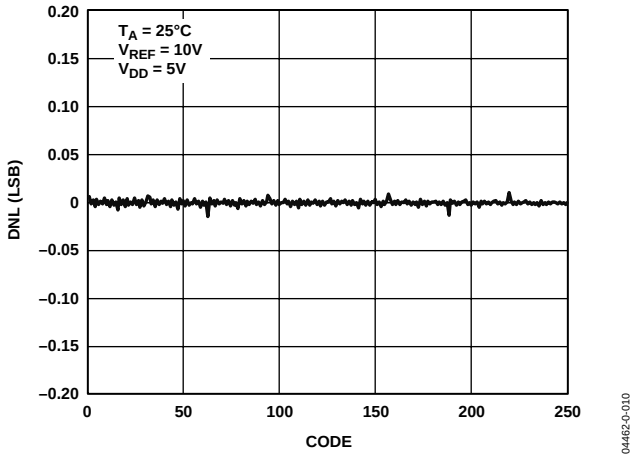


Figure 10. DNL vs. Code (8-Bit DAC)

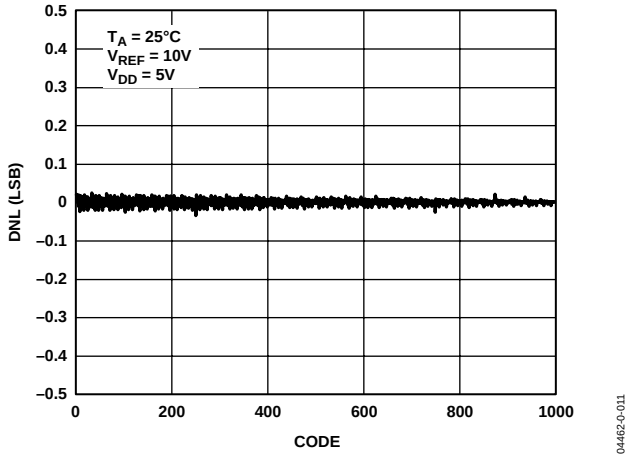


Figure 11. DNL vs. Code (10-Bit DAC)

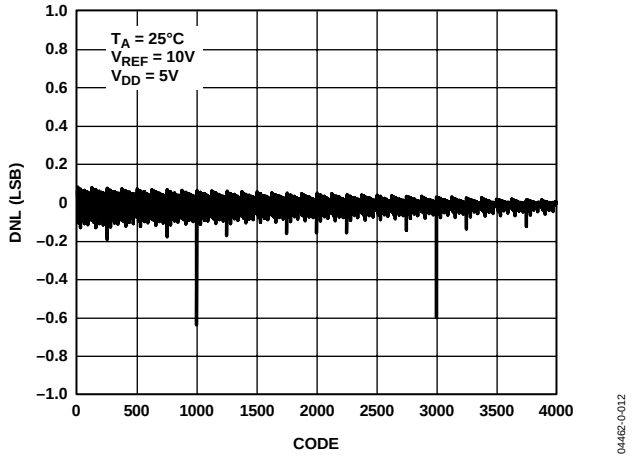


Figure 12. DNL vs. Code (12-Bit DAC)

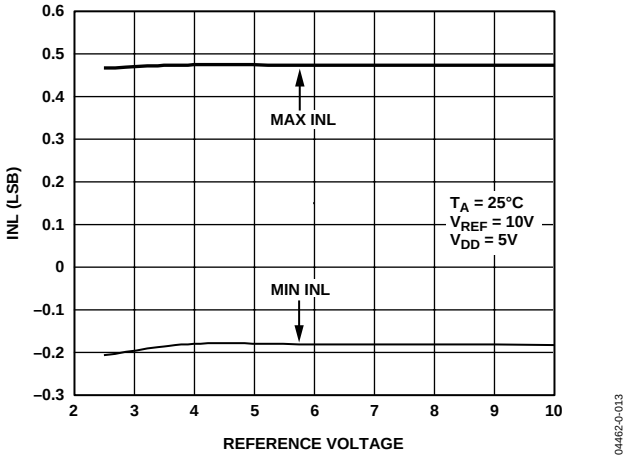


Figure 13. INL vs. Reference Voltage

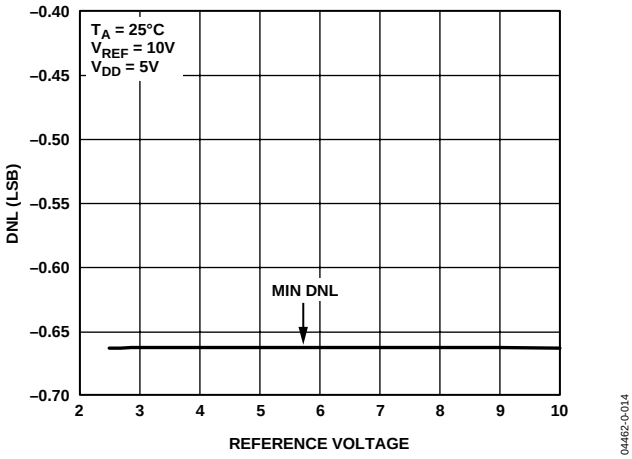


Figure 14. DNL vs. Reference Voltage

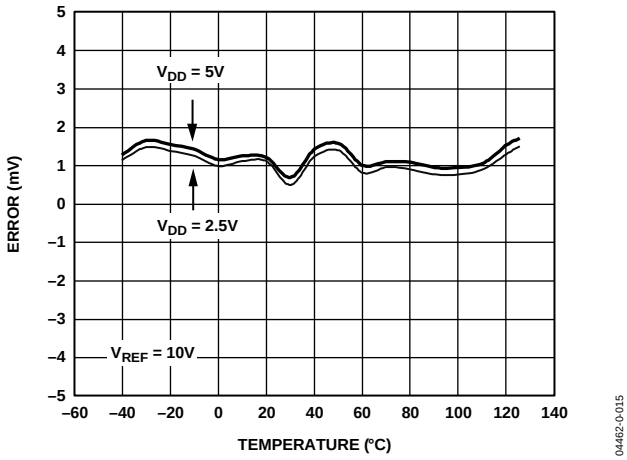


Figure 15. Gain Error vs. Temperature

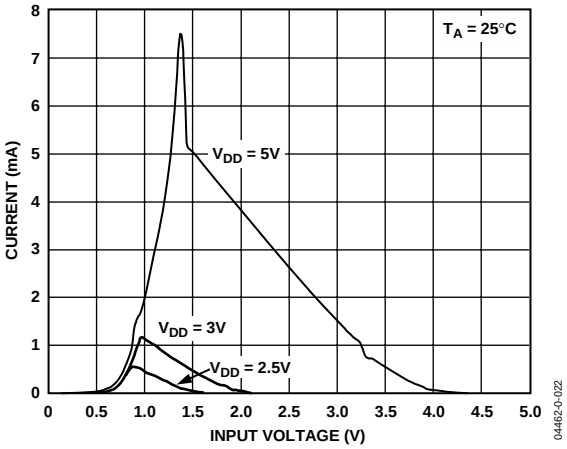


Figure 16. Supply Current vs. Logic Input Voltage

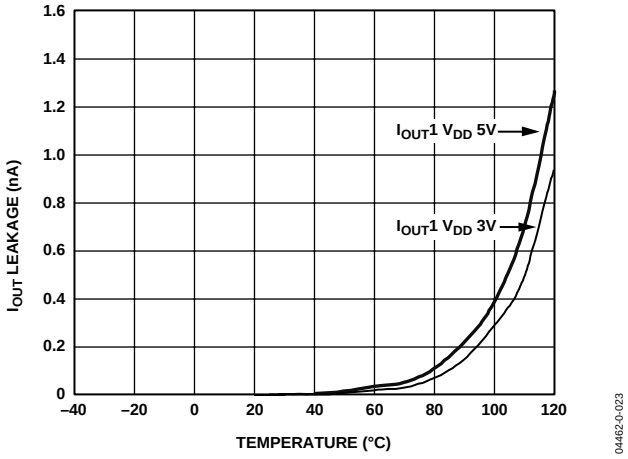


Figure 17. $I_{OUT}1$ Leakage Current vs. Temperature

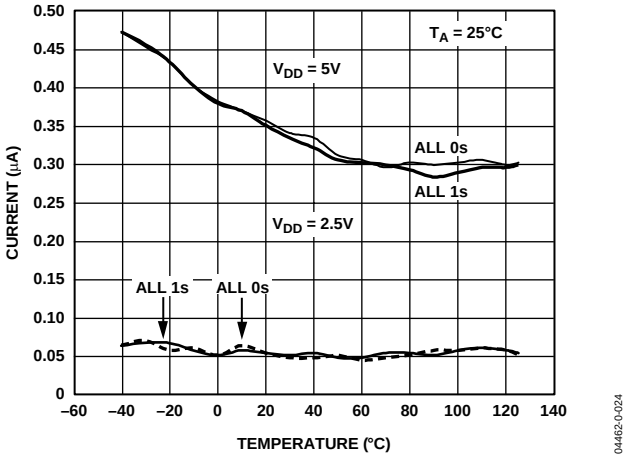


Figure 18. Supply Current vs. Temperature

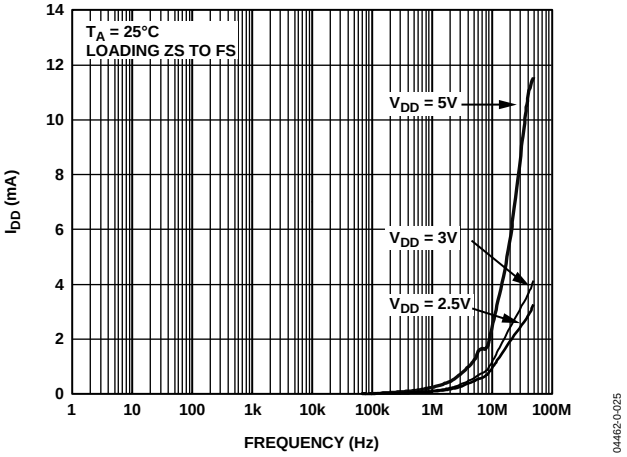


Figure 19. Supply Current vs. Update Rate

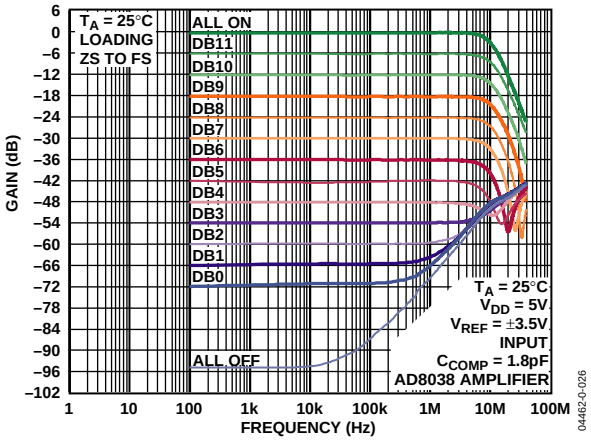


Figure 20. Reference Multiplying Bandwidth vs. Frequency and Code

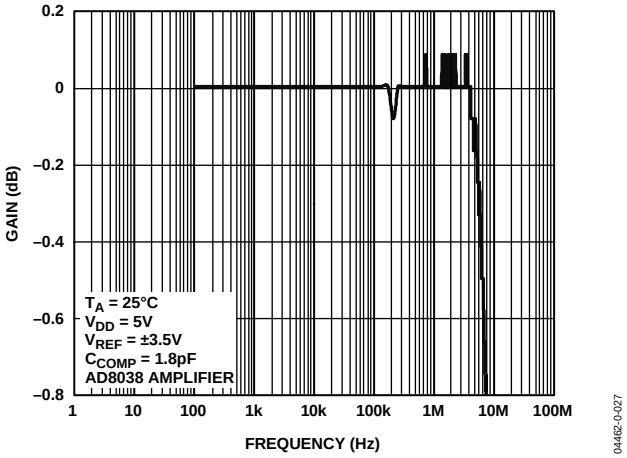


Figure 21. Reference Multiplying Bandwidth–All Ones Loaded

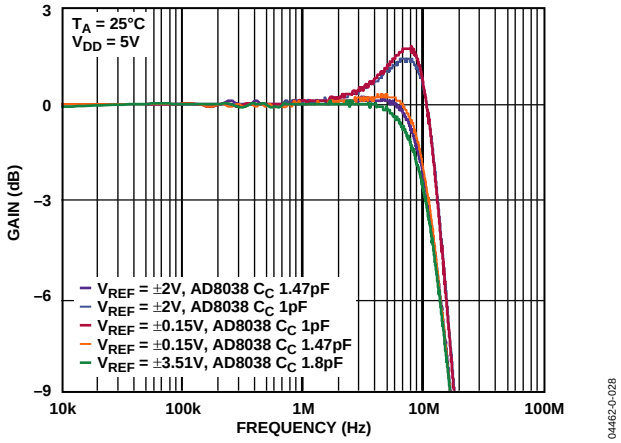


Figure 22. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor

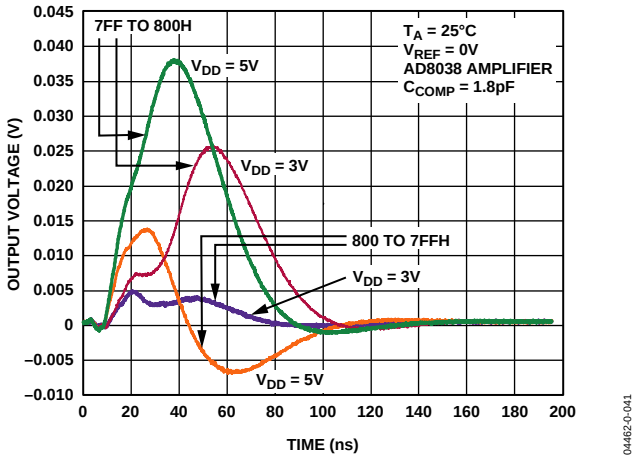


Figure 23. Midscale Transition, V_{REF} = 0 V

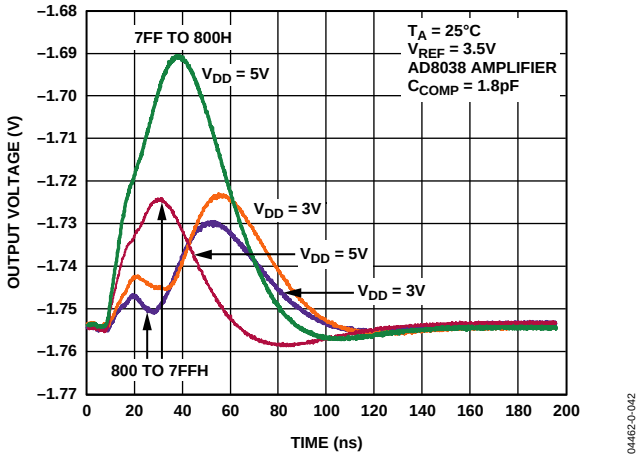


Figure 24. Midscale Transition, V_{REF} = 3.5 V

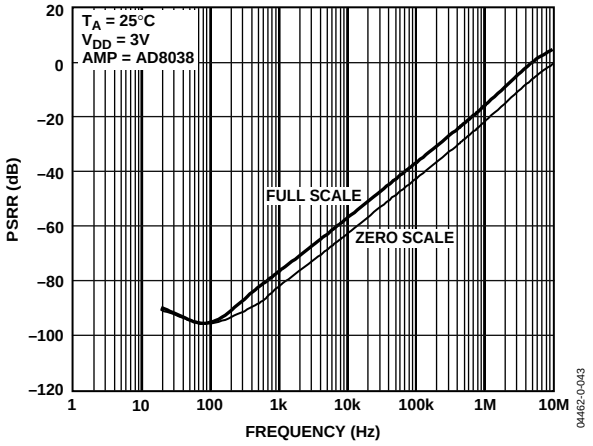


Figure 25. Power Supply Rejection vs. Frequency

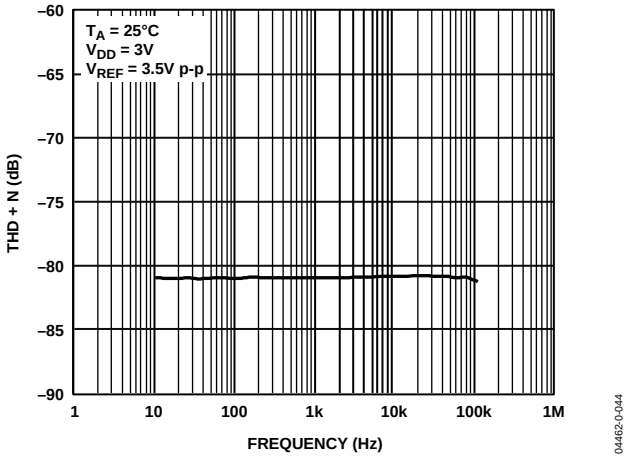


Figure 26. THD + Noise vs. Frequency

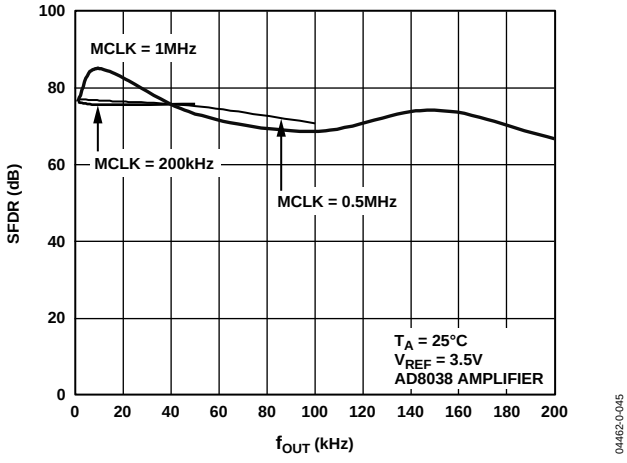


Figure 27. Wideband SFDR vs. f_{OUT} Frequency

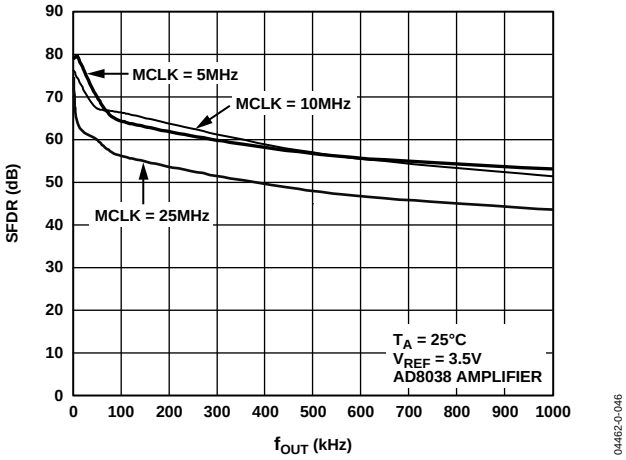


Figure 28. Wideband SFDR vs. f_{OUT} Frequency

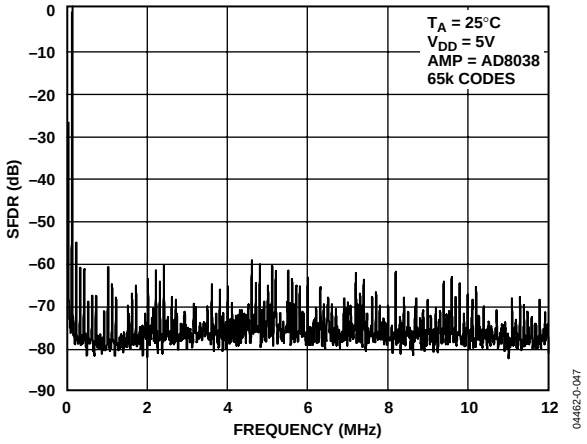


Figure 29. Wideband SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz

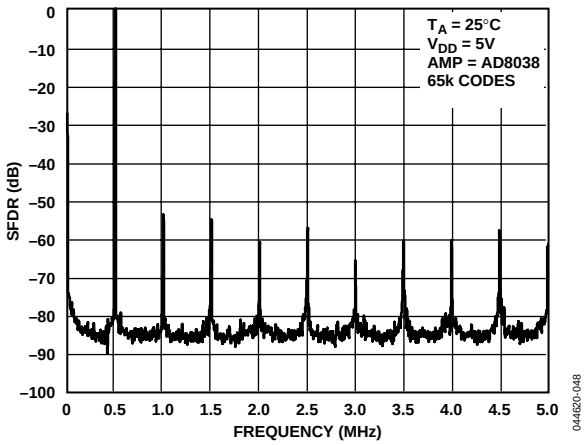


Figure 30. Wideband SFDR, f_{OUT} = 500 kHz, Clock = 10 MHz

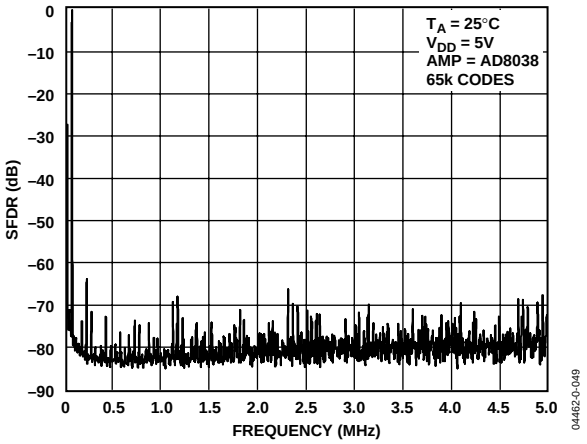


Figure 31. Wideband SFDR, f_{OUT} = 50 kHz, Clock = 10 MHz

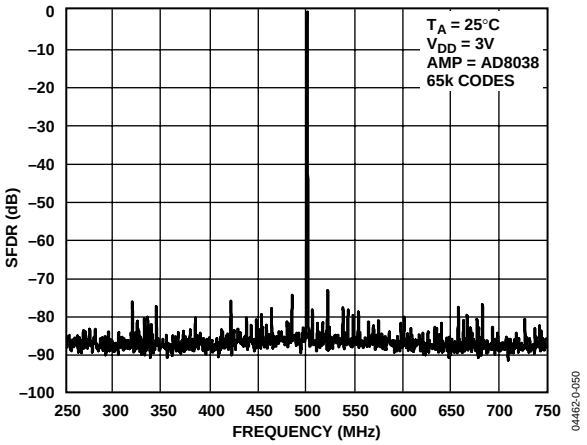


Figure 32. Narrow-Band Spectral Response, f_{OUT} = 500 kHz, Clock = 25 MHz

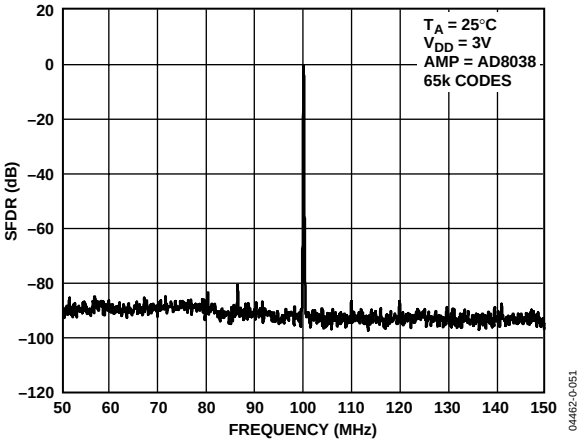


Figure 33. Narrow-Band SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz

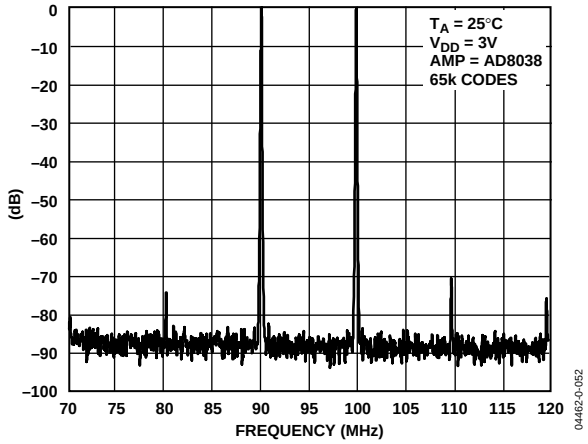


Figure 34. Narrow-Band IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 10 MHz

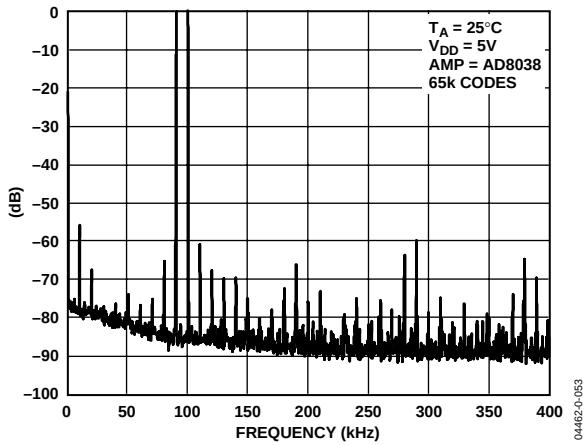


Figure 35. Wideband IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 25 MHz

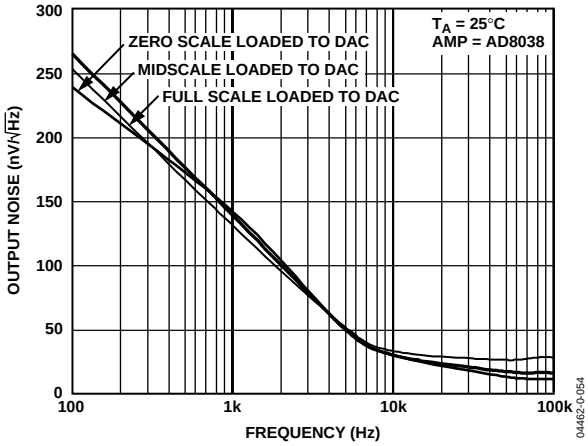


Figure 36. Output Noise Spectral Density

GENERAL DESCRIPTION

The AD5428, AD5440 and AD5447 are dual 8-, 10- and 12-bit current output DACs consisting of a standard inverting R-2R ladder configuration. A simplified diagram for the 8-bit AD5428 is shown in Figure 37. The feedback resistor R_{FB} has a value of R. The value of R is typically 10 kΩ (minimum 8 kΩ and maximum 12 kΩ). If $I_{OUT}1$ and $I_{OUT}2$ are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at V_{REF} is always constant and nominally of value R. The DAC output (I_{OUT}) is code dependent, producing various resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the DAC on the amplifier's inverting input node.

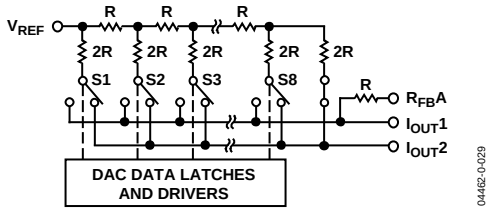


Figure 37. Simplified Ladder

Access is provided to the V_{REF}, R_{FB}, and I_{OUT} terminals of DAC A and DAC B, making the device extremely versatile and allowing it to be configured in several different operating modes, for example, to provide a unipolar output, 4-quadrant multiplication in bipolar mode or in single-supply modes of operation. Note that a matching switch is used in series with the internal R_{FB} feedback resistor. If users attempt to measure R_{FB}, power must be applied to V_{DD} to achieve continuity.

CIRCUIT OPERATION

Unipolar Mode

Using a single op amp, these devices can easily be configured to provide 2-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 38. When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times D/2^n$$

where D is the fractional representation of the digital word loaded to the DAC and n is the resolution of the DAC.

D = 0 to 255 (8-bit AD5428)
= 0 to 1023 (10-bit AD5440)
= 0 to 4095 (12-bit AD5447)

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages. These DACs are designed to operate with either negative or positive reference voltages. The VDD power pin is only used by the internal digital logic to drive the on and off states of the DAC switches.

These DACs are also designed to accommodate ac reference input signals in the range of –10 V to +10 V.

With a fixed 10 V reference, the circuit in Figure 8 gives a unipolar 0 V to –10 V output voltage swing. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication.

The following table shows the relationship between digital code and the expected output voltage for unipolar operation (AD5428, 8-bit device).

Table 7. Unipolar Code Table

Digital Input		Analog Output (V)
1111	1111	$-V_{REF}$ (255/256)
1000	0000	$-V_{REF}$(128/256) = $-V_{REF}$/2
0000	0001	$-V_{REF}$ (1/256)
0000	0000	$-V_{REF}$ (0/256) = 0

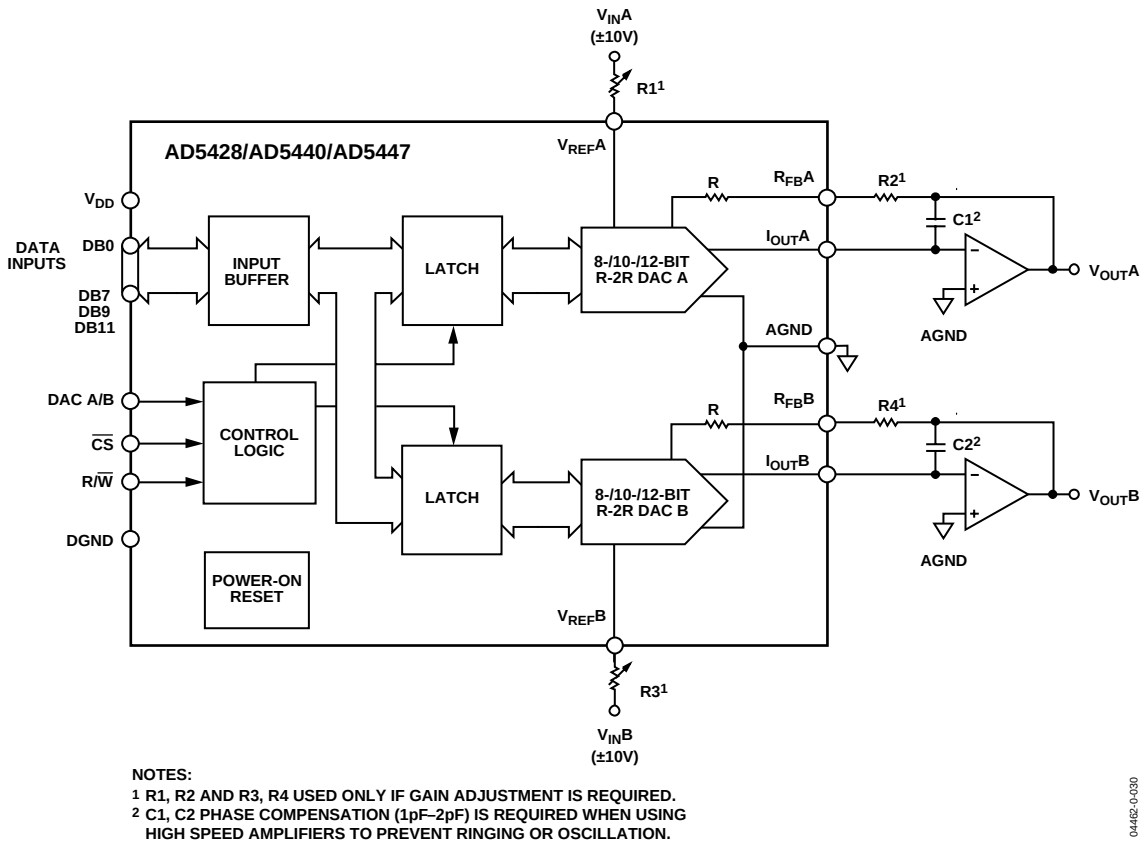


Figure 38. Unipolar Operation

Bipolar Operation

In some applications, it may be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier and some external resistors, as shown in Figure 39. In this circuit, the second amplifier, A2, provides a gain of 2. Biasing the external amplifier with an offset from the reference voltage results in full 4-quadrant multiplying operation. The transfer function of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero ($V_{OUT} = -V_{REF}$) to midscale (V_{OUT} = 0 V) to full scale ($V_{OUT} = +V_{REF}$). When connected in bipolar mode, the output voltage is given by

$$V_{OUT} = \left(V_{REF} \times D / 2^{n-1}\right) - V_{REF}$$

where *D* is the fractional representation of the digital word loaded to the DAC, and *n* is the number of bits.

D = 0 to 255 (AD5428)
= 0 to 1023 (AD5440)
= 0 to 4095 (AD5447)

When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication. Table 8 shows the relationship between digital code and the expected output voltage for bipolar operation (AD5428, 8-bit device).

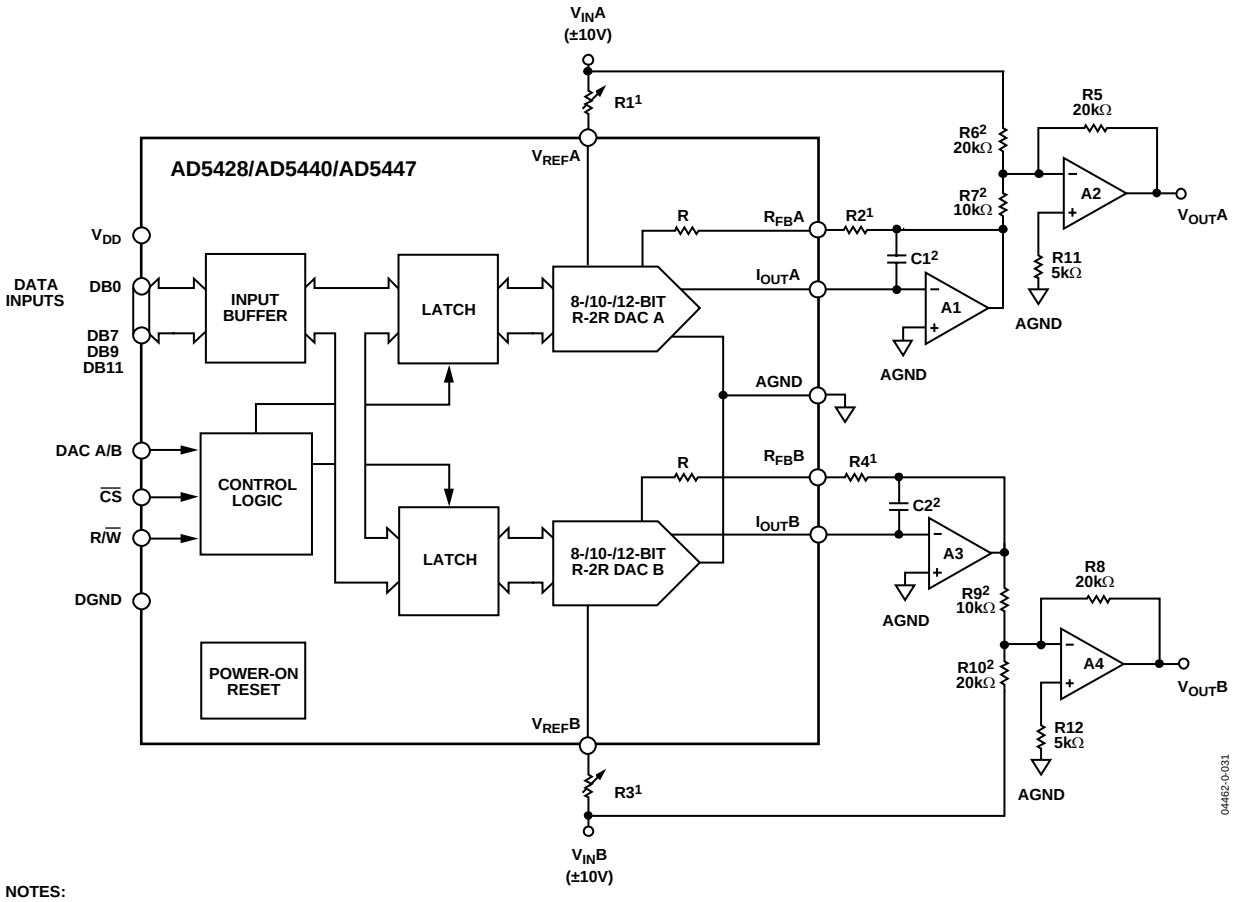
Table 8. Bipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (127/128)
1000 0000	0
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

Stability

In the I-to-V configuration, the IOUT of the DAC and the inverting node of the op amp must be connected as close as possible and proper PCB layout techniques must be employed. Because every code change corresponds to a step function, gain peaking may occur if the op amp has limited GBP and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open loop response which can cause ringing or instability in the closed loop applications circuit.

An optional compensation capacitor, C1, can be added in parallel with R_{FB} for stability, as shown in Figure 38 and in Figure 39. Too small a value of C1 can produce ringing at the output, while too large a value can adversely affect the settling time. C1 should be found empirically, but 1 pF to2 pF is generally adequate for the compensation.



NOTES:
1 R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. ADJUST R1 FOR $V_{OUT}A$ = 0V WITH CODE 10000000 IN DAC A LATCH. ADJUST R3 FOR $V_{OUT}B$ = 0V WITH CODE 10000000 IN DAC B LATCH.
2 MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.
3 C1, C2 PHASE COMPENSATION (1pF–2pF) MAY BE REQUIRED IF A1/A3 IS A HIGH SPEED AMPLIFIER.

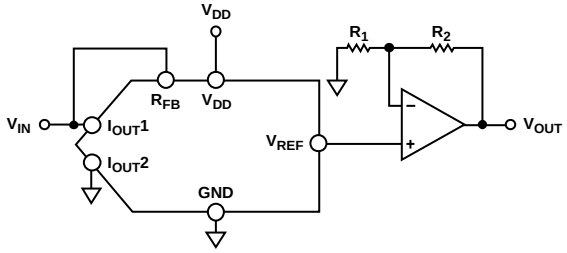
Figure 39. Bipolar Operation (4-Quadrant Multiplication)

SINGLE-SUPPLY APPLICATIONS

Voltage-Switching Mode

Figure 40 shows these DACs operating in voltage-switching mode. The reference voltage, V_{IN}, is applied to the $I_{OUT}1$ pin, $I_{OUT}2$ is connected to AGND, and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is voltage at constant impedance (the DAC ladder resistance), thus an op amp is necessary to buffer the output voltage. The reference input no longer sees constant input impedance, but one that varies with code. So, the voltage input should be driven from a low impedance source.

Note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, their on resistance differs and this degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3 V or an internal diode turns on, exceeding the maximum ratings of the device. In this type of application, the full range of multiplying capability of the DAC is lost.



NOTES:
1 ADDITIONAL PINS OMITTED FOR CLARITY.
2 C1 PHASE COMPENSATION (1pF–2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 40. Single-Supply Voltage-Switching Mode

POSITIVE OUTPUT VOLTAGE

Note the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages. For a positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the resistor's tolerance errors. To generate a negative reference, the reference can be level shifted by an op amp such that the V_{OUT} and GND pins of the reference become the virtual ground and −2.5 V respectively, as shown in Figure 41.

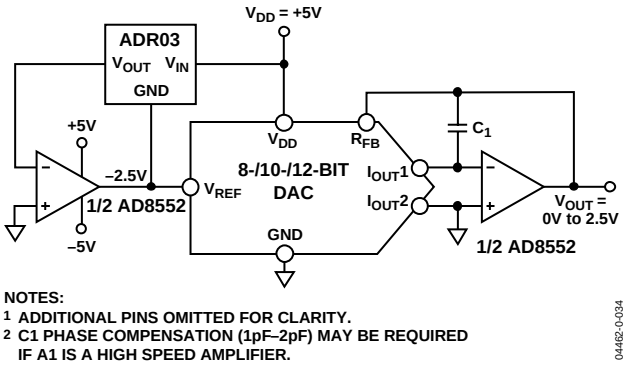


Figure 41. Positive Voltage Output with Minimum Components

ADDING GAIN

In applications where the output voltage is required to be greater than V_{IN}, gain can be added with another external amplifier or it can also be achieved in a single stage. It is important to take into consideration the effect of temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the R_{FB} resistor causes mismatches in the temperature coefficients, resulting in larger gain temperature coefficient errors. Instead, the circuit of Figure 42 shows the recommended method of increasing the gain of the circuit. R_1, R_2, and R_3 should all have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains of >1 are required.

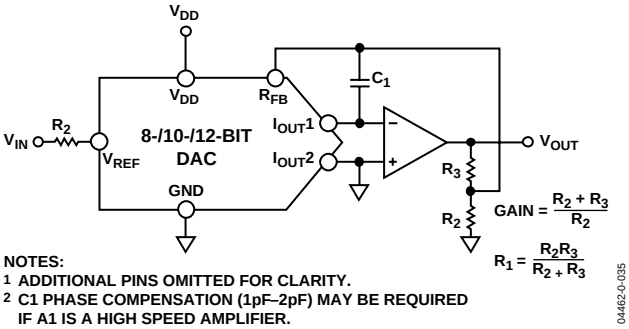


Figure 42. Increasing Gain of Current Output DAC

USED AS A DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Current-steering DACs are very flexible and lend themselves to many different applications. If this type of DAC is connected as the feedback element of an op amp and R_{FB} is used as the input resistor as shown in Figure 43, then the output voltage is inversely proportional to the digital input fraction D.

For $D = 1\text{-}2^n$ the output voltage is

$$V_{OUT} = -V_{IN} / D = -V_{IN} / \left(1 - 2^n\right)$$

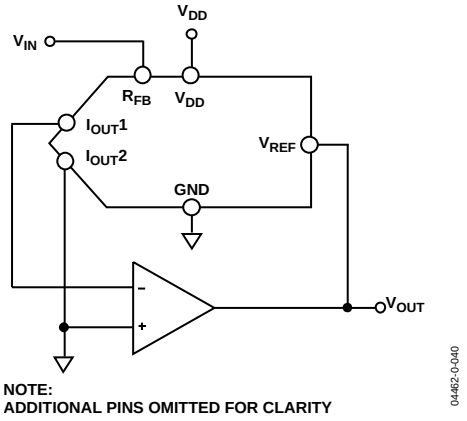


Figure 43. Current-Steering DAC Used as a Divider or Programmable Gain Element

As D is reduced, the output voltage increases. For small values of the digital fraction D, it is important to ensure that the amplifier does not saturate and also that the required accuracy is met. For example, an 8-bit DAC driven with the binary code 0 × 10 (00010000)—that is, 16 decimal—in the circuit of Figure 43 should cause the output voltage to be 16 ×V_{IN}. However, if the DAC has a linearity specification of ± 0.5 LSB, then *D* can, in fact, have the weight anywhere in the range 15.5/256 to 16.5/256 so that the possible output voltage is in the range 15.5 V_{IN} to 16.5 V_{IN}—an error of 3% even though the DAC itself has a maximum error of 0.2%.

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Because only a fraction, D, of the current into the V_{REF} terminal is routed to the $I_{OUT}1$ terminal, the output voltage must change to:

$$\textit{Output Error Voltage Due to DAC Leakage} = \left(\textit{Leakage} \times R\right) / D$$

where *R* is the DAC resistance at the VREF terminal. For a DAC leakage current of 10 nA, R = 10 kΩ and a gain (i.e, a/D) of 16, the error voltage is 1.6 mV.

REFERENCE SELECTION

When selecting a reference for use with the AD54XX series of current output DACs, pay attention to the reference's output voltage temperature coefficient specification. This parameter not only affects the full-scale error, but can also affect the linearity (INL and DNL) performance. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1 LSB over the temperature range 0° to 50°C dictates that the maximum system drift with temperature should be less than 78 ppm/°C. A 12-bit system with the same temperature range to overall specification within 2 LSBs requires a maximum drift of 10 ppm/°C. By choosing a precision reference with low output temperature coefficient this error source can be minimized. Table 9 lists some of the references available from Analog Devices, Inc. that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an op amp is multiplied by the variable gain (due to the code-dependent output resistance of the DAC) of the circuit. A change in the noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the change in output between the two codes and gives rise to a differential linearity error, which if too large might cause the DAC to be nonmonotonic. The input offset voltage should be <1/4 LSB to ensure monotonic behavior when stepping through codes.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor, R_{FB}. Most op amps have input bias currents low enough to prevent significant errors in 12-bit applications.

In voltage-switching circuits, common-mode rejection of the op amp is important because it produces a code-dependent error at the voltage output of the circuit. Most op amps have adequate common-mode rejection for use at 8-, 10-, and 12-bit resolution.

Provided the DAC switches are driven from true wideband, low impedance sources (V_{IN} and AGND), they settle quickly. Thus, the slew rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, it is important to minimize capacitance at the V_{REF} node (voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which in turns requires an amplifier that can handle rail-to-rail signals. Analog Devices, Inc. provides a large variety of single-supply amplifiers.

PARALLEL INTERFACE

Data is loaded to the AD5428/ AD5440/ AD5447 in the format of an 8-, 10-, or 12-bit parallel word. Control lines $\overline{CS}$ and R/$\overline{W}$ allow data to be written to or read from the DAC register. A write event takes place when $\overline{CS}$ and R/$\overline{W}$ are brought low, data available on the data lines fills the shift register, and the rising edge of CS latches the data and transfers the latched data word to the DAC register. The DAC latches are not transparent, thus a write sequence must consist of a falling and rising edge on $\overline{CS}$ to ensure data is loaded to the DAC register and its analog equivalent reflected on the DAC output.

A read event takes place when R/$\overline{W}$ is held high and $\overline{CS}$ is brought low. Data is loaded from the DAC register back to the input register and out onto the data line where it can be read back to the controller for verification or diagnostic purposes. The input and DAC registers of these devices are not transparent, so a falling and rising edge of $\overline{CS}$ is required to load each data-word.

MICROPROCESSOR INTERFACING

The AD5428/AD5440/AD5447 can be interfaced to a variety of 16-bit microcontrollers or DSP processors. Figure 44 shows the AD54xx DAC interfaced to a generic 16-bit microcontroller/ DSP processor. Microprocessor interfacing to this family of DACs is via a data bus that uses standard protocol compatible with microcontrollers and DSP processors. The address decoder is used to select DAC A or DAC B and also to load parallel data to the input latch or to read data from the DAC using an AND gate.

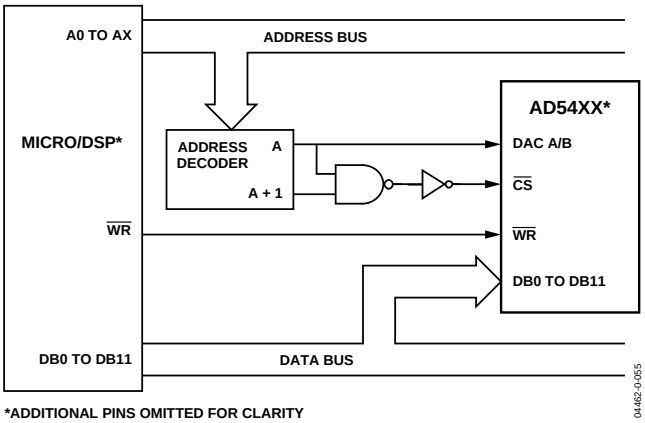


Figure 44. AD54xx to Parallel Interface

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5428/AD5440/AD5447 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

These DACs should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the soldered side.

It is good practice to employ compact, minimum lead length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error. To maximize on high frequency performance, the I-to-V amplifier should be located as close to the device as possible.

EVALUATION BOARD FOR THE DACS

The evaluation board consists of a DAC and a current to voltage amplifier AD8065. Included on the evaluation board is a 10 V reference, ADR01. An external reference may also be applied via an SMB input.

The evaluation kit consists of a CD-ROM with self-installing PC software to control the DAC. The software simply allows the user to write a code to the device.

POWER SUPPLIES FOR THE EVALUATION BOARD

The board requires ±12 V, and +5 V supplies. The +12 V V_{DD} and Vss are used to power the output amplifier, while the +5 V is used to power the DAC (V_{DD1}) and transceivers (V_{CC}).

Both supplies are decoupled to their respective ground plane with 10µF tantalum and 0.1µF ceramic capacitors.

Table 9. Suitable ADI Precision References Recommended for Use with AD5428/AD5440/AD5447 DACs

Reference	Output Voltage	Initial Tolerance	Temperature Drift	0.1 Hz to 10 Hz noise	Package
ADR01	10 V	0.1%	3 ppm/°C	20 µV p-p	SC70, TSOT, SOIC
ADR02	5 V	0.1%	3 ppm/°C	10 µV p-p	SC70, TSOT, SOIC
ADR03	2.5 V	0.2%	3 ppm/°C	10 µV p-p	SC70, TSOT, SOIC
ADR425	5 V	0.04%	3 ppm/°C	3.4 µV p-p	MSOP, SOIC

Table 10. Precision ADI Op Amps Suitable for Use with AD5428/AD5440/AD5447 DACs

Part #	Max Supply Voltage V	V_{OS} (max) µVI_B(max) nA	I_B (max) nA	GBP MHz	Slew Rate V/µs
OP97	±20	25	0.1	0.9	0.2
OP1177	±18	60	2	1.3	0.7
AD8551	+6	5	0.05	1.5	0.4

Table 11. High Speed ADI Op Amps Suitable for Use with AD5428/AD5440/AD5447 DACs

Part #	Max Supply Voltage V	BW @ A_{CL} MHz	Slew Rate V/µs	V_{OS} (max) µV	I_B (max) nA
AD8065	±12	145	180	1500	0.01
AD8021	±12	200	100	1000	1000
AD8038	±5	350	425	3000	0.75

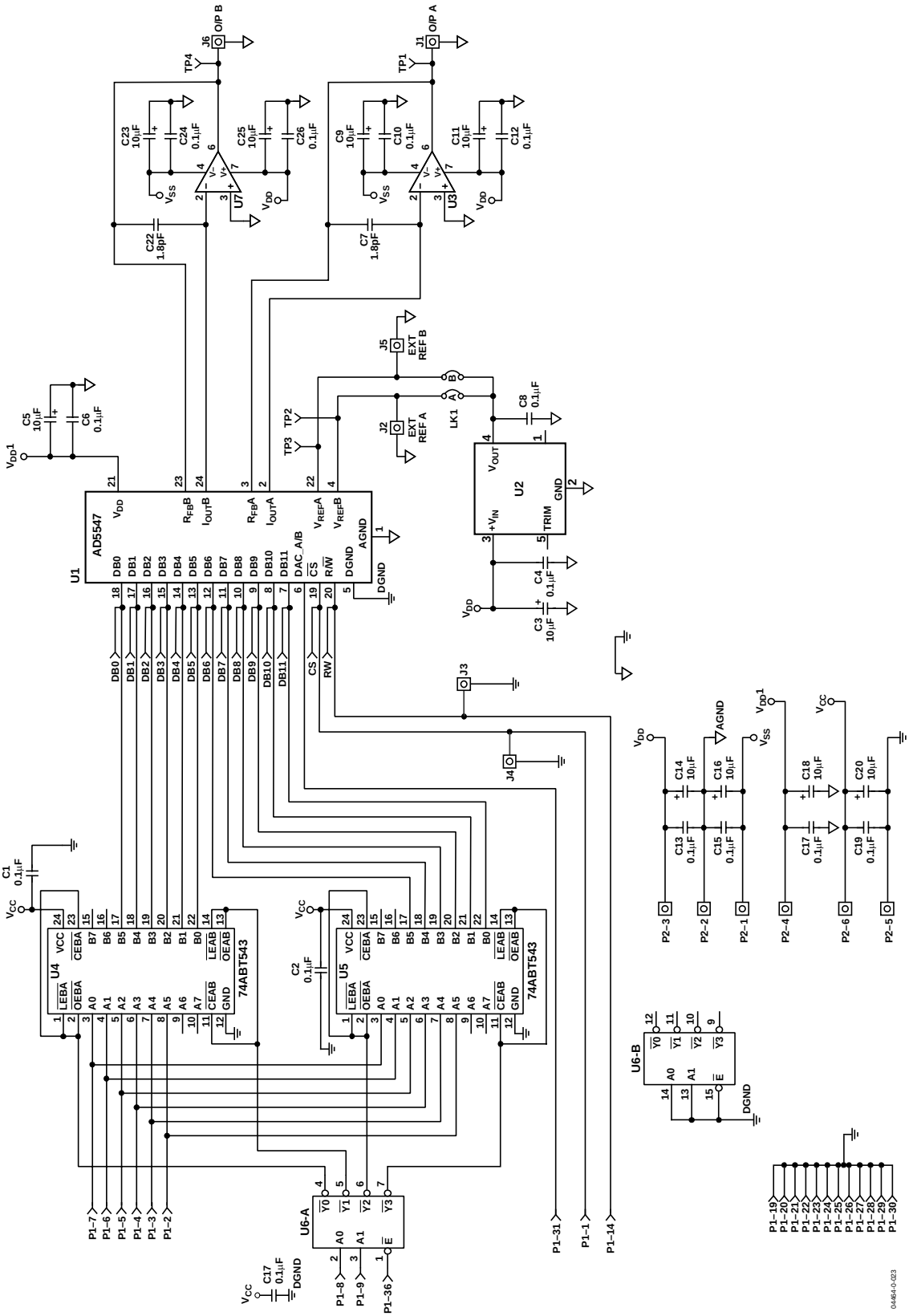


Figure 45. Schematic of AD5428/AD5440/AD5447 Evaluation Board

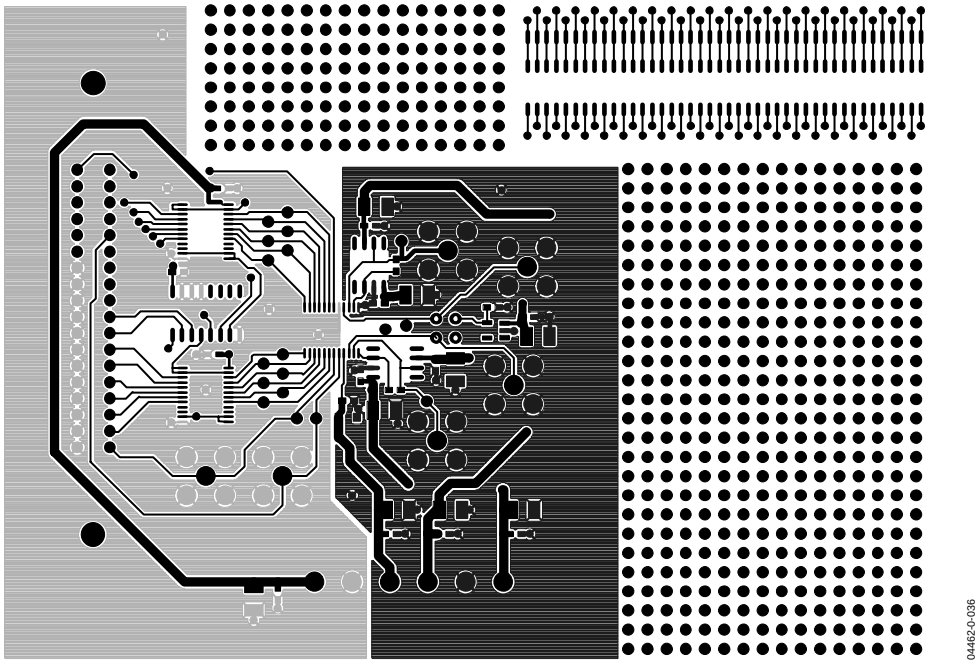


Figure 46. Component-Side Artwork

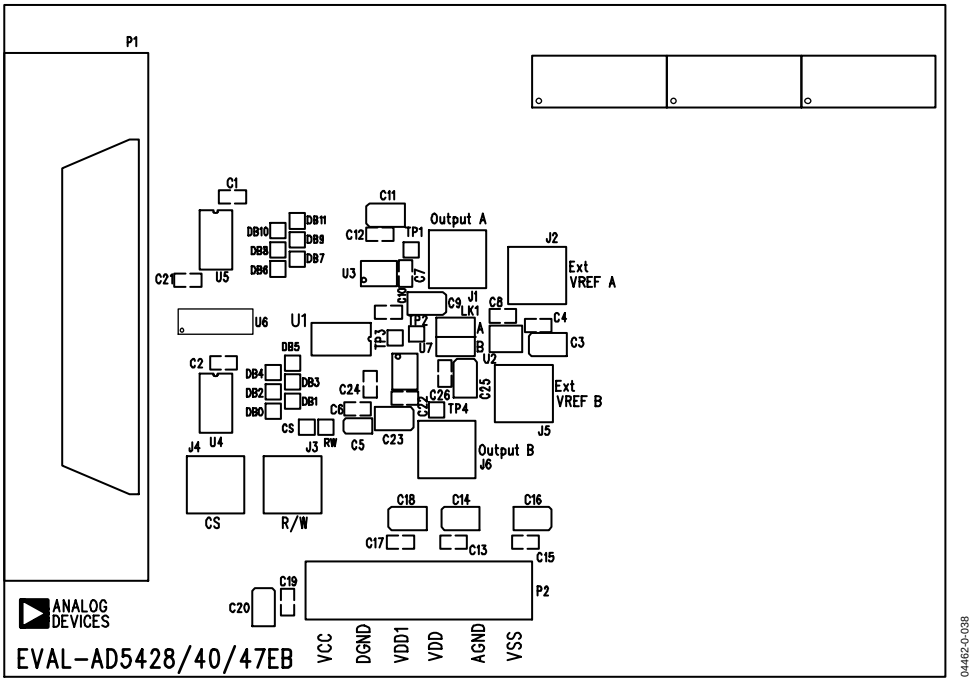


Figure 47. Silkscreen—Component-Side View (Top Layer)

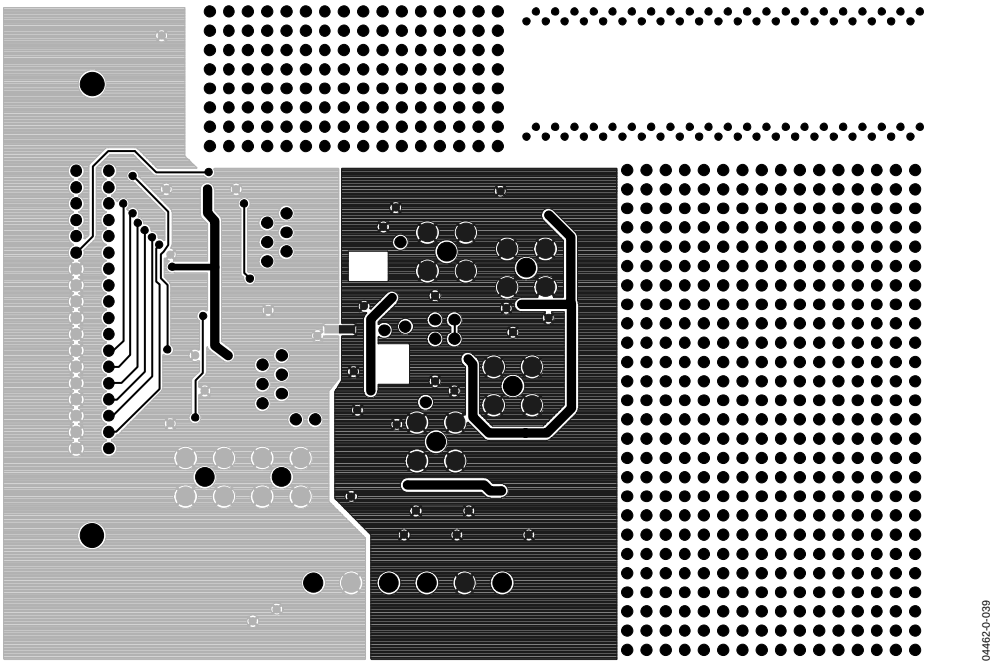


Figure 48. Solder-Side Artwork

BILL OF MATERIALS

Table 12.

Name	Part Description	Value	Tolerance (%)	Stock Code
C1	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C2	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C3	Tantalum Capacitor—Taj Series	10 uF 20 V	10	FEC 197-427
C4	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C5	Tantalum Capacitor—Taj Series	10 uF 10 V	10	FEC 197-130
C6	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C7	NPO Ceramic Capacitor	1.8 pF	10	FEC 721-876
C8	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C9	Tantalum Capacitor—Taj Series	10 uF 20 V	10	FEC 197-427
C10	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C11	Tantalum Capacitor—Taj Series	10 uF 20 V	10	FEC 197-427
C12	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C13	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C14	Tantalum Capacitor—Taj Series	10 uF 20 V	10	FEC 197-427
C15	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C16	Tantalum Capacitor—Taj Series	10 uF 20 V	10	FEC 197-427
C17	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C18	Tantalum Capacitor—Taj Series	10 uF 20 V	10	FEC 197-427
C19	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C20	Tantalum Capacitor—Taj Series	10 uF 20 V	10	FEC 197-427
C21	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C22	NPO Ceramic Capacitor	1.8 pF	10	FEC 721-876
C23	Tantalum Capacitor—Taj Series	10 uF 20 V	10	FEC 197-427
C24	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
C25	Tantalum Capacitor—Taj Series	10 uF 20 V	10	FEC 197-427
C26	X7R Ceramic Capacitor	0.1 uF	10	FEC 499-675
CS, DB0-11	Red Testpoint			FEC 240-345 (Pack)
J1-6	SMB Socket			FEC 310-682
J2	SMB Socket			FEC 310-682
J3	SMB Socket			FEC 310-682
J4	SMB Socket			FEC 310-682
J5	SMB Socket			FEC 310-682
J6	SMB Socket			FEC 310-682
LK1	3-Pin Header (2x2)			FEC 511-791&528-456
P1	36-Pin Centronics Connector			FEC 147-753
P2	6-Pin Terminal Block			FEC 151-792
RW	Red Testpoint			FEC 240-345 (Pack)
TP1 to 4	Red Testpoint			FEC 240-345 (Pack)
U1	AD5428/AD5440/AD5447			AD5428YRU / AD5440YRU / AD5447YRU
U2	ADR01			ADR01AR
U3	AD8065			AD8065AR
U4, U5	74ABT543			Fairchild 74ABT543CMTC
U6	74139			CD74HCT139M
U7	AD8065			AD8065AR
Each Corner	Rubber Stick-On Feet			FEC 148-922

OVERVIEW OF AD54xx DEVICES

Table 13.

Part No.	Resolution	No. DACs	INL(LSB)	Interface	Package	Features
AD5424	8	1	±0.25	Parallel	RU-16, CP-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5426	8	1	±0.25	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5428	8	2	±0.25	Parallel	RU-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5429	8	2	±0.25	Serial	RU-10	10 MHz BW, 50 MHz Serial
AD5450	8	1	±0.25	Serial	RJ-8	10 MHz BW, 50 MHz Serial
AD5432	10	1	±0.5	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5433	10	1	±0.5	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5439	10	2	±0.5	Serial	RU-16	10 MHz BW, 50 MHz Serial
AD5440	10	2	±0.5	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5451	10	1	±0.25	Serial	RJ-8	10 MHz BW, 50 MHz Serial
AD5443	12	1	±1	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5444	12	1	±0.5	Serial	RM-8	10 MHz BW, 50 MHz Serial
AD5415	12	2	±1	Serial	RU-24	10 MHz BW, 58 MHz Serial
AD5445	12	2	±1	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5447	12	2	±1	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5449	12	2	±1	Serial	RU-16	10 MHz BW, 50 MHz Serial
AD5452	12	1	±0.5	Serial	RJ-8, RM-8	10 MHz BW, 50 MHz Serial
AD5446	14	1	±1	Serial	RM-8	10 MHz BW, 50 MHz Serial
AD5453	14	1	±2	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz Serial
AD5553	14	1	±1	Serial	RM-8	4 MHz BW, 50 MHz Serial Clock
AD5556	14	1	±1	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width
AD5555	14	2	±1	Serial	RM-8	4 MHz BW, 50 MHz Serial Clock
AD5557	14	2	±1	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width
AD5543	16	1	±2	Serial	RM-8	4 MHz BW, 50 MHz Serial Clock
AD5546	16	1	±2	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width
AD5545	16	2	±2	Serial	RU-16	4 MHz BW, 50 MHz Serial Clock
AD5547	16	2	±2	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width

OUTLINE DIMENSIONS

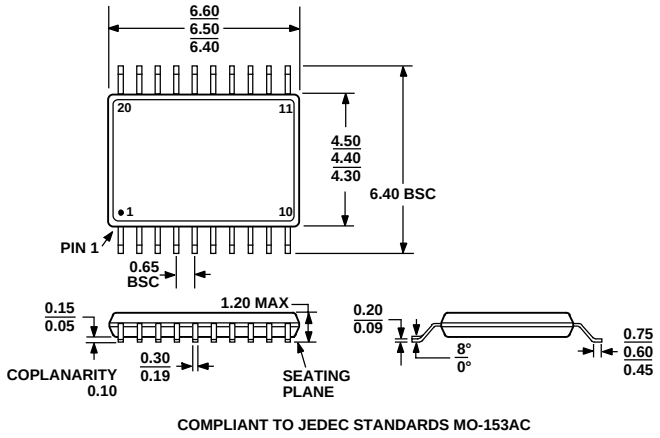


Figure 49. 20-Lead TSSOP
(RU-20)
Dimensions shown in millimeters

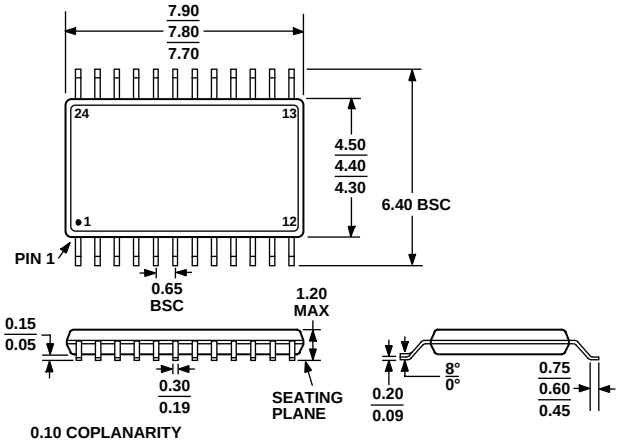


Figure 50. 24-Lead TSSOP
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Resolution	INL (LSBs)	Temperature Range	Package Description	Package Option
AD5428YRU	8	±0.5	–40 °C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5428YRU-REEL	8	±0.5	–40 °C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5428YRU-REEL7	8	±0.5	–40 °C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5440YRU	10	±0.5	–40 °C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-24
AD5440YRU-REEL	10	±0.5	–40 °C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-24
AD5440YRU-REEL7	10	±0.5	–40 °C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-24
AD5447YRU	12	±1	–40 °C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-24
AD5447YRU-REEL	12	±1	–40 °C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-24
AD5447YRU-REEL7	12	±1	–40 °C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-24
EVAL-AD5428EB				Evaluation Kit	
EVAL-AD5440EB				Evaluation Kit	
EVAL-AD5447EB				Evaluation Kit	

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