大容量積層セラミックコンデンサ
HIGH VALUE MULTILAYER CERAMIC CAPACITORS

OPERATING TEMP.	BJ	BJ	−25～+85℃
		X7R	−55～+125℃
		X5R	−55～+85℃
	F	F	−25～+85℃
		Y5V	−30～+85℃

フロー／WAVE　リフロー／REFLOW

特長　FEATURES

・電極にNi金属を使用し、端子電極部にメッキをしてあることにより、はんだ付け性および耐熱性にすぐれ、マイグレーションもほとんど発生せず、高い信頼性を示します
・等価直列抵抗(ESR)が小さく、ノイズ吸収性にすぐれています。特にタンタルおよびアルミ電解コンデンサに比較した場合
・高い許容リップル電流値
・高い定格電圧でありながら小型形状
・絶縁抵抗、破壊電圧が高く信頼性にすぐれる
等の特徴があります

・The use of Nickel(Ni) as material for both the internal and external electrodes improves the solderability and heat resistance characteristics. This almost completely eliminates migration and raises the level of reliability significantly.
・Low equivalent series resistance(ESR) provides excellent noise absorption characteristics.
・Compared to tantalum or aluminum electrolytic capacitors these ceramic capacitors offer a number of excellent features, including:
Higher permissible ripple current values
Smaller case sizes relative to rated voltage
Improved reliability due to higher insulation resistance and breakdown voltage.

用途　APPLICATIONS

・デジタル回路全般
・電源バイパスコンデンサ
液晶モジュール用
液晶駆動電圧ライン用
電源電圧の高いLSI、IC、OPアンプ用
・平滑コンデンサ
DC-DCコンバータ(入力、出力側用)
スイッチング電源(2次側用)

・General digital circuit
・Power supply bypass capacitors
Liquid crystal modules
Liquid crystal drive voltage lines
LS I, I C, converters(both for input and output)
・Smoothing capacitors
DC-DC converters (both for input and output)
Switching power supplies (secondary side)

形名表記法　ORDERING CODE

1 定格電圧 (VDC)

A	4
J	6.3
L	10
E	16
T	25
G	35
U	50

2 シリーズ名

M	積層コンデンサ

3 端子電極

K	メッキ品

4 形状寸法 (EIA)L×W(mm)

107(0603)	1.6×0.8
212(0805)	2.0×1.25
316(1206)	3.2×1.6
325(1210)	3.2×2.5
432(1812)	4.5×3.2
550(2220)	5.7×5.0

5 温度特性 (%)

△F	± 30/80
B J	±10

△= スペース

6 公称静電容量 (pF)

例	
473	47,000
105	1,000,000

7 容量許容差

K	±10	%
M	±20	%
Z	± 80/20	%

8 製品厚み (mm)

A	0.8
D	0.85
F	1.15
G	1.25
H	1.5
L	1.6
N	1.9
M	2.5

9 個別仕様

–	標準

10 包装

B	単品(袋づめ)
T	リールテーピング

11 当社管理記号

△	標準品

△= スペース

J M K 3 1 6 B J 1 0 6 M L – T ○
1 2 3 4 5 6 7 8 9 10 11

1 Rated voltage(VDC)

A	4
J	6.3
L	10
E	16
T	25
G	35
U	50

2 Series name

M	Multilayer ceramic capacitors

3 End termination

K	Plated

4 Dimensions(case size)(mm)

107(0603)	1.6×0.8
212(0805)	2.0×1.25
316(1206)	3.2×1.6
325(1210)	3.2×2.5
432(1812)	4.5×3.2
550(2220)	5.7×5.0

5 Temperature characteristics code

△F	Y5V	−30～+85℃ +22／−82%
B J	X7R	−55～+125℃ ±15%
B J	X5R	−55～+85℃ ±15%

△=Blank space

6 Nominal capacitance(pF)

example	
473	47,000
105	1,000,000

7 Capacitance tolerances(%)

K	±10
M	±20
Z	± 80/20

8 Thickness(mm)

A	0.8
D	0.85
F	1.15
G	1.25
H	1.5
L	1.6
N	1.9
M	2.5

9 Special code

–	Standard products

10 Packaging

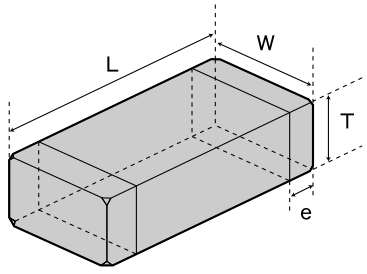
B	Bulk
T	Tape & reel

11 Internal code

△	Standard products

△=Blank space

外形寸法　EXTERNAL DIMENSIONS



Type(EIA)	L	W	T		e
□MK107 (0603)	1.6±0.10 (0.063±0.004)	0.8±0.10 (0.031±0.004)	0.8±0.10 (0.031±0.004)	A	0.35±0.25 (0.014±0.010)
□MK212 (0805) ＊1 ＊2	2.0±0.10 (0.079±0.004)	1.25±0.10 (0.049±0.04)	0.85±0.10 (0.033±0.004)	D	0.5±0.25 (0.020±0.010)
			1.25±0.10 (0.049±0.004)	G	
□MK316 (1206)	3.2±0.15 (0.126±0.006)	1.6±0.15 (0.063±0.006)	0.85±0.10 (0.033±0.004)	D	$0.5^{+0.35}_{-0.25}$ ($0.020^{+0.014}_{-0.010}$)
			1.15±0.10 (0.045±0.004)	F	
			1.25±0.10 (0.049±0.004)	G	
			1.6±0.20 (0.063±0.008)	L	
□MK325 (1210)	3.2±0.30 (0.126±0.012)	2.5±0.20 (0.098±0.008)	0.85±0.10 (0.033±0.004)	D	0.6±0.3 (0.024±0.012)
			1.15±0.10 (0.045±0.004)	F	
			1.5±0.10 (0.059±0.004)	H	
			1.9±0.20 (0.075±0.008)	N	
			2.5±0.20 (0.098±0.008)	M	
□MK432 (1812)	4.5±0.40 (0.177±0.016)	3.2±0.30 (0.126±0.012)	2.5±0.20 (0.098±0.008)	M	0.9±0.6 (0.035±0.024)
□MK550 (2220)	5.7±0.40 (0.224±0.016)	5.0±0.3 (0.197±0.012)	2.5±0.20 (0.098±0.008)	M	0.3～2.0 (0.012～0.079)

注：＊1. ±0.2mm交差、＊2. ±0.15mm交差あり

Note: ＊1. Including dimension tolerance ±0.2mm (±0.008inch).
＊2. Including dimension tolerance ±0.15mm (±0.006inch).

Unit：mm (inch)

概略バリエーション　AVAILABLE CAPACITANCE RANGE

■汎用積層セラミックコンデンサ　General Multilayer Ceramic Capacitors

Cap	Type	107							212											316												325												432			550
	Temp.Char	BJ/X7R		BJ/X5R		F/Y5V			BJ/X7R				BJ/X5R			F/Y5V				BJ/X7R				BJ/X5R		F/Y5V				BJ/X7R				BJ/X5R			F/Y5V				BJ/X5R		F/Y5V	BJ/X5R
	VDC	25	16	10	6.3	16	10	6.3	50	35	25	16	10	16	10	6.3	4	50	16	10	6.3	50	35	25	16	10	16	6.3	50	35	25	16	10	35	25	16	6.3	50	35	25	10	6.3	25	10	6.3	10	6.3	6.3
[μF]	[pF:3digits]																																														
0.022	223	A							D																																						
0.033	333		A						D																																						
0.047	473		A						G		D																																				
0.068	683		A						G		D																																				
0.10	104		A						G																																						
0.15	154			A					G			G							F		D																										
0.22	224			A		A				G		G					D		L		F																										
0.33	334				A					G		G									F																										
0.47	474				A	A						G					G		L		L																										
0.68	684				A							G	G							L	L	F																										
1.0	105					A		A					G	G			G	G			L	L	F					H																			
1.5	155																												N																		
2.2	225							A						G			G				L				G	G	G						N													
3.3	335														G						L	L						N																		
4.7	475														G			G			L	L			G	G				N			N			H									
6.8	685																																														
10.0	106																G		G					L			L			N			N		H	H		M						
22.0	226																										L								M			N			M				
47.0	476																																						N			M	M			
100.0	107																																												M	M	

■低背積層セラミックコンデンサ　Low profile Multilayer Ceramic Capacitors

Cap	Type	212				316				325			
	Temp.Char	BJ/X7R		F/Y5V		BJ/X7R	BJ/X5R	F/Y5V		BJ/X7R	BJ/X5R	F/Y5V	
	VDC	16	10	10	6.3	10	6.3	10	6.3	10	6.3	16	10
[μF]	[pF:3digits]												
0.47	474	D											
0.68	684	D											
1.0	105		D										
2.2	225			D		D							
3.3	335					F	D			D			
4.7	475				D		D	D		F			
6.8	685						F						
10.0	106							F	D		D	F	
22.0	226												F

温度特性コード Temp. char.Code	温度特性 Temperature characteristics					静電容量許容差(%) Capacitance tolerance	tanδ(%) Dissipation factor
	準拠規格 Applicable standard		温度範囲(℃) Temperature range	基準温度(℃) Ref. Temp.	静電容量変化率(%) Capacitance change		
BJ	JIS	BJ	−25～85	20	±10	±20(M) ±10(K)	2.5%max.**
	EIA	X7R*	−55～125	25	±15		
F	JIS	F	−25～85	20	$^{+30}_{-80}$	$^{+80}_{-20}$(Z)	7.0%max.***
	EIA	Y5V	−30～85	25	$^{+22}_{-82}$		

★Some exceptions apply. Refer to the available capacitance range table for the parts which are only available in X5R.
★★3.5%max：LMKtype ; 107type (C≦0.47μF), 212type (C≦1.0μF), 316／325／432type
EMKtype ; 107／212／316／325type
TMKtype ; 316type (C>0.47μF), 325type, 432type
GMKtype ; 212type, 316type, 325type
UMKtype ; 212type (C>0.1μF), 316type (C≧0.47μF), 325type
★★5.0%max：JMKtype ; 107type, 212type, 316type, 325type, 432type, 550type
LMKtype ; 107type (C>0.47μF), 212type (C≧2.2μF)

★★10%max：AMKtype ; 212type
★★★9%max：LMKtype ; 212type, 汎用316type (C=10μF)
低背316type (C=4.7μF)
UMKtype ; 325type
16%max：JMKtype ; 107／212／316／325／432type
LMKtype ; 107／325／432, 汎用316type (C>10μF)

セレクションガイド Selection Guide P.8
アイテム一覧 Part Numbers P.40
特性図 Electrical Characteristics P.44
梱包 Packaging P.78
信頼性 Reliability Data P.80
使用上の注意 Precautions P.86
etc

■107TYPE (0603 case size)

定格電圧 RatedVoltage	形名 Ordering code		公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm] (inch)
25V	TMK107BJ223□A		0.022	BJ/X7R	2.5	R,W	±10% ±20%	0.8±0.10 (0.031±0.004)
16V	EMK107BJ333□A		0.033		3.5			
	EMK107BJ473□A		0.047					
	EMK107BJ683□A		0.068					
	EMK107BJ104□A		0.1					
10V	LMK107BJ154□A		0.15					
	LMK107BJ224□A		0.22					
	LMK107BJ334□A		0.33	BJ/X5R				
	LMK107BJ474□A		0.47			R		
	LMK107BJ684□A		0.68		5			
6.3V	JMK107BJ105□A		1.0					
16V	EMK107F224ZA		0.22	F/Y5V	7	R,W	+80% −20%	0.8±0.10 (0.031±0.004)
	EMK107F474ZA		0.47					
10V	LMK107F105ZA		1.0		16	R		
6.3V	JMK107F225ZA		2.2					

形名の□には静電容量許容差記号が入ります。　□ Please specify the capacitance tolerance code.

■212TYPE (0805 case size)

定格電圧 RatedVoltage	形名 Ordering code		公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm] (inch)
50V	UMK212BJ223□D		0.022	BJ/X7R	2.5	R,W	±10% ±20%	0.85±0.1 (0.033±0.004)
	UMK212BJ333□D		0.033					
	UMK212BJ473□G		0.047					1.25±0.1 (0.049±0.004)
	UMK212BJ683□G		0.068					
	UMK212BJ104□G		0.1					
	UMK212BJ154□G		0.15		3.5			
35V	GMK212BJ224□G		0.22					
	GMK212BJ334□G		0.33					
25V	TMK212BJ473□D		0.047		2.5			0.85±0.1 (0.033±0.004)
	TMK212BJ683□D		0.068					
16V	EMK212BJ154□G		0.15		3.5			1.25±0.1 (0.049±0.004)
	EMK212BJ224□G		0.22					
	EMK212BJ334□G		0.33					
	EMK212BJ474□G		0.47					
	EMK212BJ684□G		0.68					
	EMK212BJ105□G		1.0	BJ/X5R				
10V	LMK212BJ684□G		0.68	BJ/X7R				
	LMK212BJ105□G		1.0					
	LMK212BJ225MG		2.2	BJ/X5R	5	R	±20%	1.25±0.15 (0.049±0.006)
6.3V	JMK212BJ335MG		3.3					
	JMK212BJ475MG		4.7					
4V	AMK212BJ106MG		10		10			1.25±0.20(0.049±0.008)
50V	UMK212F224ZD		0.22	F/Y5V	7	R,W	+80% −20%	0.85±0.1(0.033±0.004)
	UMK212F474ZG		0.47					1.25±0.1 (0.049±0.004)
	UMK212F105ZG		1.0					
16V	EMK212F105ZG		1.0					
	EMK212F225ZG		2.2					
10V	LMK212F475ZG		4.7		9	R		
6.3V	JMK212F106ZG		10		16			

形名の□には静電容量許容差記号が入ります。　□ Please specify the capacitance tolerance code.

アイテム一覧　PART NUMBERS

■316TYPE(1206 case size)

定格電圧 RatedVoltage	形名 Ordering code		公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm] (inch)
50V	UMK316BJ154□F		0.15	BJ/X7R	2.5	R,W	±10% ±20%	1.15±0.1 (0.045±0.004)
	UMK316BJ224□L		0.22					1.6±0.2 (0.063±0.008)
	UMK316BJ474□L		0.47		3.5			
35V	GMK316BJ684□L		0.68					
	GMK316BJ105□L		1.0					
25V	TMK316BJ154□D		0.15		2.5			0.85±0.1 (0.033±0.004)
	TMK316BJ224□F		0.22					1.15±0.1 (0.045±0.004)
	TMK316BJ334□F		0.33					
	TMK316BJ474□L		0.47					1.6±0.2 (0.063±0.008)
	TMK316BJ684□L		0.68		3.5			
	TMK316BJ105□L		1.0					
16V	EMK316BJ684□F		0.68					1.15±0.1 (0.045±0.004)
	EMK316BJ105□F		1.0					
	EMK316BJ225ML		2.2				±20%	1.6±0.2 (0.063±0.008)
	EMK316BJ335ML		3.3	BJ/X5R		R		
	EMK316BJ475ML		4.7					
10V	LMK316BJ335ML		3.3	BJ/X7R				
	LMK316BJ475ML		4.7					
6.3V	JMK316BJ106ML		10	BJ/X5R	5			
50V	UMK316F225ZG		2.2	F/Y5V	7	R,W	+80% −20%	1.25±0.1 (0.049±0.004)
35V	GMK316F225ZG		2.2					
	GMK316F475ZG		4.7			R		
25V	TMK316F225ZG		2.2			R,W		
	TMK316F475ZG		4.7					
10V	LMK316F106ZL		10		9	R		1.6±0.2 (0.063±0.008)
	LMK316F226ZL		22		16			

形名の□には静電容量許容差記号が入ります。　□ Please specify the capacitance tolerance code.

■325TYPE(1210 case size)

定格電圧 RatedVoltage	形名 Ordering code		公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm] (inch)
50V	UMK325BJ105□H		1.0	BJ/X7R	3.5	R,W	±10% ± 20%	1.5±0.1 (0.059±0.004)
35V	GMK325BJ155MN		1.5			R	±20%	1.9±0.2 (0.075±0.008)
	GMK325BJ225MN		2.2	BJ/X5R				
25V	TMK325BJ335MN		3.3	BJ/X7R				
	TMK325BJ475MN		4.7	BJ/X5R				
16V	EMK325BJ475MN		4.7	BJ/X7R				
	EMK325BJ106MN		10	BJ/X5R				
10V	LMK325BJ106MN		10	BJ/X7R				
6.3V	JMK325BJ226MM		22	BJ/X5R	5			2.5±0.2 (0.098±0.008)
50V	UMK325F475ZH		4.7	F/Y5V	9	R	+80% −20%	1.5±0.1 (0.059±0.004)
35V	GMK325F106ZH		10		7			
25V	TMK325F106ZH		10					
10V	LMK325F226ZN		22		16			1.9±0.2 (0.075±0.008)
6.3V	JMK325F476ZN		47					

形名の□には静電容量許容差記号が入ります。　□ Please specify the capacitance tolerance code.

アイテム一覧　PART NUMBERS

■432TYPE(1812 case size)

定格電圧 RatedVoltage	形名 Ordering code		公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm] (inch)
25V	TMK432BJ106MM		10	BJ/X5R	3.5	R	±20%	2.5±0.2 (0.098±0.008)
10V	LMK432BJ226MM		22					
6.3V	JMK432BJ476MM		47		5			
10V	LMK432F476ZM		47	F/Y5V	16	R	+80% −20%	2.5±0.2 (0.098±0.08)
6.3V	JMK432F107ZM		100					

■550TYPE(2220 case size)

定格電圧 RatedVoltage	形名 Ordering code		公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm] (inch)
6.3V	JMK550BJ107MM		100	BJ/X5R	5	R	±20%	2.5±0.2 (0.098±0.008)

アイテム一覧　PART NUMBERS

■212TYPE(0805 case size)

定格電圧 RatedVoltage	形名 Ordering code		公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm] (inch)
16V	EMK212BJ474□D		0.47	BJ/X7R	3.5	R, W	±10% ±20%	0.85±0.1 (0.033±0.004)
	EMK212BJ684□D		0.68					
10V	LMK212BJ105□D		1.0			R		
10V	LMK212F225ZD		2.2	F/Y5V	9	R	+80% −20%	0.85±0.1 (0.033±0.004)
6.3V	JMK212F475ZD		4.7		16			

形名の□には静電容量許容差記号が入ります。

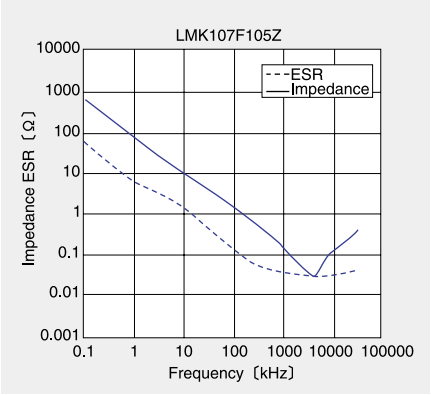
■316TYPE(1206 case size)

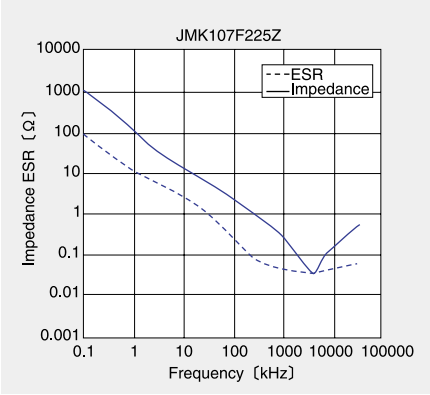
定格電圧 RatedVoltage	形名 Ordering code		公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm] (inch)
10V	LMK316BJ225MD		2.2	BJ/X7R	3.5	R	±20%	0.85±0.1 (0.033±0.004)
	LMK316BJ335MF		3.3					1.15±0.1 (0.045±0.004)
6.3V	JMK316BJ335MD		3.3	BJ/X5R	5			0.85±0.1 (0.033±0.004)
	JMK316BJ475MD		4.7					
	JMK316BJ685MF		6.8					1.15±0.1 (0.045±0.004)
10V	LMK316F475ZD		4.7	F/Y5V	9	R	+80% −20%	0.85±0.1 (0.033±0.004)
	LMK316F106ZF		10		16			1.15±0.1 (0.045±0.004)
6.3V	JMK316F106ZD		10					0.85±0.1 (0.033±0.004)

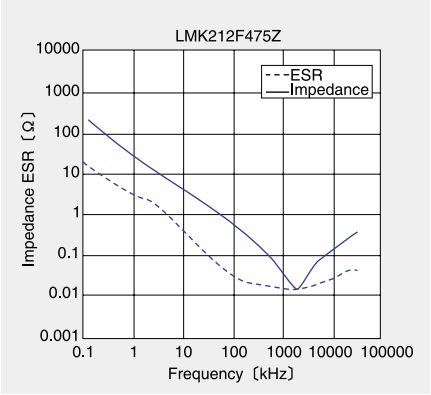
■325TYPE(1210 case size)

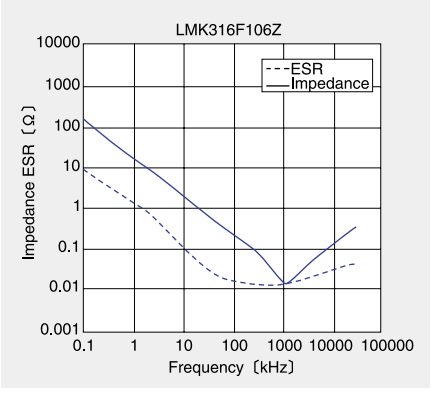
定格電圧 RatedVoltage	形名 Ordering code		公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm] (inch)
10V	LMK325BJ335MD		3.3	BJ/X7R	3.5	R	±20%	0.85±0.1 (0.033±0.004)
	LMK325BJ475MF		4.7					1.15±0.1 (0.045±0.004)
6.3V	JMK325BJ106MF		10	BJ/X5R	5			
	JMK325BJ106MD		10					0.85±0.1 (0.033±0.004)
16V	EMK325F106ZF		10	F/Y5V	7	R	+80% −20%	1.15±0.1 (0.045±0.004)
10V	LMK325F226ZF		22		16			

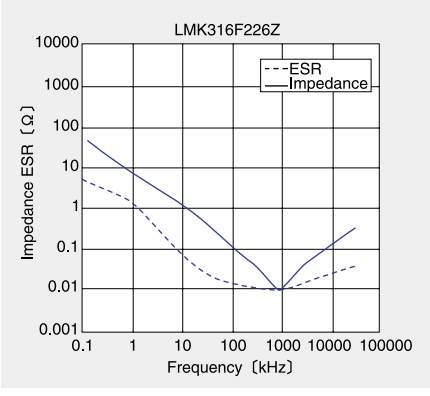
インピーダンス・ESR–周波数特性例　Example of Impedance ESR vs. Frequency characteristics
・当社積層セラミックコンデンサ例　(Taiyo Yuden multilayer ceramic capacitor)

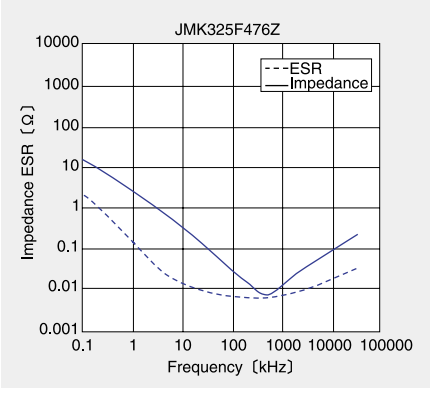


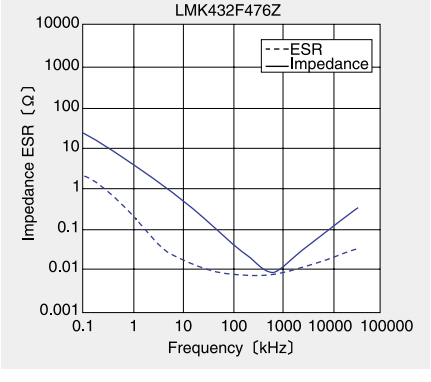


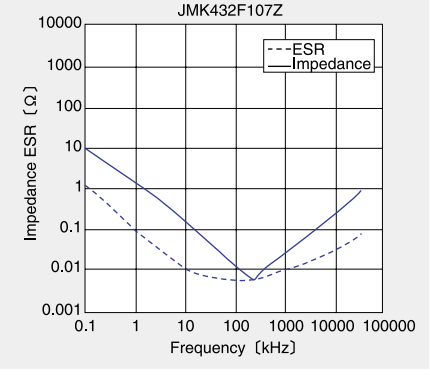












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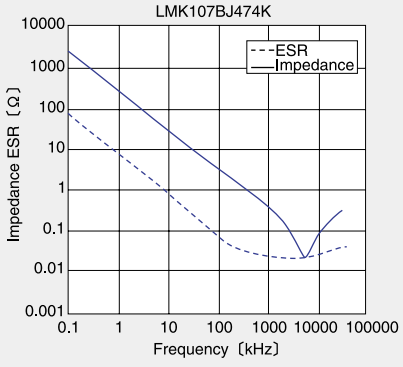

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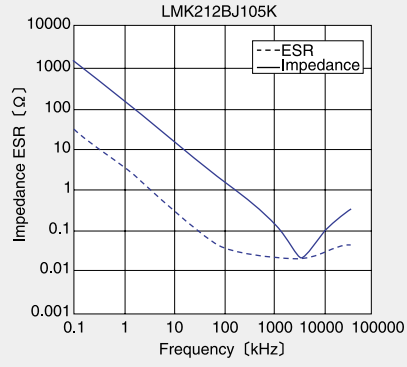

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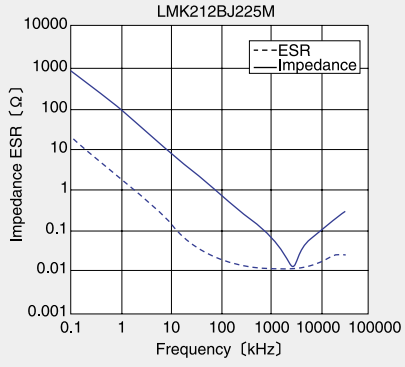

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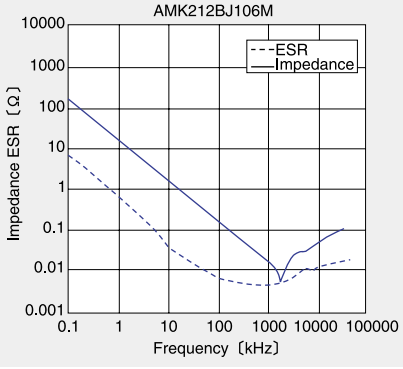

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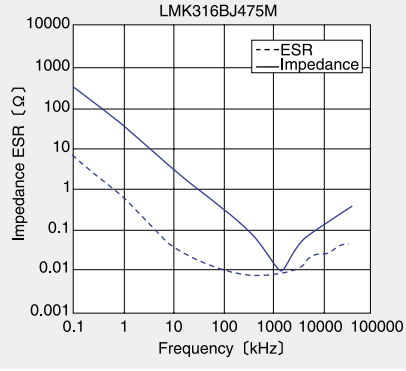

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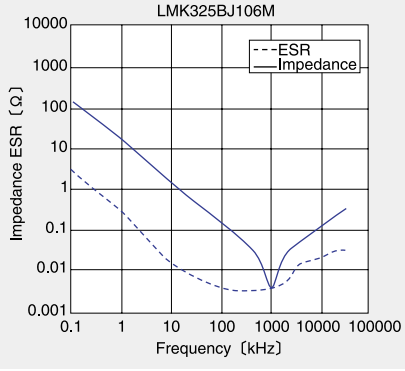

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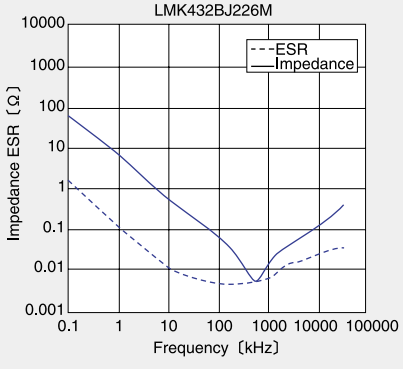

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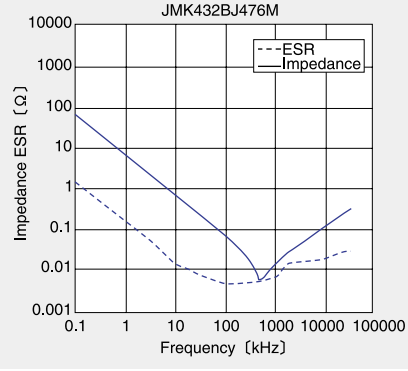

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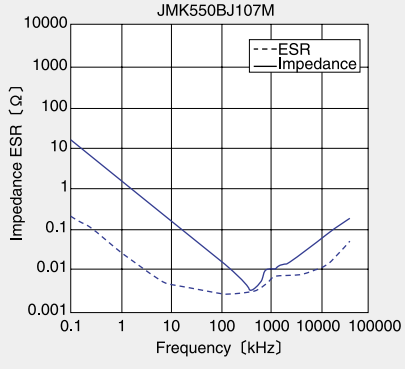
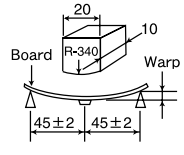
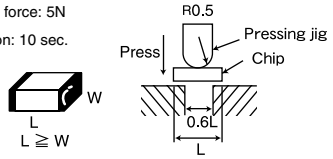
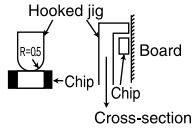


Multilayer Ceramic Capacitor Chips

Item	Specified Value				Test Methods and Remarks
	Temperature Compensating (Class 1)		High Permitivity (Class 2)		
	Standard	High Frequency Type	Standard Note1	High Value	
1.Operating Temperature Range	−55 to +125℃		B：−55 to +125℃ F：−25 to +85℃	−25 to +85℃	High Capacitance Type BJ(X7R)：−55 to +125℃ BJ(X5R)：−55 to +85℃ F(Y5V)：−30 to +85℃
2.Storage Temperature Range	−55 to +125℃		B：−55 to +125℃ F：−25 to +85℃	−25 to +85℃	High Capacitance Type BJ(X7R)：−55 to +125℃ BJ(X5R)：−55 to +85℃ F(Y5V)：−30 to +85℃
3.Rated Voltage	50VDC,25VDC, 16VDC	16VDC	50VDC,25VDC	50VDC,35VDC,25VDC 16VDC,10VDC,6.3VDC 4DVC	
4.Withstanding Voltage Between terminals	No breakdown or damage	No abnormality	No breakdown or damage		Applied voltage: Rated voltage×3 (Class 1) Rated voltage×2.5 (Class 2) Duration: 1 to 5 sec. Charge/discharge current: 50mA max. (Class 1,2)
5.Insulation Resistance	10000 MΩ min.		500 MΩ μF. or 10000 MΩ., whichever is the smaller. Note 4		Applied voltage: Rated voltage Duration: 60±5 sec. Charge/discharge current: 50mA max.
6.Capacitance (Tolerance)	0.5 to 5 pF: ±0.25 pF 1 to 10pF: ±0.5 pF 5 to 10 pF: ±1 pF 11 pF or over: ± 5% ±10% 105TYPER△, S△, T△, U△ only 0.5～2pF: ±0.1pF 2.2～20pF: ±5%	0.5 to 2 pF : ±0.1 pF 2.2 to 5.1 pF : ±5%	B: ±10%, ±20% F：$^{+80}_{-20}$ %	BJ：±10%, ±20% F：$^{+80}_{-20}$ %	Measuring frequency： Class1：1MHz±10%(C≦1000pF) 1 k Hz±10%(C>1000pF) Class2：1 k Hz±10%(C≦22μF) 120Hz±10Hz(C>22μF) Measuring voltage： Class1：0.5～5Vrms(C≦1000pF) 1±0.2Vrms(C>1000pF) Class2：1±0.2Vrms(C≦22μF) 0.5±0.1Vrms(C>22μF) Bias application: None
7.Q or Tangent of Loss Angle (tan δ)	Under 30 pF : Q≧400 + 20C 30 pF or over : Q≧1000 C= Nominal capacitance	Refer to detailed specification	B: 2.5% max.(50V, 25V) F: 5.0% max. (50V, 25V)	BJ: 2.5% max.(50V, 35V, 25V) 3.5% max. ※ 5.0% max. ※ 10.0% max. ※ F: 7.0% max. 5.0% max. ※ 9.0% max. ※ 11.0% max. ※ 16.0% max. ※ 20.0% max. ※ ※ See Table.1	Multilayer: Measuring frequency： Class1：1MHz±10%(C≦1000pF) 1 k Hz±10%(C>1000pF) Class2：1 k Hz±10%(C≦22μF) 120Hz±10Hz(C>22μF) Measuring voltage： Class1：0.5～5Vrms(C≦1000pF) 1±0.2Vrms(C>1000pF) Class2：1±0.2Vrms(C≦22μF) 0.5±0.1Vrms(C>22μF) Bias application: None High-Frequency-Multilayer: Measuring frequency: 1GHz Measuring equipment: HP4291A Measuring jig: HP16192A
8.Temperature Characteristic of Capacitance (Without voltage application)	CK：0±250 CJ：0±120 CH：0±60 CG：0±30 PK：−150±250 PJ：−150±120 PH：−150±60 RK：−220±250 RJ：−220±120 RH：−220±60 SK：−330±250 SJ：−330±120 SH：−330±60 TK：−470±250 TJ：−470±120 TH：−470±60 UK：−750±250 UJ：−750±120 SL：+350 to -1000 (ppm/℃)	CH：0±60 RH：−220±60 (ppm/℃)	B：±10%(−25～85℃) F：$^{+30}_{-80}$ %(−25～85℃) B(X7R)：±15% F(Y5V)：$^{+22}_{-82}$%	BJ：±10%(−25～85℃) F：$^{+30}_{-80}$ % (−25～85℃) BJ(X7R,X5R)：±15% F(Y5V)：$^{+22}_{-82}$ %	According to JIS C 5102 clause 7.12. Temperature compensating: Measurement of capacitance at 20℃ and 85℃ shall be made to calculate temperature characteristic by the following equation. $\frac{(C_{85} - C_{20})}{C_{20} \times \triangle T} \times 10^{6}$ (ppm/℃) High permitivity: Change of maximum capacitance deviation in step 1 to 5 Temperature at step 1: +20℃ Temperature at step 2: minimum operating temperature Temperature at step 3: +20℃ (Reference temperature) Temperature at step 4: maximum operating temperature Temperature at step 5: +20℃ Reference temperature for X7R, X5R and Y5V shall be +25℃
9.Resistance to Flexure of Substrate	Appearance: No abnormality Capacitance change: Within ±5% or ±0.5 pF, whichever is larger.	Appearance: No abnormality Capacitance change: Within±0.5 pF	Appearance: No abnormality Capacitance change: B, BJ: Within ±12.5% F: Within ±30%		Warp: 2mm Testing board: paper-phenol substrate Thickness: 1.6mm The measurement shall be made with board in the bent position.  (Unit: mm)

Multilayer Ceramic Capacitor Chips

Item	Specified Value				Test Methods and Remarks
	Temperature Compensating (Class 1)		High Permittivity (Class 2)		
	Standard	High Frequency Type	Standard Note1	High Value	
10.Body Strength	—	No mechanical damage.	—	—	High Frequency Multilayer: Applied force: 5N Duration: 10 sec. 
11.Adhesion of Electrode	No separation or indication of separation of electrode.				Applied force: 5N Duration: 30±5 sec. 
12.Solderability	At least 95% of terminal electrode is covered by new solder.				Solder temperature: 230±5℃ Duration: 4±1 sec.
13.Resistance to soldering	Appearance: No abnormality Capacitance change: Within ± 2.5% or ±0.25pF, whichever is larger. Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±2.5% Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±7.5% (B, BJ) Within ±20% (F) tan δ: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality		Preconditioning: Thermal treatment (at 150℃ for 1 hr) (Applicable to Class 2.) Solder temperature: 270±5℃ Duration: 3±0.5 sec. Preheating conditions: 80 to 100℃, 2 to 5 min. or 5 to 10 min. 150 to 200℃, 2 to 5 min. or 5 to 10 min. Recovery: Recovery for the following period under the standard condition after the test. 24±2 hrs (Class 1) 48±4 hrs (Class 2)
14.Thermal shock	Appearance: No abnormality Capacitance change: Within ± 2.5% or ±0.25pF, whichever is larger. Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±0.25pF Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±7.5% (B, BJ) Within ±20% (F) tan δ: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality		Preconditioning: Thermal treatment (at 150℃ for 1 hr) (Applicable to Class 2.) Conditions for 1 cycle: Step 1: Minimum operating temperature 30±3 min. Step 2: Room temperature 15 min. Step 3: Maximum operating temperature 30±3 min. Step 4: Room temperature 15 min. Number of cycles: 5 times Recovery after the test: 24±2 hrs (Class 1) 48±4 hrs (Class 2)
15.Damp Heat (steady state)	Appearance: No abnormality Capacitance change: Within ±5% or ±0.5pF, whichever is larger. Q: C≧30 pF : Q≧350 10≦C＜30 pF: Q≧275 + 2.5C C＜10 pF : Q≧200 + 10C C: Nominal capacitance Insulation resistance: 1000 MΩ min.	Appearance: No abnormality Capacitance change: Within ±0.5pF, Insulation resistance: 1000 MΩ min.	Appearance: No abnormality Capacitance change: B: Within ±12.5% F: Within ±30% tan δ: B: 5.0% max. F: 7.5% max. Insulation resistance: 50 MΩ μF or 1000 MΩ whichever is smaller.	Appearance: No abnormality Capacitance change: BJ: Within ±12.5% F: Within ±30% tan δ: BJ: 5.0% max. 7.5% max.※ 20.0% max.※ F: 11.0% max. 7.5% max.※ 16.0% max.※ 19.5% max.※ 25.0% max.※ ※See Table.2 Insulation resistance: 50 MΩ μF or 1000 MΩ whichever is smaller.	Multilayer： Preconditioning: Thermal treatment (at 150℃ for 1 hr) (Applicable to Class 2.) Temperature: 40±2℃ Humidity: 90 to 95% RH Duration: 500 $^{+24}_{-0}$ hrs Recovery: Recovery for the following period under the standard condition after the removal from test chamber. 24±2 hrs (Class 1) 48±4 hrs (Class 2) High-Frequency Multilayer: Temperature: 60±2℃ Humidity: 90 to 95% RH Duration: 500 $^{+24}_{-0}$ hrs Recovery: Recovery for the following period under the standard condition after the removal from test chamber. 24±2 hrs (Class 1)

Multilayer Ceramic Capacitor Chips

Item	Specified Value				Test Methods and Remarks
	Temperature Compensating (Class 1)		High Permittivity (Class 2)		
	Standard	High Frequency Type	Standard Note1	High Value	
16.Loading under Damp Heat	Appearance: No abnormality Capacitance change: Within ± 7.5% or ±0.75pF, whichever is larger. Q: C≧30 pF: Q≧200 C＜30 pF: Q≧100 + 10C/3 C： Nominal capacitance Insulation resistance: 500 MΩ min.	Appearance: No abnormality Capacitance change: C≦2 pF: Within ±0.4 pF C>2 pF: Within ±0.75 pF C： Nominal capacitance Insulation resistance: 500 MΩ min.	Appearance: No abnormality Capacitance change: B: Within ±12.5% F: Within ±30% tan δ: B: 5.0% max. F: 7.5% max. Insulation resistance: 25 MΩ μF or 500 MΩ, whichever is the smaller.	Appearance: No abnormality Capacitance change: BJ: Within ± 12.5% (50V, 35V, 25V) Within ± 15.0% (16V and under) F: Within ±30% tan δ: BJ: 5.0% max. 7.5% max.※ 20.0% max.※ F: 11.0% max. 7.5% max.※ 16.0% max.※ 19.5% max.※ 25.0% max.※ ※See Table.2 Insulation resistance: 25 MΩ μF or 500 MΩ, whichever is the smaller.	According to JIS C 5102 Clause 9. 9. Multilayer: Preconditioning: Voltage treatment (Class 2) Temperature: 40±2℃ Humidity: 90 to 95% RH Duration: 500 $^{+24}_{-0}$ hrs Applied voltage: Rated voltage Charge and discharge current: 50mA max. (Class 1,2) Recovery: Recovery for the following period under the standard condition after the removal from test chamber. 24±2 hrs (Class 1) 48±4 hrs (Class 2) High-Frequency Multilayer: Temperature: 60±2℃ Humidity: 90 to 95% RH Duration: 500 $^{+24}_{-0}$ hrs Applied voltage: Rated voltage Charge and discharge current: 50mA max. Recovery: 24±2 hrs of recovery under the standard condition after the removal from test chamber.
17.Loading at High Temperature	Appearance: No abnormality Capacitance change: Within ±3% or ±0.3pF, whichever is larger. Q: C≧30 pF : Q≧350 10≦C＜30 pF: Q≧275 + 2.5C C＜10 pF: Q≧200 + 10C C： Nominal capacitance Insulation resistance: 1000 MΩ min.	Appearance: No abnormality Capacitance change: Within ±3% or ±0.3pF, whichever is larger. Insulation resistance: 1000 MΩ min.	Appearance: No abnormality Capacitance change: B: Within ±12.5% F: Within ±30% tan δ: B: 4.0% max. F: 7.5% max. Insulation resistance: 50 MΩ μF or 1000 MΩ, whichever is smaller.	Appearance: No abnormality Capacitance change: BJ: Within ±12.5% F: Within ±30% tan δ: 5.0% max. 7.5% max.※ 20.0% max.※ F: 11.0% max. 7.5% max.※ 16.0% max.※ 19.5% max.※ 25.0% max.※ ※See Table.2 Insulation resistance: 50 MΩ μF or 1000 MΩ, whichever is smaller.	According to JIS C 5102 clause 9.10. Multilayer: Preconditioning: Voltage treatment (Class 2) Temperature:125±3℃(Class 1, Class 2: B, BJ(X7R)) 85±2℃ (Class 2: BJ,F) Duration: 1000 $^{+48}_{-0}$ hrs Applied voltage: Rated voltage×2 Recovery: Recovery for the following period under the standard condition after the removal from test chamber. As for Ni product, thermal treatment shall be performed prior to the recovery. 24±2 hrs (Class 1) 48±4 hrs (Class 2) High-Frequency Multilayer: Temperature: 125±3℃ (Class 1) Duration: 1000 $^{+48}_{-0}$ hrs Applied voltage: Rated voltage×2 Recovery: 24±2 hrs of recovery under the standard condition after the removal from test chamber.

Note 1: For 105 type, specified in "High value".
Note 2: Thermal treatment (Multilayer): 1 hr of thermal treatment at 150 +0 /−10 ℃ followed by 48±4 hrs of recovery under the standard condition shall be performed before the measurement.
Note 3: Voltage treatment (Multilayer): 1 hr of voltage treatment under the specified temperature and voltage for testing followed by 48±4 hrs of recovery under the standard condition shall be performed before the measurement.
Note on standard condition: "standard condition" referred to herein is defined as follows: 5 to 35℃ of temperature, 45 to 85% relative humidity, and 86 to 106kPa of air pressure.
When there are questions concerning measurement results: In order to provide correlation data, the test shall be conducted under condition of 20±2℃ of temperature, 65 to 70% relative humidity, and 86 to 106kPa of air pressure. Unless otherwise specified, all the tests are conducted under the "standard condition."
Note 4: Specified value for Instration Resistance of JMK212BJ475M only: 100MΩ μF or more.

Table. 1 tanδ(D. F.)

Item	tanδ
BJ: LMK type; 063 type 105 type (C≦0.047μF) 107 type (C≦0.47μF) 212 type (C≦1μF) 316 / 325 / 432 type EMK type; 105 / 107/ 212 / 316 / 325 type TMK type; 316 type(C > 0.47μF) 325 / 432 type GMK type;212 type (C≧0.22μF) 316 type (C≧0.68μF) 325 type UMK type;212 type (C > 0.1μF) 316 type (C≧0.47μF) 325 type (C≦1μF)	3.5%max.
BJ: JMK type LMK type; 105 type (C≧0.056μF) 107 type (C > 0.47μF) 212 type (C > 1μF) J4K, E4K type F: 105 type (50V, 25V)	5.0% max.
F: LMK type; 212 type 316 type (C=10μF)：汎用 (C=4.7μF)：低背 325 type (C > 10μF) EMK type; 105 type (C≧0.068μF) UMK type; 325 type (C≧4.7μF)	9.0% max.
BJ: AMK type	10.0% max.
F: LMK type; 105 type (C =0.22μF)	11.0% max.
F: JMK type; 105 / 107 / 212 / 316 / 325 / 432 type LMK type; 107 type,325 type 432 type,316 type (C > 10μF) E4K type	16.0% max.
F: AMK type	20.0% max.

Table. 2 tanδ(D. F.)

Item	tanδ
BJ: JMK type LMK type; 063 type 105 type (C≧0.056μF) 107 type (C≧0.47μF) 212 type (C > 1μF) J4K, E4K type F: 105 type(50V, 25V)	7.5% max.
F: LMK type; 105 type (C=0.22μF)	16.0% max.
F: JMK type; 105 / 107 / 212 / 316 / 325 / 432 type LMK type; 107 type 432 type E4K type	19.5% max.
BJ: AMK type	20.0% max.
F: AMK type	25.0% max.

梱包　PACKAGING

①標準数量 Standard quantity

■袋づめ梱包 Bulk packaging

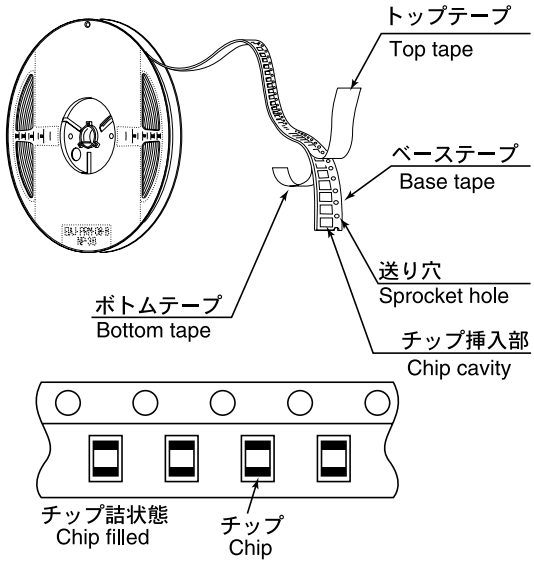
形式(EIA) Type	製品厚み Thickness		標準数量 Standard quantity [pcs]
	mm(inch)	code	
□MK105(0402)	0.5 (0.020)	V	1000
E VK105(0402)		W	
□MK107(0603)	0.8 (0.031)	A	
		Z	
□MK212(0805)	0.85 (0.033)	D	
	1.25 (0.049)	G	
□4K212(0805)	0.85 (0.033)	D	
□MK316(1206)	0.85 (0.033)	D	
	1.15 (0.045)	F	
	1.25 (0.049)	G	
	1.6 (0.063)	L	
□4K316(1206)	1.15 (0.045)	F	
□MK325(1210)	0.85 (0.033)	D	
	1.15 (0.045)	F	
	1.5 (0.059)	H	
	1.9 (0.075)	N	
	2.5 (0.098)	M	

■テーピング梱包　Taped packaging

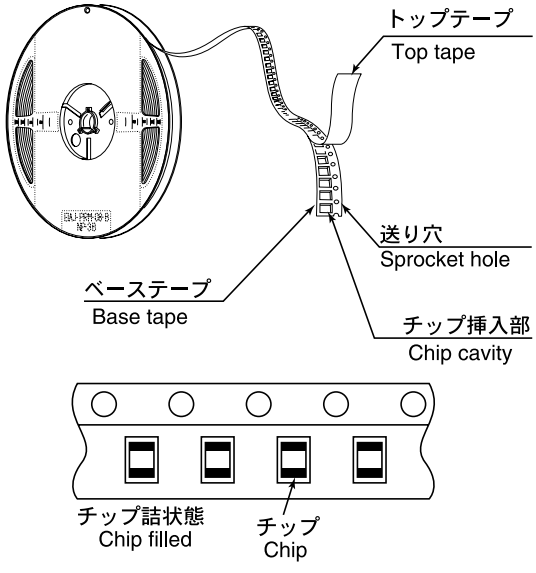
形式(EIA) Type	製品厚み Thickness		標準数量 Standard quantity [pcs]	
	mm(inch)	code	紙テープ paper	エンボステープ Embossed tape
□MK063(0201)	0.3 (0.012)	P	15000	—
□MK105(0402)	0.5 (0.020)	V	10000	—
E VK105(0402)		W		
□MK107(0603)	0.8 (0.031)	A	4000	—
		Z		
□MK212(0805)	0.85 (0.033)	D	4000	—
	1.25 (0.049)	G	—	3000
□4K212(0805)	0.85 (0.033)	D	4000	—
□MK316(1206)	0.85 (0.033)	D	4000	—
	1.15 (0.045)	F	—	3000
	1.25 (0.049)	G		
	1.6 (0.063)	L	—	2000
□4K316(1206)	1.15 (0.045)	F		
□MK325(1210)	0.85 (0.033)	D	—	2000
	1.15 (0.045)	F		
	1.5 (0.059)	H		
	1.9 (0.075)	N		
	2.5 (0.098)	M	—	500
□MK432(1812)	2.5 (0.098)	M	—	500
□MK550(2220)	2.5 (0.098)	M	—	500

②テーピング材質　Taping material

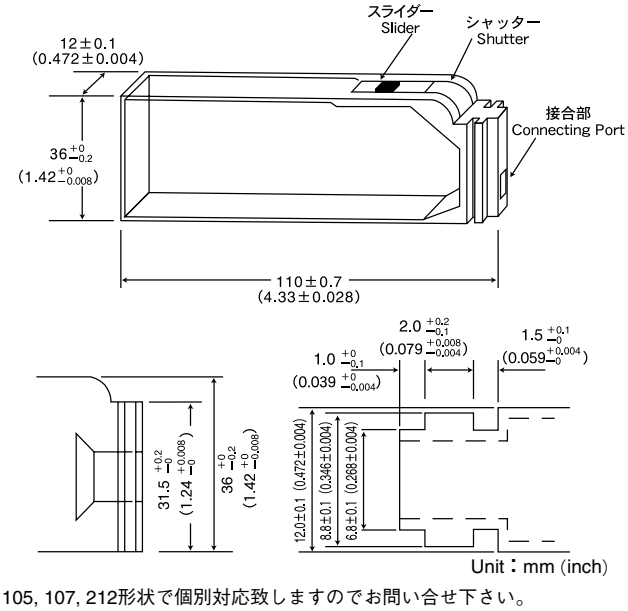
紙テープ
Card board carrier tape



エンボステープ
Embossed Tape



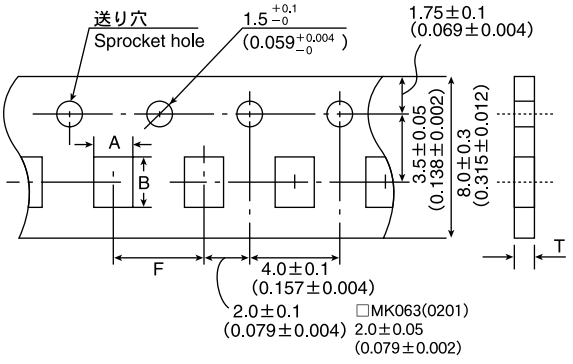
③バルクカセット　Bulk Cassette



105, 107, 212形状で個別対応致しますのでお問い合せ下さい。
Please contact any of our offices for accepting your requirement according to dimensions 0402, 0603, 0805.(inch)

③テーピング寸法　Taping dimensions

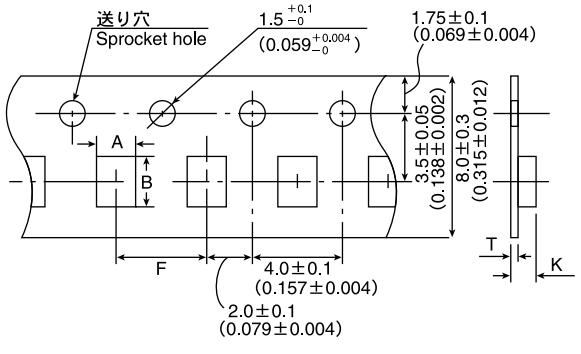
紙テープ　Paper Tape（8mm幅）(0.315inches wide)



Type (EIA)	チップ挿入部 Chip Cavity		挿入ピッチ Insertion Pitch	テープ厚み Tape Thickness
	A	B	F	T
□MK063(0201)	0.37±0.06 (0.06±0.002)	0.67±0.06 (0.027±0.002)	2.0±0.05 (0.079±0.002)	0.42±0.02 (0.017±0.001)
□MK105(0402) E VK105(0402)	0.65±0.1 (0.026±0.004)	1.15±0.1 (0.045±0.004)	2.0±0.05 (0.079±0.002)	0.8max. (0.031max.)
□MK107(0603)	1.0±0.2 (0.039±0.008)	1.8±0.2 (0.071±0.008)		
□MK212(0805)	1.65±0.2 (0.065±0.008)	2.4±0.2 (0.094±0.008)	4.0±0.1 (0.157±0.004)	1.1max. (0.043max.)
□4K212(0805)				
□MK316(1206)	2.0±0.2 (0.079±0.008)	3.6±0.2 (0.142±0.008)		

Unit：mm(inch)

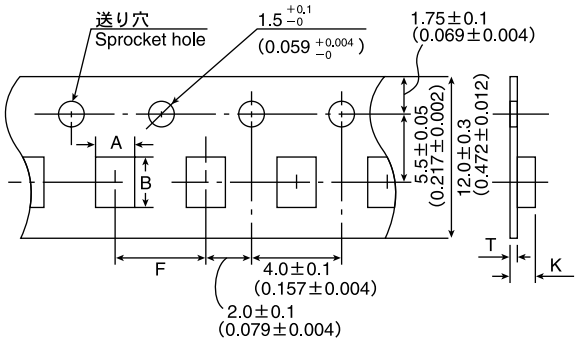
エンボステープ　Embossed tape（8mm幅）(0.315inches wide)



Type (EIA)	チップ挿入部 Chip cavity		挿入ピッチ Insertion Pitch	テープ厚み Tape Thickness	
	A	B	F	K	T
□MK212(0805)	1.65±0.2 (0.065±0.008)	2.4±0.2 (0.094±0.008)	4.0±0.1 (0.157±0.004)	2.5max. (0.098max.)	0.6max (0.024max.)
□MK316(1206)	2.0±0.2 (0.079±0.008)	3.6±0.2 (0.142±0.008)			
□4K316(1206)					
□MK325(1210)	2.8±0.2 (0.110±0.008)	3.6±0.2 (0.142±0.008)		3.4max. (0.134max.)	

Unit：mm(inch)

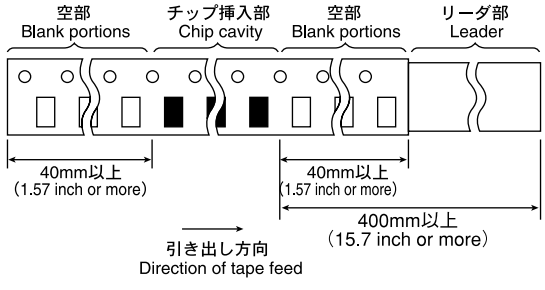
エンボステープ　Embossed tape（12mm幅）(0.472inches wide)



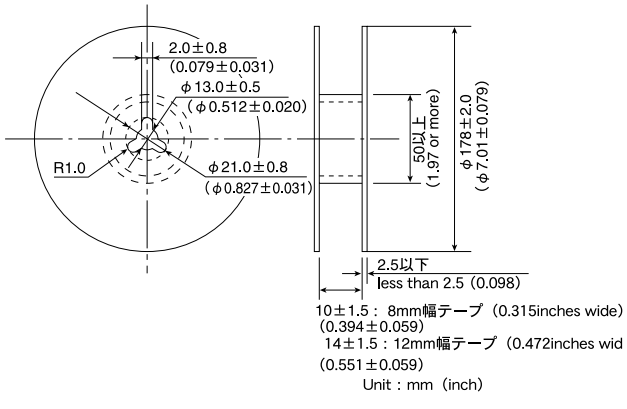
Type (EIA)	チップ挿入部 Chip cavity		挿入ピッチ Insertion Pitch	テープ厚み Tape Thickness	
	A	B	F	K	T
□MK432(1812)	3.7±0.2 (0.146±0.008)	4.9±0.2 (0.193±0.008)	8.0±0.1 (0.315±0.004)	3.4max. (0.134max.)	0.6max. (0.024max.)
□MK550(2220)	5.4±0.2 (0.213±0.008)	6.1±0.2 (0.240±0.008)	8.0±0.1 (0.315±0.004)	3.5max. (0.138max.)	0.6max. (0.024max.)

Unit：mm(inch)

④リーダ部／空部　Leader and Blank portion

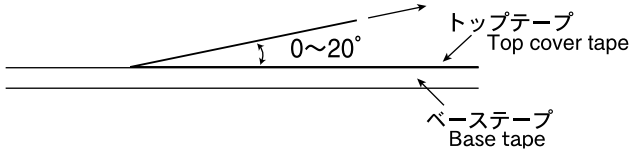


⑤リール寸法　Reel size

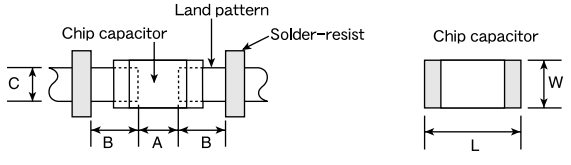
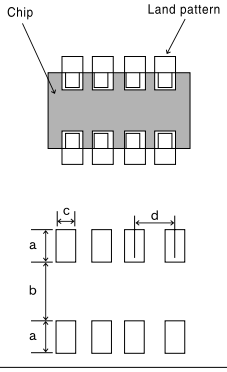


⑥トップテープ強度　Top Tape Strength

トップテープのはがし力は下図矢印方向にて0.1～0.7Nとなります。
The top tape requires a peel-off force of 0.1～0.7N in the direction of the arrow as illustrated below.

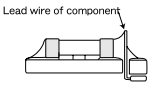
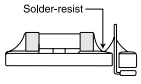
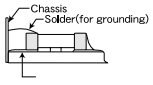
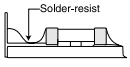
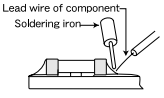
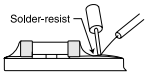
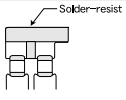


Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
1.Circuit Design	Verification of operating environment, electrical rating and performance 1. A malfunction in medical equipment, spacecraft, nuclear reactors, etc. may cause serious harm to human life or have severe social ramifications. As such, any capacitors to be used in such equipment may require higher safety and/or reliability considerations and should be clearly differentiated from components used in general purpose applications. Operating Voltage (Verification of Rated voltage) 1. The operating voltage for capacitors must always be lower than their rated values. If an AC voltage is loaded on a DC voltage, the sum of the two peak voltages should be lower than the rated value of the capacitor chosen. For a circuit where both an AC and a pulse voltage may be present, the sum of their peak voltages should also be lower than the capacitor's rated voltage. 2. Even if the applied voltage is lower than the rated value, the reliability of capacitors might be reduced if either a high frequency AC voltage or a pulse voltage having rapid rise time is present in the circuit.	
2.PCB Design	Pattern configurations (Design of Land-patterns) 1. When capacitors are mounted on a PCB, the amount of solder used (size of fillet) can directly affect capacitor performance. Therefore, the following items must be carefully considered in the design of solder land patterns: (1) The amount of solder applied can affect the ability of chips to withstand mechanical stresses which may lead to breaking or cracking. Therefore, when designing land-patterns it is necessary to consider the appropriate size and configuration of the solder pads which in turn determines the amount of solder necessary to form the fillets. (2) When more than one part is jointly soldered onto the same land or pad, the pad must be designed so that each component's soldering point is separated by solder-resist.	1.The following diagrams and tables show some examples of recommended patterns to prevent excessive solder amourts.(larger fillets which extend above the component end terminations) Examples of improper pattern designs are also shown. (1) Recommended land dimensions for a typical chip capacitor land patterns for PCBs  Recommended land dimensions for wave-soldering (unit: mm) <table><tr><td colspan="2">Type</td><td>107</td><td>212</td><td>316</td><td>325</td></tr><tr><td rowspan="2">Size</td><td>L</td><td>1.6</td><td>2.0</td><td>3.2</td><td>3.2</td></tr><tr><td>W</td><td>0.8</td><td>1.25</td><td>1.6</td><td>2.5</td></tr><tr><td colspan="2">A</td><td>0.8~1.0</td><td>1.0~1.4</td><td>1.8~2.5</td><td>1.8~2.5</td></tr><tr><td colspan="2">B</td><td>0.5~0.8</td><td>0.8~1.5</td><td>0.8~1.7</td><td>0.8~1.7</td></tr><tr><td colspan="2">C</td><td>0.6~0.8</td><td>0.9~1.2</td><td>1.2~1.6</td><td>1.8~2.5</td></tr></table> Recommended land dimensions for reflow-soldering (unit: mm) <table><tr><td colspan="2">Type</td><td>063</td><td>105</td><td>107</td><td>212</td><td>316</td><td>325</td><td>432</td><td>550</td></tr><tr><td rowspan="2">Size</td><td>L</td><td>0.6</td><td>1.0</td><td>1.6</td><td>2.0</td><td>3.2</td><td>3.2</td><td>4.5</td><td>5.7</td></tr><tr><td>W</td><td>0.3</td><td>0.5</td><td>0.8</td><td>1.25</td><td>1.6</td><td>2.5</td><td>3.2</td><td>5.0</td></tr><tr><td colspan="2">A</td><td>0.20~0.30</td><td>0.45~0.55</td><td>0.6~0.8</td><td>0.8~1.2</td><td>1.8~2.5</td><td>1.8~2.5</td><td>2.5~3.5</td><td>3.7~4.7</td></tr><tr><td colspan="2">B</td><td>0.20~0.30</td><td>0.40~0.50</td><td>0.6~0.8</td><td>0.8~1.2</td><td>1.0~1.5</td><td>1.0~1.5</td><td>1.5~1.8</td><td>1.5~2.3</td></tr><tr><td colspan="2">C</td><td>0.25~0.40</td><td>0.45~0.55</td><td>0.6~0.8</td><td>0.9~1.6</td><td>1.2~2.0</td><td>1.8~3.2</td><td>2.3~3.5</td><td>3.5~5.5</td></tr></table> Excess solder can affect the ability of chips to withstand mechanical stresses. Therefore, please take proper precautions when designing land-patterns.  <table><tr><td colspan="2">Type</td><td>316 (4 circuits)</td><td>212 (4 circuits)</td></tr><tr><td rowspan="2">Size</td><td>L</td><td>3.2</td><td>2.0</td></tr><tr><td>W</td><td>1.6</td><td>1.25</td></tr><tr><td colspan="2">a</td><td>0.7~0.9</td><td>0.5~0.6</td></tr><tr><td colspan="2">b</td><td>1</td><td>0.5~0.6</td></tr><tr><td colspan="2">c</td><td>0.4~0.5</td><td>0.2~0.3</td></tr><tr><td colspan="2">d</td><td>0.8</td><td>0.5</td></tr></table>

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
2.PCB Design		(2) Examples of good and bad solder application

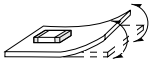
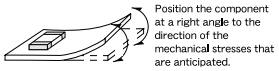
Items	Not recommended	Recommended
Mixed mounting of SMD and leaded components		
Component placement close to the chassis		
Hand-soldering of leaded components near mounted components		
Horizontal component placement		

Pattern configurations

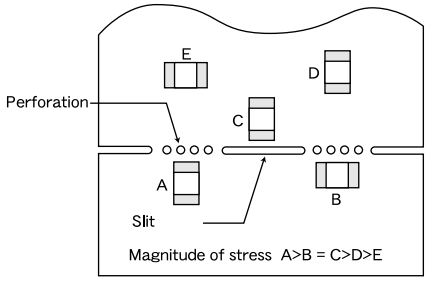
(Capacitor layout on panelized [breakaway] PC boards)

1. After capacitors have been mounted on the boards, chips can be subjected to mechanical stresses in subsequent manufacturing processes (PCB cutting, board inspection, mounting of additional parts, assembly into the chassis, wave soldering the reflow soldered boards etc.) For this reason, planning pattern configurations and the position of SMD capacitors should be carefully performed to minimize stress.

1-1. The following are examples of good and bad capacitor layout; SMD capacitors should be located to minimize any possible mechanical stresses from board warp or deflection.

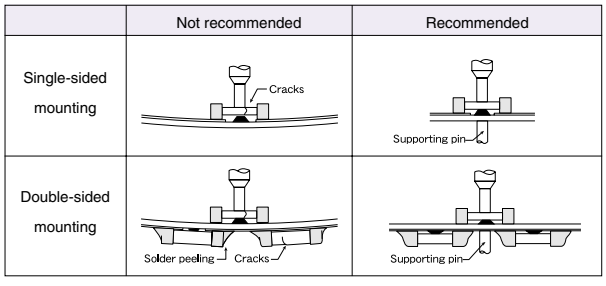
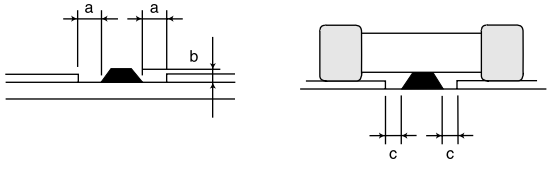
	Not recommended	Recommended
Deflection of the board		

1-2. To layout the capacitors for the breakaway PC board, it should be noted that the amount of mechanical stresses given will vary depending on capacitor layout. The example below shows recommendations for better design.

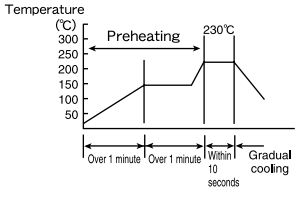
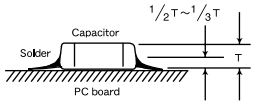
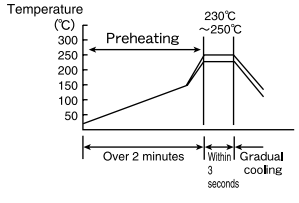


1-3. When breaking PC boards along their perforations, the amount of mechanical stress on the capacitors can vary according to the method used. The following methods are listed in order from least stressful to most stressful: push-back, slit, V-grooving, and perforation. Thus, any ideal SMD capacitor layout must also consider the PCB splitting procedure.

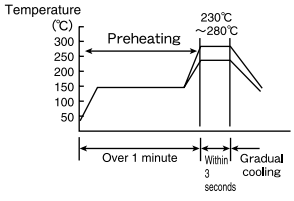
Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
3.Considerations for automatic placement	Adjustment of mounting machine 1. Excessive impact load should not be imposed on the capacitors when mounting onto the PC boards. 2. The maintenance and inspection of the mounters should be conducted periodically.	1. If the lower limit of the pick-up nozzle is low, too much force may be imposed on the capacitors, causing damage. To avoid this, the following points should be considered before lowering the pick-up nozzle: (1)The lower limit of the pick-up nozzle should be adjusted to the surface level of the PC board after correcting for deflection of the board. (2)The pick-up pressure should be adjusted between 1 and 3 N static loads. (3)To reduce the amount of deflection of the board caused by impact of the pick-up nozzle, supporting pins or back-up pins should be used under the PC board. The following diagrams show some typical examples of good pick-up nozzle placement:  2. As the alignment pin wears out, adjustment of the nozzle height can cause chipping or cracking of the capacitors because of mechanical impact on the capacitors. To avoid this, the monitoring of the width between the alignment pin in the stopped position, and maintenance, inspection and replacement of the pin should be conducted periodically.
	Selection of Adhesives 1. Mounting capacitors with adhesives in preliminary assembly, before the soldering stage, may lead to degraded capacitor characteristics unless the following factors are appropriately checked; the size of land patterns, type of adhesive, amount applied, hardening temperature and hardening period. Therefore, it is imperative to consult the manufacturer of the adhesives on proper usage and amounts of adhesive to use.	1. Some adhesives may cause reduced insulation resistance. The difference between the shrinkage percentage of the adhesive and that of the capacitors may result in stresses on the capacitors and lead to cracking. Moreover, too little or too much adhesive applied to the board may adversely affect component placement, so the following precautions should be noted in the application of adhesives. (1)Required adhesive characteristics a. The adhesive should be strong enough to hold parts on the board during the mounting & solder process. b. The adhesive should have sufficient strength at high temperatures. c. The adhesive should have good coating and thickness consistency. d. The adhesive should be used during its prescribed shelf life. e. The adhesive should harden rapidly f. The adhesive must not be contaminated. g. The adhesive should have excellent insulation characteristics. h. The adhesive should not be toxic and have no emission of toxic gasses. (2)The recommended amount of adhesives is as follows; Figure / 212/316 case sizes as examples a / 0.3mm min b / 100～120 μm c / Adhesives should not contact the pad Amount of adhesive After capacitors are bonded 

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
4. Soldering	Selection of Flux 1. Since flux may have a significant effect on the performance of capacitors, it is necessary to verify the following conditions prior to use; (1)Flux used should be with less than or equal to 0.1 wt% (equivelent to chroline) of halogenated content. Flux having a strong acidity content should not be applied. (2)When soldering capacitors on the board, the amount of flux applied should be controlled at the optimum level. (3)When using water-soluble flux, special care should be taken to properly clean the boards.	1-1. When too much halogenated substance (Chlorine, etc.) content is used to activate the flux, or highly acidic flux is used, an excessive amount of residue after soldering may lead to corrosion of the terminal electrodes or degradation of insulation resistance on the surface of the capacitors. 1-2. Flux is used to increase solderability in flow soldering, but if too much is applied, a large amount of flux gas may be emitted and may detrimentally affect solderability. To minimize the amount of flux applied, it is recommended to use a flux-bubbling system. 1-3. Since the residue of water-soluble flux is easily dissolved by water content in the air, the residue on the surface of capacitors in high humidity conditions may cause a degradation of insulation resistance and therefore affect the reliability of the components. The cleaning methods and the capability of the machines used should also be considered carefully when selecting water-soluble flux.
	Soldering Temperature, time, amount of solder, etc. are specified in accordance with the following recommended conditions.	1-1. Preheating when soldering Heating: Ceramic chip components should be preheated to within 100 to 130℃ of the soldering. Cooling: The temperature difference between the components and cleaning process should not be greater than 100℃. Ceramic chip capacitors are susceptible to thermal shock when exposed to rapid or concentrated heating or rapid cooling. Therefore, the soldering process must be conducted with great care so as to prevent malfunction of the components due to excessive thermal shock. Recommended conditions for soldering [Reflow soldering] Temperature profile  Caution 1. The ideal condition is to have solder mass (fillet) controlled to 1/2 to 1/3 of the thickness of the capacitor, as shown below:  2. Because excessive dwell times can detrimentally affect solderability, soldering duration should be kept as close to recommended times as possible. [Wave soldering] Temperature profile  Caution 1. Make sure the capacitors are preheated sufficiently. 2. The temperature difference between the capacitor and melted solder should not be greater than 100 to130℃ 3. Cooling after soldering should be as gradual as possible. 4. Wave soldering must not be applied to the capacitors designated as for reflow soldering only.

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
4. Soldering		[Hand soldering] Temperature profile  Caution 1. Use a 20W soldering iron with a maximum tip diameter of 1.0 mm. 2. The soldering iron should not directly touch the capacitor.
5.Cleaning	Cleaning conditions 1. When cleaning the PC board after the capacitors are all mounted, select the appropriate cleaning solution according to the type of flux used and purpose of the cleaning (e.g. to remove soldering flux or other materials from the production process.) 2. Cleaning conditions should be determined after verifying, through a test run, that the cleaning process does not affect the capacitor's characteristics.	1. The use of inappropriate solutions can cause foreign substances such as flux residue to adhere to the capacitor or deteriorate the capacitor's outer coating, resulting in a degradation of the capacitor's electrical properties (especially insulation resistance). 2. Inappropriate cleaning conditions (insufficient or excessive cleaning) may detrimentally affect the performance of the capacitors. (1)Excessive cleaning In the case of ultrasonic cleaning, too much power output can cause excessive vibration of the PC board which may lead to the cracking of the capacitor or the soldered portion, or decrease the terminal electrodes' strength. Thus the following conditions should be carefully checked; Ultrasonic output Below 20 W/ℓ Ultrasonic frequency Below 40 kHz Ultrasonic washing period 5 min. or less
6.Post cleaning processes	1. With some type of resins a decomposition gas or chemical reaction vapor may remain inside the resin during the hardening period or while left under normal storage conditions resulting in the deterioration of the capacitor's performance. 2. When a resin's hardening temperature is higher than the capacitor's operating temperature, the stresses generated by the excess heat may lead to capacitor damage or destruction. The use of such resins, molding materials etc. is not recommended.	
7.Handling	Breakaway PC boards (splitting along perforations) 1. When splitting the PC board after mounting capacitors and other components, care is required so as not to give any stresses of deflection or twisting to the board. 2. Board separation should not be done manually, but by using the appropriate devices. Mechanical considerations 1. Be careful not to subject the capacitors to excessive mechanical shocks. (1)If ceramic capacitors are dropped onto the floor or a hard surface, they should not be used. (2)When handling the mounted boards, be careful that the mounted components do not come in contact with or bump against other boards or components.	

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
8.Storage conditions	Storage 1. To maintain the solderability of terminal electrodes and to keep the packaging material in good condition, care must be taken to control temperature and humidity in the storage area. Humidity should especially be kept as low as possible. ・Recommended conditions Ambient temperature Below 40℃ Humidity Below 70% RH The ambient temperature must be kept below 30℃. Even under ideal storage conditions capacitor electrode solderability decreases as time passes, so ceramic chip capacitors should be used within 6 months from the time of delivery. ・The packaging material should be kept where no chlorine or sulfur exists in the air. 2. The capacitance value of high dielectric constant capacitors (type 2 &3) will gradually decrease with the passage of time, so this should be taken into consideration in the circuit design. If such a capacitance reduction occurs, a heat treatment of 150℃ for 1hour will return the capacitance to its initial level.	1. If the parts are stored in a high temperature and humidity environment, problems such as reduced solderability caused by oxidation of terminal electrodes and deterioration of taping/packaging materials may take place. For this reason, components should be used within 6 months from the time of delivery. If exceeding the above period, please check solderability before using the capacitors.