600mA, 2MHz, High-Efficiency Synchronous Buck PWM Converter

General Description

The RT8003 is a high-efficiency synchronous buck PWM converter with integrated P-Channel and N-Channel power MOSFET switches. Capable of delivering 600mA output current over a wide input voltage range of 2.4V to 5.5V, the RT8003 is ideally suited for portable applications powered by a single Li-Ion battery or by 3-cell NiMH/NiCd batteries. The device operates at 2MHz PWM switching fixed frequency, can use smaller C_{IN}, C_{OUT} capacitor and inductor.

The RT8003 integrates two low $R_{DS(ON)}$ 230mΩ and 180mΩ of high- and low-side switching MOSFETs to reduce board space, as only resistors and capacitors along with one inductor are required externally for operation. The RT8003 has adjustable output range down to 0.5V. The other features include internal soft-start, chip enable, over-temperature and over-current protections. It is available in a space-saving VDFN-10L 3x3 package.

Ordering Information

RT8003 ☐ ☐

Package Type
QV : VDFN-10L 3x3 (V-Type)

Operating Temperature Range
P : Pb Free with Commercial Standard

Note :

RichTek Pb-free products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area, otherwise visit our website for detail.

Features

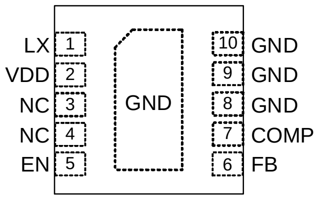
- **2.4V to 5.5V Input Voltage Range**
- **Adjustable Output from 0.5V to V_{IN}**
- **Guaranteed 600mA Output Current**
- **Accurate Reference : 0.5V (±1.5%)**
- **Up to 90% Conversion Efficiency**
- **Typical Quiescent Current : 200μA**
- **Integrated Low $R_{DS(ON)}$ High- and Low-Side Power MOSFET Switches: 230mΩ and 180mΩ**
- **Current Mode PWM Operation**
- **Fixed Frequency : 2MHz**
- **100% Maximum Duty Cycle for Lowest Dropout**
- **Internal Soft-Start**
- **No Schottky Diode Required**
- **Over-Temperature and Over-Current Protection**
- **Small 10-Lead VDFN 3x3 Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Battery-Powered Equipments
- Low Power CPU and DSP Supplies
- Digital Cameras and Hard Disks
- Protable Instruments and Notebook Computers
- Celluar Phones, PDAs, and Handheld PCs
- USB-Based DSL Modems and Other Network Interface Cards

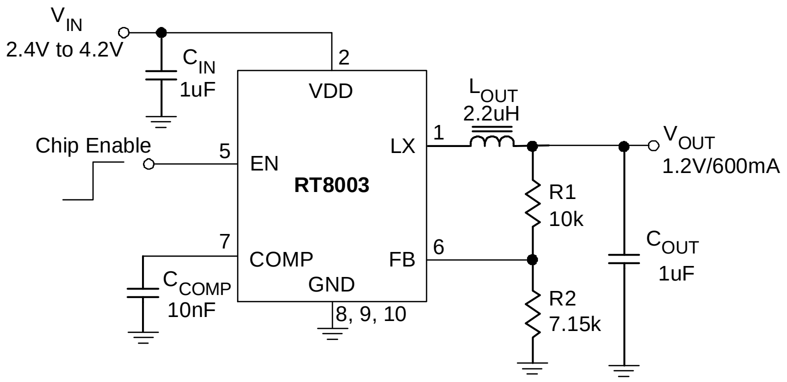
Pin Configurations

(TOP VIEW)



VDFN-10L 3x3

Typical Application Circuit



Recommended component selection for Typical Application Circuit.

V_{OUT} (V)	V_{IN} (V)	C_{IN} (uF)	C_{OUT} (uF)	L_{OUT} (uH)	R1 (kW)	R2 (kW)	C_{COMP} (nF)
0.5	2.4 to 3.3	1	1/2.2	2.2/1	10	Open	10
1	2.4 to 3.6	1	1/2.2	2.2/1	10	10	10
1.2	2.4 to 4.2	1	1/2.2	2.2/1	10	7.15	10
1.8	2.4 to 5.5	1	1/2.2	2.2/1	10	3.83	10
2.5	3.3 to 5.5	1	1/2.2	2.2/1	10	2.49	10
3.3	4.2 to 5.5	1	1/2.2	2.2/1	10	1.78	10

Suggested Inductors

Component Supplier	Series	Inductance (μH)	ESR (mW)	Current Rating (mA)	Dimensions (mm)
ABC	SR0302	1 2.2	60 90	2100 1650	3x2.8x2.5
Sumida	CDRH2D14	2.2	94	1000	3.2x3.2x1.55
TDK	VLP4612	1 2.5	110 170	1500 1100	4.6x3.4x1.2

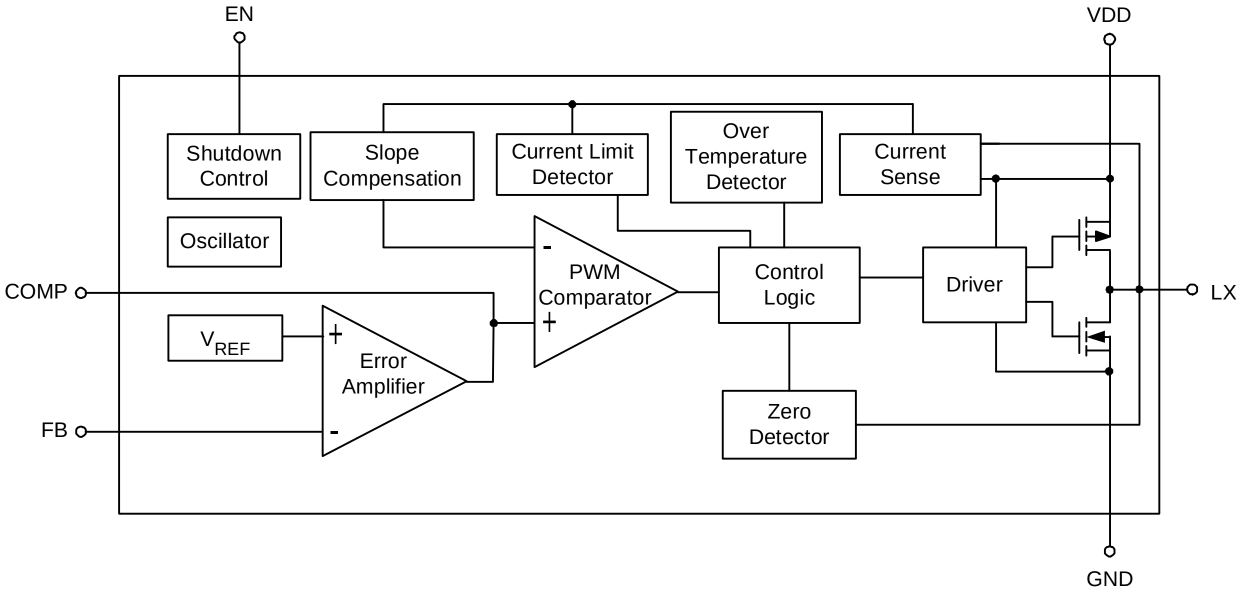
Suggested Capacitors For C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (uF)	Case Size
TDK	C1608X5R1A105M	1	0603
	C1608X5R1A225M	2.2	0603
Panasonic	ECJ1VB0J105M	1	0603
	ECJ1VB0J225M	2.2	0603
TAIYO YUDEN	JMK107BJ105M	1	0603
	JMK107BJ225M	2.2	0603

Functional Pin Description

No	Pin Name	Pin Function
1	LX	Internal Power MOSFET Switches Output. Connect this pin to the inductor.
2	VDD	Power Input Supply. Input voltage which supplies current to the output pin. Connect this pin with a low-ESR capacitor to GND
3,4	NC	No Internal Connection
5	EN	Chip Enable (Active High). Logic low shuts down the converter. Floating this pin is forbidden.
6	FB	Switcher Feedback Voltage. This pin is the inverting input of the error amplifier. FB senses the switcher output through an external resistor divider network. FB regulation voltage is 0.5V.
7	COMP	Compensation Input. This pin is the output of the internal error amplifier. Connect an external capacitor to compensate the regulator controlled loop.
8,9,10	GND	Ties the pin directly to the cathode terminal of C_{IN} and C_{OUT} and ground plane with the lowest impedance. Signal and Common Ground (Exposed thermal pad is connected to GND). The GND pad area should be as large as possible and using many vias to conduct the heat into the buried GND plate of PCB layer. All small-signal, compensation and feedback components should connect to this pin.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage -- –0.3V to 6V
- LX Voltage -- –0.3V to (V_{DD} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  VDFN-10L 3x3 -- 1.923W
- Package Thermal Resistance (Note 4)
  VDFN-10L 3x3, θ_{JA} -- 52°C/W
- Junction Temperature -- 150°C
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Storage Temperature Range -- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) -- 2kV
  MM (Machine Mode) -- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage -- 2.4V to 5.5V
- Enable Input Voltage, V_{EN} -- 0V to 5.5V
- Ambient Temperature Range -- –40°C to 85°C
- Junction Temperature Range -- 0°C to 125°C

Electrical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
Quiescent Current	I_Q	V_{EN} = 3.3V, V_{FB} = V_{REF} + 0.15V, I_{OUT} = 0mA	--	200	400	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	0.01	1	μA
Reference						
Reference Voltage	V_{REF}		0.4925	0.5	0.5075	V
Oscillator						
Switching Frequency Range	f_{OSC}		1.7	2.0	2.3	MHz
Maximum Duty Cycle	DC	V_{DD} = V_{OUT}	100	--	--	%
Output Voltage						
Line Regulation		V_{DD} = 2.4V to 5.5V, I_{LOAD} = 100mA	--	--	+1.5	%
Load Regulation		10mA < I_{LOAD} < 600mA	--	--	+1.5	%
Power Switches						
$R_{DS(ON)}$ of P-Channel MOSFET	R_{P_FET}	V_{DD} = 3.3V, I_{LX} = 300mA	--	230	--	mΩ
$R_{DS(ON)}$ of N-Channel MOSFET	R_{N_FET}	V_{DD} = 3.3V, I_{LX} = –300mA	--	180	--	mΩ
Current Limit	I_{LIMIT}	V_{DD} = 3.3V, V_{FB} = V_{REF} - 0.15V	--	1.8	--	A

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Logic Input							
EN Threshold	Logic-Low Voltage	V_{IL}	V_{DD} = 2.4V to 5.5V, Shutdown	--	--	0.4	V
	Logic-High Voltage	V_{IH}	V_{DD} = 2.4V to 5.5V, Enable	1.5	--	--	
Protection							
Thermal Shutdown Temperature		T_{SD}		--	180	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C

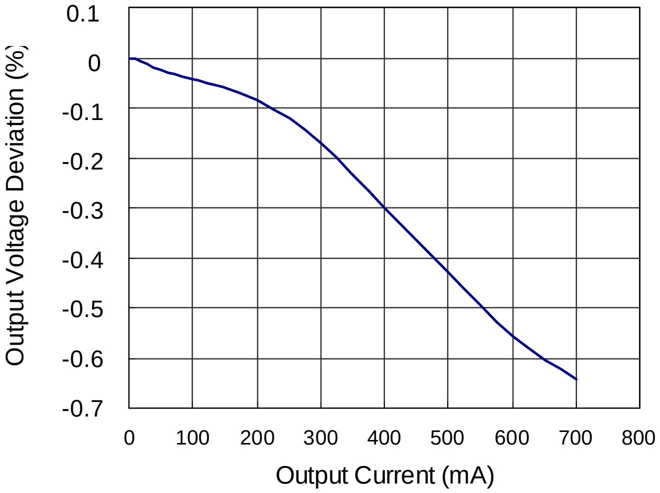
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

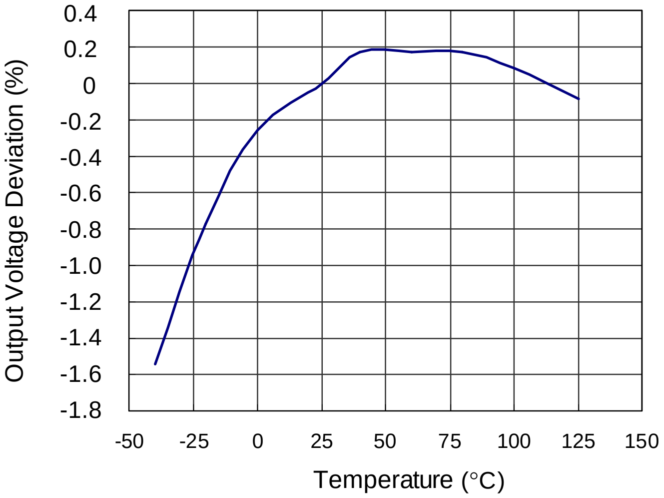
Note 2. Devices are ESD sensitive. Handling precaution recommended.

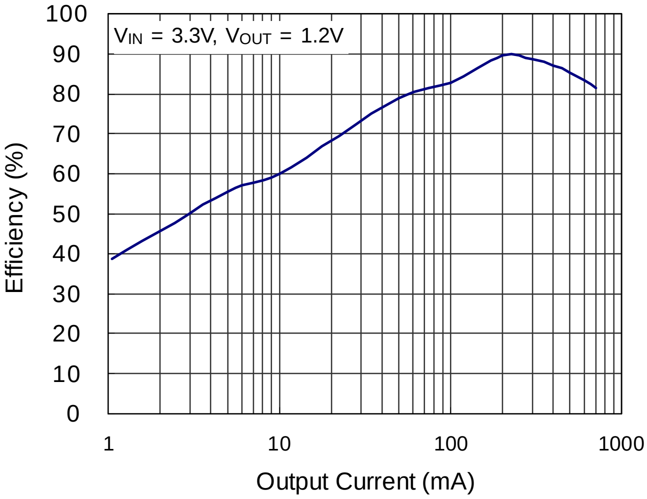
Note 3. The device is not guaranteed to function outside its operating conditions.

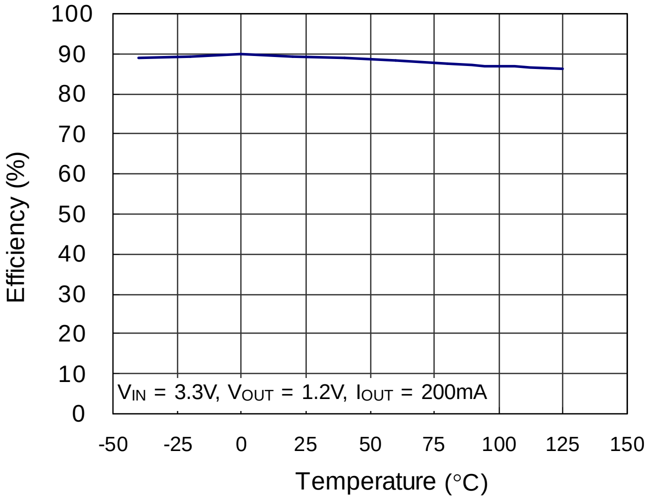
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

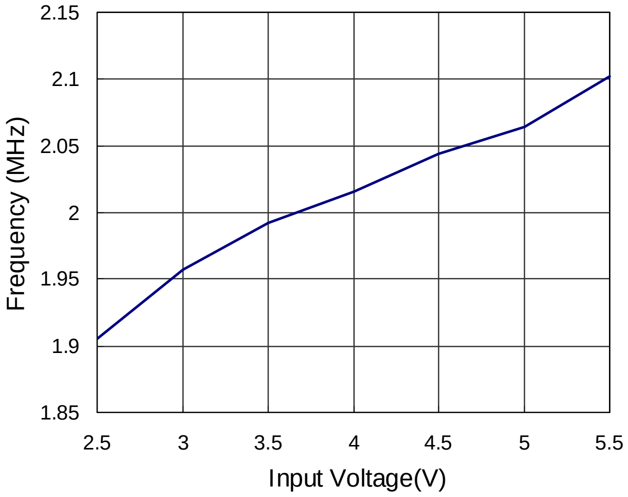
Typical Operating Characteristics

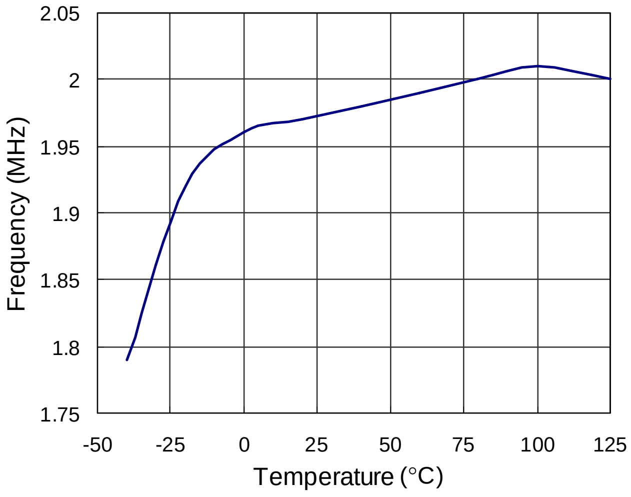

Output Voltage Deviation vs. Output Current

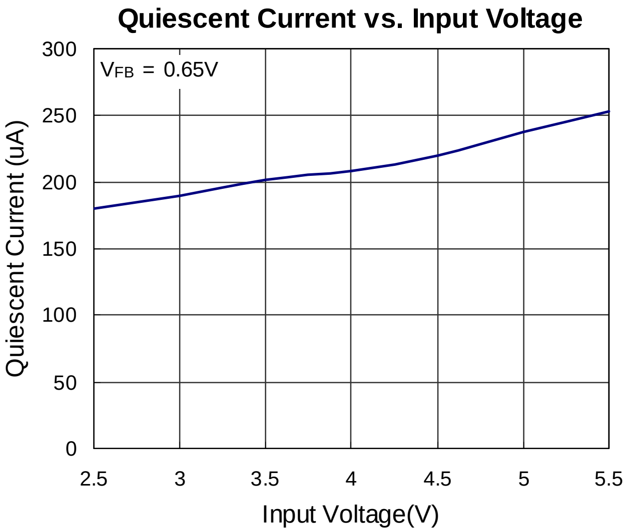

Output Voltage Deviation vs. Temperature

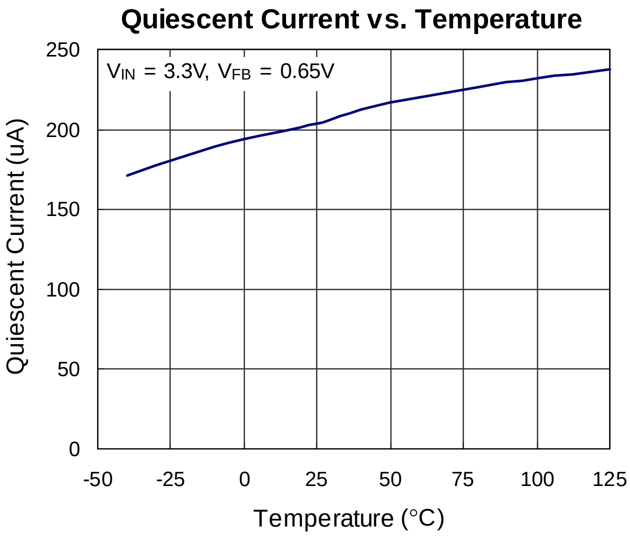

Efficiency vs. Output Current

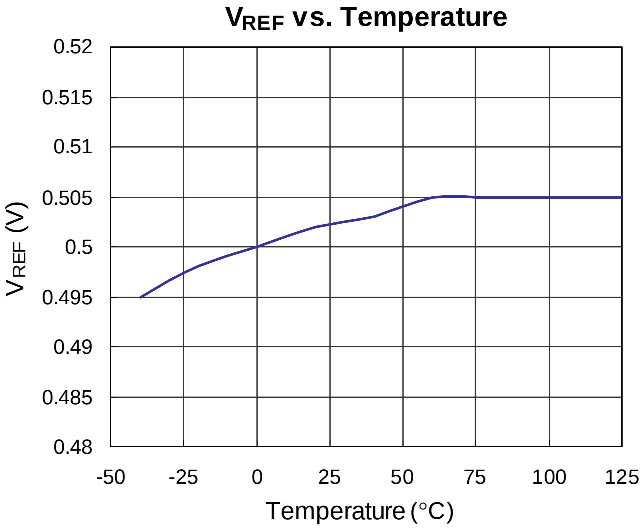

Efficiency vs. Temperature

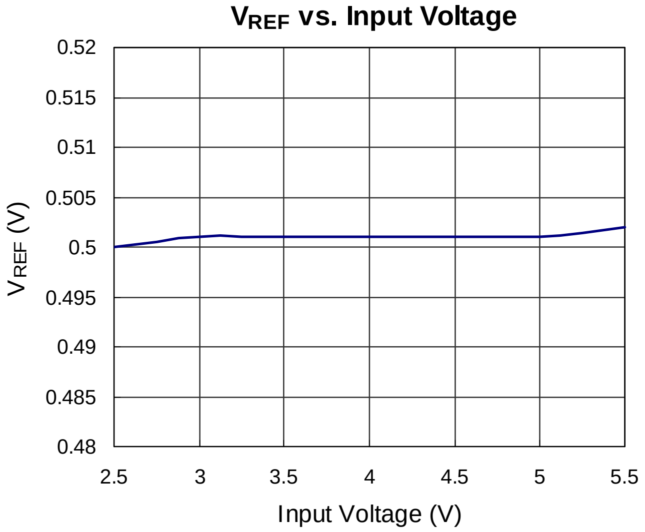

Frequency vs. Input Voltage

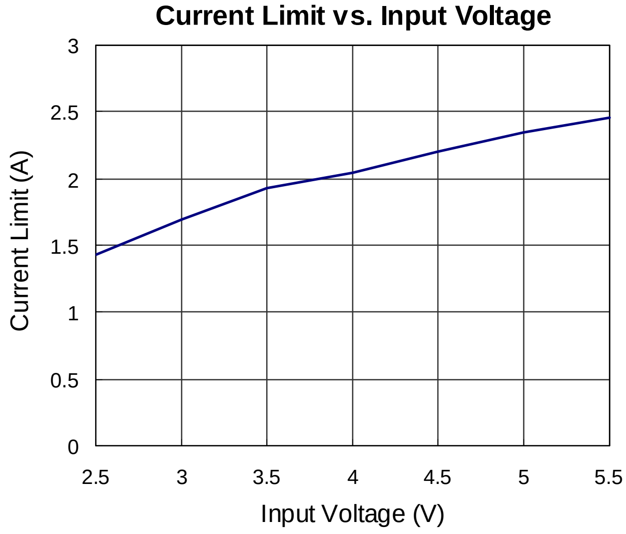

Frequency vs.Temperature

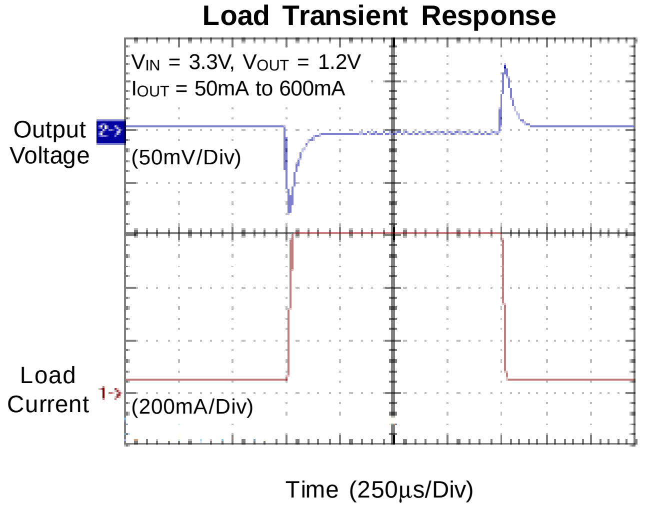

Quiescent Current vs. Input Voltage
VFB = 0.65V
Quiescent Current (uA)
300
250
200
150
100
50
0
2.5
3
3.5
4
4.5
5
5.5
Input Voltage(V)


Quiescent Current vs. Temperature
VIN = 3.3V, VFB = 0.65V
Quiescent Current (uA)
250
200
150
100
50
0
-50
-25
0
25
50
75
100
125
Temperature (°C)

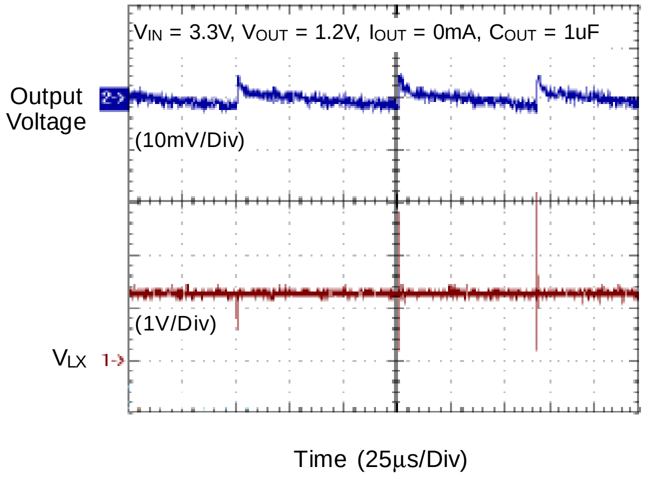

VREF vs. Temperature
VREF (V)
0.52
0.515
0.51
0.505
0.5
0.495
0.49
0.485
0.48
-50
-25
0
25
50
75
100
125
Temperature (°C)


VREF vs. Input Voltage
VREF (V)
0.52
0.515
0.51
0.505
0.5
0.495
0.49
0.485
0.48
2.5
3
3.5
4
4.5
5
5.5
Input Voltage (V)

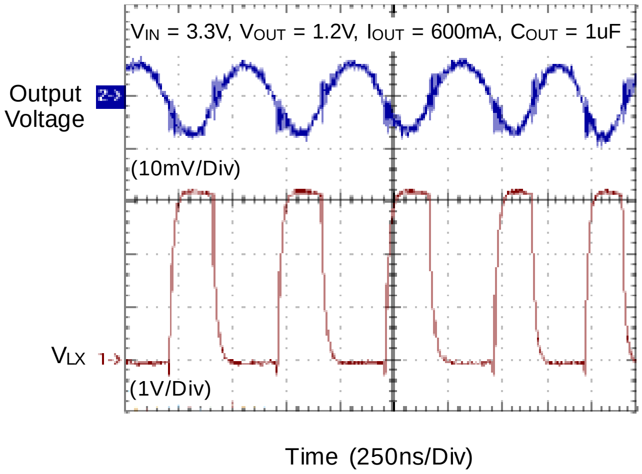

Current Limit vs. Input Voltage
Current Limit (A)
3
2.5
2
1.5
1
0.5
0
2.5
3
3.5
4
4.5
5
5.5
Input Voltage (V)


Load Transient Response
VIN = 3.3V, VOUT = 1.2V
IOUT = 50mA to 600mA
Output Voltage
(50mV/Div)
Load Current
(200mA/Div)
Time (250µs/Div)

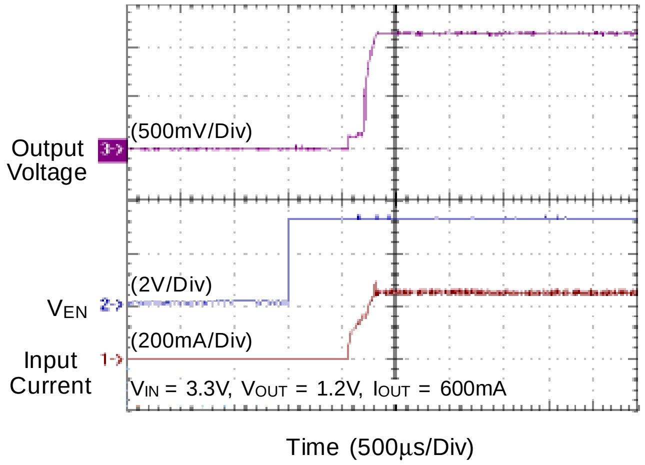
Steady State



Steady State



Soft Start Function



Application Information

RT8003 is a pulse-width-modulated (PWM) step-down DC-DC converter. Capable of delivering 600mA output current over a wide input voltage range from 2.4V to 5.5V. The RT8003 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range such as cellular phones, PDAs and handy terminals.

Chip Enable/Disable and Soft Start

Four operational modes are available: PWM, PSM, Low-Drop-Out and shut-down modes. Pulling EN pin lower than 0.4V shuts down the RT8003 and reduces its quiescent current to 1μA. Pulling EN pin higher than 1.5V enables the RT8003 and initiates the softstart cycle. RT8003 has internal soft-start that can reduce the Inrush Current during the rising of Output Voltage.

PWM Operation

During normal operation, the RT8003 regulates output voltage by switching at a constant frequency transferring the power to the load in each cycle by PWM. The RT8003 uses a slope-compensated, current-mode PWM controller capable of achieving 100% duty cycle. At each rising edge of the internal oscillator, the Control Logic cell sends a PWM ON signal to the Driver cell to turn on internal P-MOSFET. This allows current to ramp up through the inductor to the load, and stores energy in a magnetic field. The switch remains on until either the current-limit is tripped or the PWM comparator signals for the output in regulation. After the switch is turned off, the inductor releases the magnetic energy and forces current through the N-MOSFET synchronous rectifier to the output-filter capacitor and load. The output-filter capacitor stores charge when the inductor current is above the average output current and releases charge when the inductor current is below the average current to smooth the output voltage across the load. A Zero Detector monitors inductor current by sensing voltage drop across the N-MOSFET synchronous rectifier when it turns on. The N-MOSFET turns off and allows the converter entering discontinuous conduction mode when the inductor current decreases to zero. The zero current detection on threshold is about 80mA.This reduces conduction loss and increase power conversion efficiency at light load condition.

PSM Operation

Consequently, the converter will enter pulse-skipping mode (PSM) during extreme light load condition or when modulation index (V_{OUT}/V_{IN}) is extreme low. This could reduce switching loss and further increase power conversion efficiency.

Over Current Protection

The RT8003 continuously monitors the inductor current by sensing the voltage across the P-MOSFET when it turns on. When the inductor current is higher than current limit threshold (1.8A typical), OCP activates and forces the P-MOSFET turning off to limit inductor current cycle by cycle.But it will shut down when the V_{OUT} trip the UV protection.

Output Voltage Setting and Feedback Network

The output voltage can be set from V_{REF} to V_{IN} by a voltage divider as: the internal V_{REF} is 0.5V with 1.5% accuracy. In practical application, keep R1 = 10kΩ respectively and choose appropriate R2 according to the required output voltage.

Inductor Selection

The output inductor is suggested as the table of suggested inductors for optimal performance. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current. If possible, choose an inductor with rated current higher than 2A so that it will not saturate even under short circuit condition.

Input Capacitor Selection

The input capacitor can filter the input peak current and noise at input voltage source. The capacitor with low ESR (effective series resistance) provides the small drop voltage to stabilize the input voltage during the transient loading. For input capacitor selection, the ceramic capacitors larger than 1μF is recommend. The capacitor must conform to the RMS current requirement. The maximum RMS ripple current is calculated as :

$$I_{RMS} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

Output Capacitor Selection

The capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient's edge. Typically, if the ESR requirement is satisfied, the capacitance is adequate to filtering. The output ripple voltage can be calculated as:

$$\Delta V_{OUT} = \Delta I_C \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{OSC}}\right)$$

Where f_{OSC} = operating frequency, C_{OUT} = output capacitance and $\Delta I_C = \Delta I_L$ = ripple current in the inductor.

The ceramic capacitor with low ESR value provides the low output ripple and low size profile. Connect a 1μF/2.2μF ceramic capacitor at output terminal for good performance and place the input and output capacitors as close as possible to the device.

Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8003.

1. For the main current paths as indicated in bold lines in Figure 1, keep their traces short and wide.

2. Put the input capacitor as close as possible to the device pins (VDD and GND).

3. LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.

4. Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8003.

5.Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

6. An example of 2-layer PCB layout is shown in Figure 2 to Figure 3 for reference.

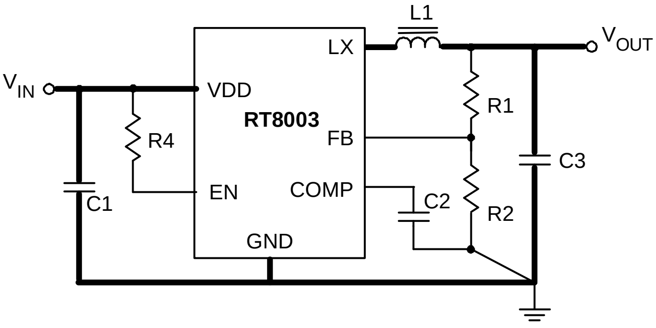


Figure 1

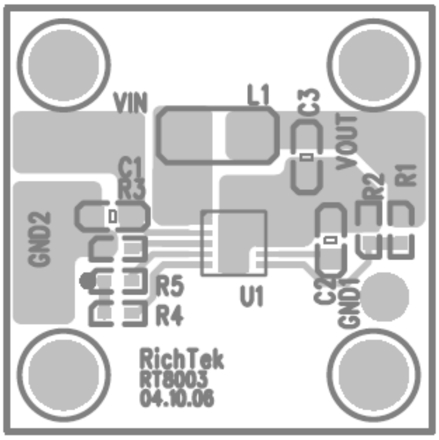


Figure 2. Top Layer

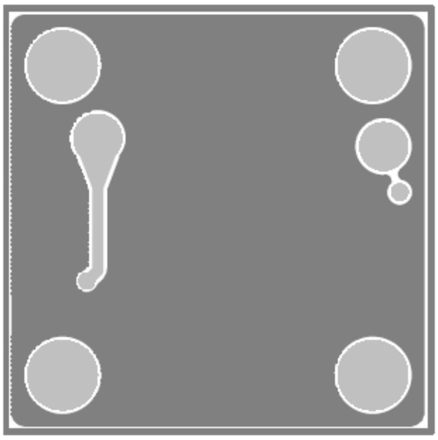
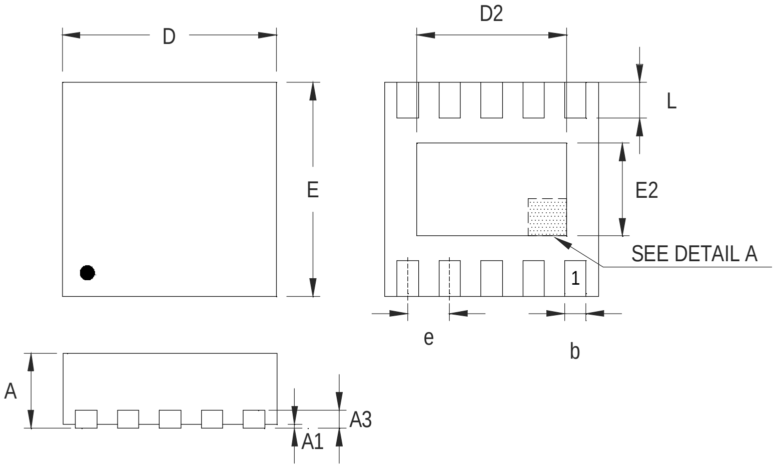
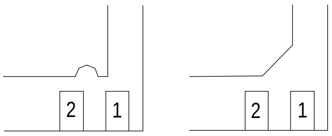


Figure 3. Bottom Layer

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 10L DFN 3x3 Package

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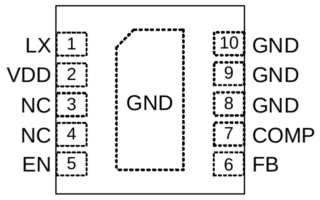
- Protable Instruments and Notebook Computers
- Celluar Phones, PDAs, and Handheld PCs
- USB-Based DSL Modems and Other Network Interface Cards

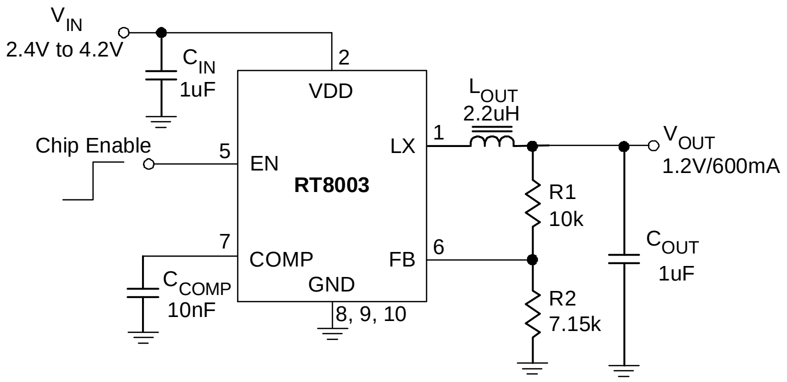
Pin Configurations

(TOP VIEW)



VDFN-10L 3x3

Typical Application Circuit



Recommended component selection for Typical Application Circuit.

V_{OUT} (V)	V_{IN} (V)	C_{IN} (uF)	C_{OUT} (uF)	L_{OUT} (uH)	R1 (kW)	R2 (kW)	C_{COMP} (nF)
0.5	2.4 to 3.3	1	1/2.2	2.2/1	10	Open	10
1	2.4 to 3.6	1	1/2.2	2.2/1	10	10	10
1.2	2.4 to 4.2	1	1/2.2	2.2/1	10	7.15	10
1.8	2.4 to 5.5	1	1/2.2	2.2/1	10	3.83	10
2.5	3.3 to 5.5	1	1/2.2	2.2/1	10	2.49	10
3.3	4.2 to 5.5	1	1/2.2	2.2/1	10	1.78	10

Suggested Inductors

Component Supplier	Series	Inductance (μH)	ESR (mW)	Current Rating (mA)	Dimensions (mm)
ABC	SR0302	1 2.2	60 90	2100 1650	3x2.8x2.5
Sumida	CDRH2D14	2.2	94	1000	3.2x3.2x1.55
TDK	VLP4612	1 2.5	110 170	1500 1100	4.6x3.4x1.2

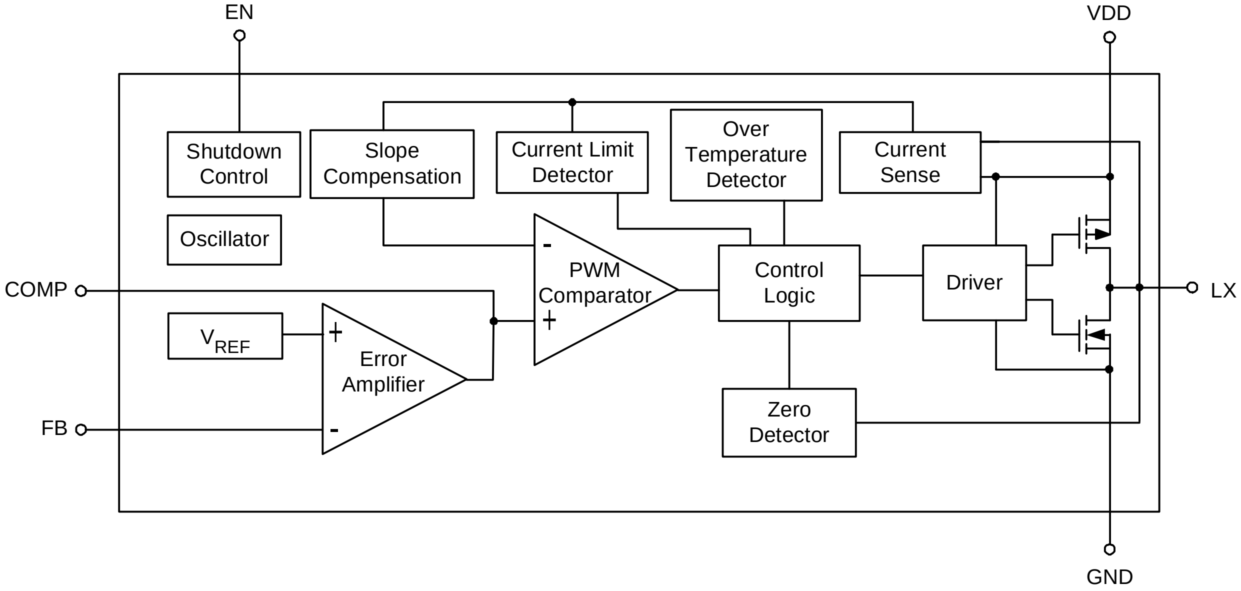
Suggested Capacitors For C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (uF)	Case Size
TDK	C1608X5R1A105M	1	0603
	C1608X5R1A225M	2.2	0603
Panasonic	ECJ1VB0J105M	1	0603
	ECJ1VB0J225M	2.2	0603
TAIYO YUDEN	JMK107BJ105M	1	0603
	JMK107BJ225M	2.2	0603

Functional Pin Description

No	Pin Name	Pin Function
1	LX	Internal Power MOSFET Switches Output. Connect this pin to the inductor.
2	VDD	Power Input Supply. Input voltage which supplies current to the output pin. Connect this pin with a low-ESR capacitor to GND
3,4	NC	No Internal Connection
5	EN	Chip Enable (Active High). Logic low shuts down the converter. Floating this pin is forbidden.
6	FB	Switcher Feedback Voltage. This pin is the inverting input of the error amplifier. FB senses the switcher output through an external resistor divider network. FB regulation voltage is 0.5V.
7	COMP	Compensation Input. This pin is the output of the internal error amplifier. Connect an external capacitor to compensate the regulator controlled loop.
8,9,10	GND	Ties the pin directly to the cathode terminal of C_{IN} and C_{OUT} and ground plane with the lowest impedance. Signal and Common Ground (Exposed thermal pad is connected to GND). The GND pad area should be as large as possible and using many vias to conduct the heat into the buried GND plate of PCB layer. All small-signal, compensation and feedback components should connect to this pin.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage ---------- –0.3V to 6V
- LX Voltage ---------- –0.3V to (V_{DD} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  VDFN-10L 3x3 ---------- 1.923W
- Package Thermal Resistance (Note 4)
  VDFN-10L 3x3, θ_{JA} ---------- 52°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage ---------- 2.4V to 5.5V
- Enable Input Voltage, V_{EN} ---------- 0V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
Quiescent Current	I_Q	V_{EN} = 3.3V, V_{FB} = V_{REF} + 0.15V, I_{OUT} = 0mA	--	200	400	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	0.01	1	μA
Reference						
Reference Voltage	V_{REF}		0.4925	0.5	0.5075	V
Oscillator						
Switching Frequency Range	f_{OSC}		1.7	2.0	2.3	MHz
Maximum Duty Cycle	DC	V_{DD} = V_{OUT}	100	--	--	%
Output Voltage						
Line Regulation		V_{DD} = 2.4V to 5.5V, I_{LOAD} = 100mA	--	--	+1.5	%
Load Regulation		10mA < I_{LOAD} < 600mA	--	--	+1.5	%
Power Switches						
$R_{DS(ON)}$ of P-Channel MOSFET	R_{P_FET}	V_{DD} = 3.3V, I_{LX} = 300mA	--	230	--	mΩ
$R_{DS(ON)}$ of N-Channel MOSFET	R_{N_FET}	V_{DD} = 3.3V, I_{LX} = –300mA	--	180	--	mΩ
Current Limit	I_{LIMIT}	V_{DD} = 3.3V, V_{FB} = V_{REF} - 0.15V	--	1.8	--	A

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Logic Input							
EN Threshold	Logic-Low Voltage	V_{IL}	V_{DD} = 2.4V to 5.5V, Shutdown	--	--	0.4	V
	Logic-High Voltage	V_{IH}	V_{DD} = 2.4V to 5.5V, Enable	1.5	--	--	
Protection							
Thermal Shutdown Temperature		T_{SD}		--	180	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

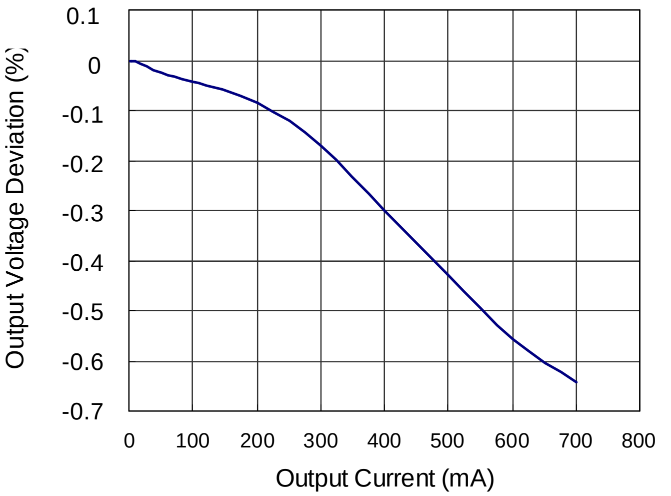
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

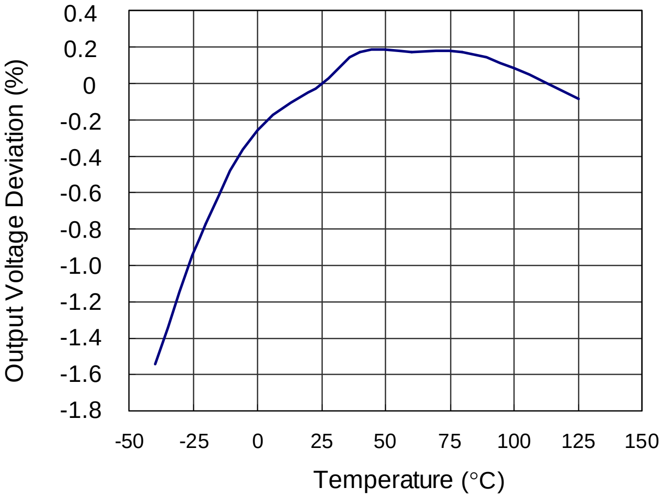
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Typical Operating Characteristics

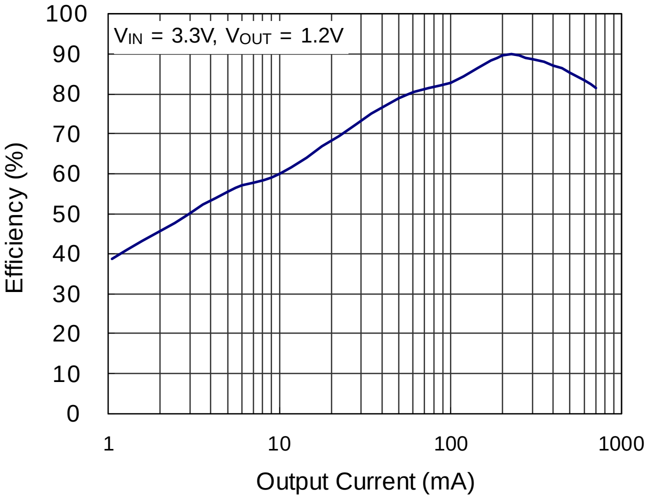
Output Voltage Deviation vs. Output Current



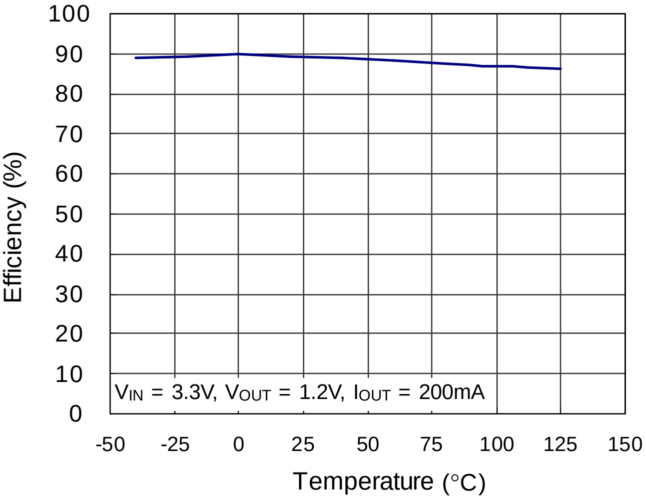
Output Voltage Deviation vs. Temperature



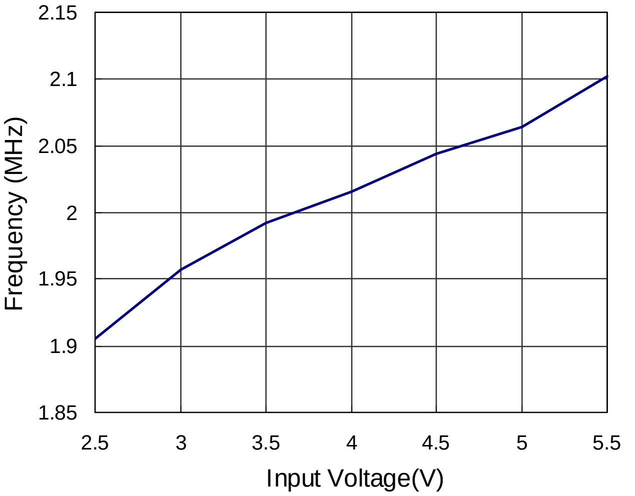
Efficiency vs. Output Current



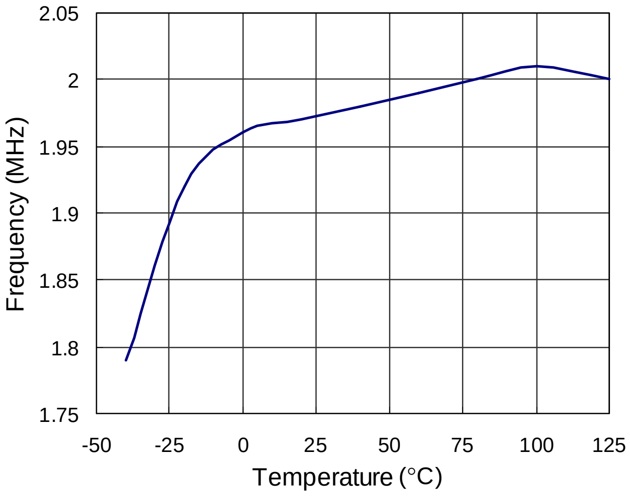
Efficiency vs. Temperature

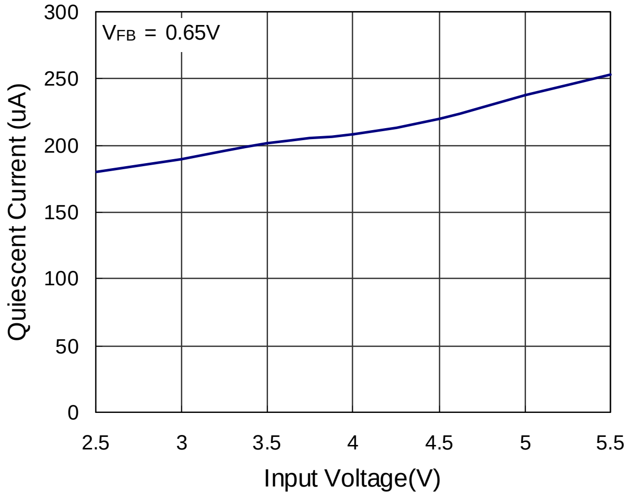


Frequency vs. Input Voltage

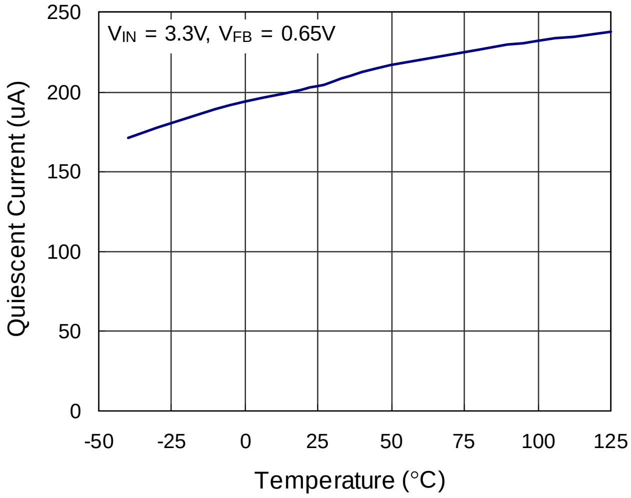


Frequency vs.Temperature

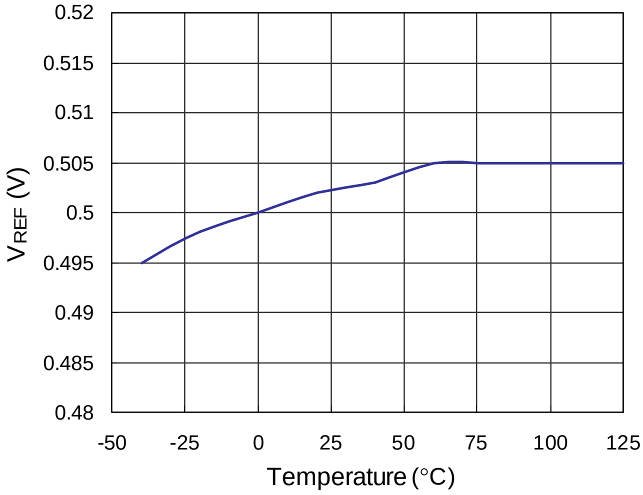




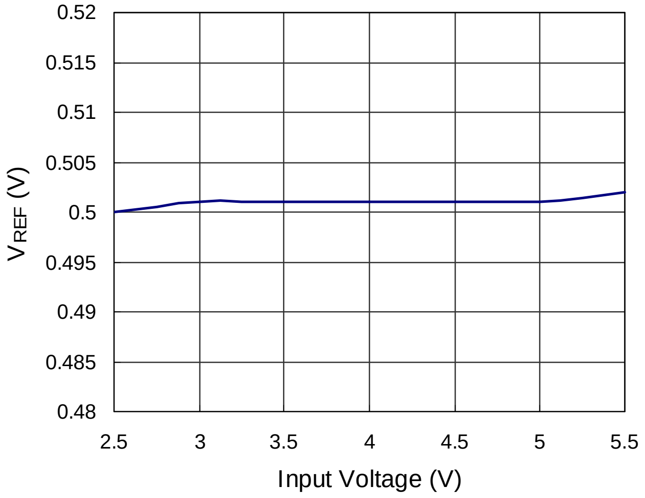
Quiescent Current vs. Input Voltage



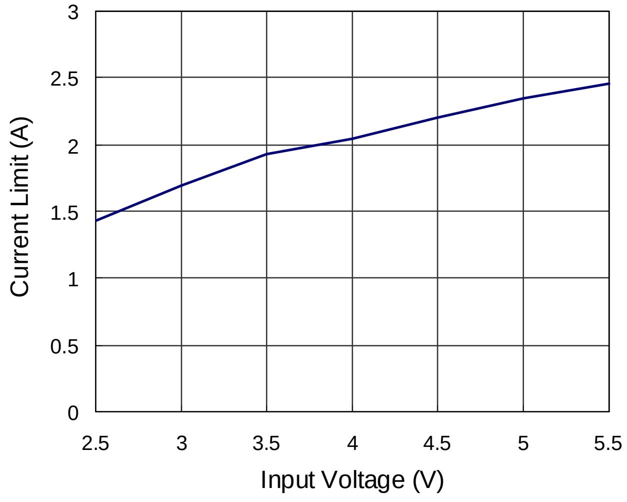
Quiescent Current vs. Temperature



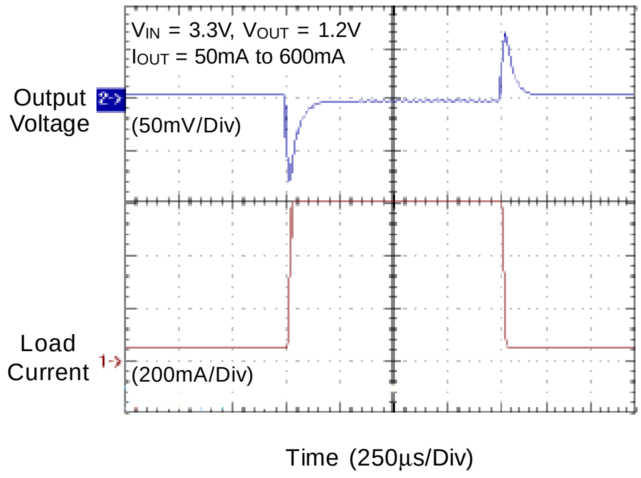
V_{REF} vs. Temperature



V_{REF} vs. Input Voltage

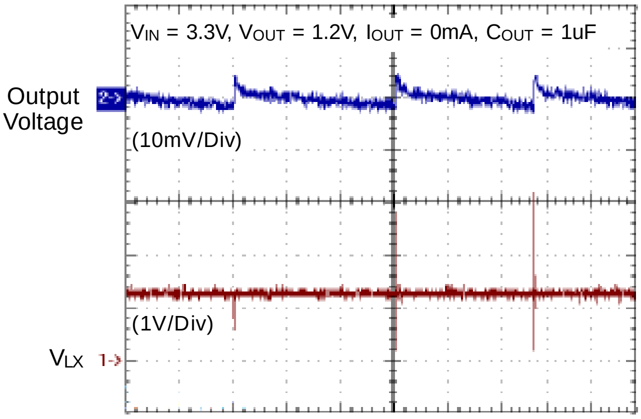


Current Limit vs. Input Voltage



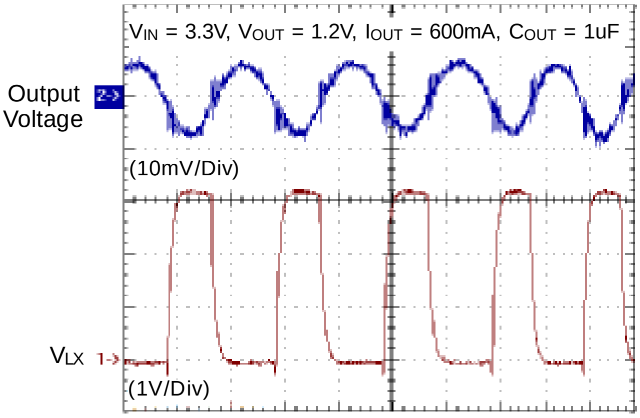
Load Transient Response

Steady State



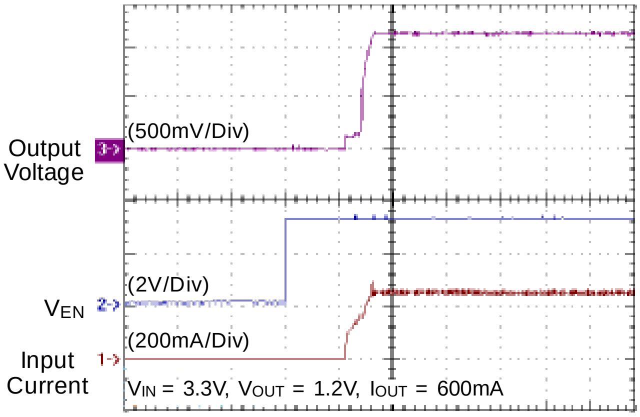
Time (25μs/Div)

Steady State



Time (250ns/Div)

Soft Start Function



Time (500μs/Div)

Application Information

RT8003 is a pulse-width-modulated (PWM) step-down DC-DC converter. Capable of delivering 600mA output current over a wide input voltage range from 2.4V to 5.5V. The RT8003 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range such as cellular phones, PDAs and handy terminals.

Chip Enable/Disable and Soft Start

Four operational modes are available: PWM, PSM, Low-Drop-Out and shut-down modes. Pulling EN pin lower than 0.4V shuts down the RT8003 and reduces its quiescent current to 1μA. Pulling EN pin higher than 1.5V enables the RT8003 and initiates the softstart cycle. RT8003 has internal soft-start that can reduce the Inrush Current during the rising of Output Voltage.

PWM Operation

During normal operation, the RT8003 regulates output voltage by switching at a constant frequency transferring the power to the load in each cycle by PWM. The RT8003 uses a slope-compensated, current-mode PWM controller capable of achieving 100% duty cycle. At each rising edge of the internal oscillator, the Control Logic cell sends a PWM ON signal to the Driver cell to turn on internal P-MOSFET. This allows current to ramp up through the inductor to the load, and stores energy in a magnetic field. The switch remains on until either the current-limit is tripped or the PWM comparator signals for the output in regulation. After the switch is turned off, the inductor releases the magnetic energy and forces current through the N-MOSFET synchronous rectifier to the output-filter capacitor and load. The output-filter capacitor stores charge when the inductor current is above the average output current and releases charge when the inductor current is below the average current to smooth the output voltage across the load. A Zero Detector monitors inductor current by sensing voltage drop across the N-MOSFET synchronous rectifier when it turns on. The N-MOSFET turns off and allows the converter entering discontinuous conduction mode when the inductor current decreases to zero. The zero current detection on threshold is about 80mA.This reduces conduction loss and increase power conversion efficiency at light load condition.

PSM Operation

Consequently, the converter will enter pulse-skipping mode (PSM) during extreme light load condition or when modulation index (V_{OUT}/V_{IN}) is extreme low. This could reduce switching loss and further increase power conversion efficiency.

Over Current Protection

The RT8003 continuously monitors the inductor current by sensing the voltage across the P-MOSFET when it turns on. When the inductor current is higher than current limit threshold (1.8A typical), OCP activates and forces the P-MOSFET turning off to limit inductor current cycle by cycle.But it will shut down when the V_{OUT} trip the UV protection.

Output Voltage Setting and Feedback Network

The output voltage can be set from V_{REF} to V_{IN} by a voltage divider as: the internal V_{REF} is 0.5V with 1.5% accuracy. In practical application, keep R1 = 10kΩ respectively and choose appropriate R2 according to the required output voltage.

Inductor Selection

The output inductor is suggested as the table of suggested inductors for optimal performance. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current. If possible, choose an inductor with rated current higher than 2A so that it will not saturate even under short circuit condition.

Input Capacitor Selection

The input capacitor can filter the input peak current and noise at input voltage source. The capacitor with low ESR (effective series resistance) provides the small drop voltage to stabilize the input voltage during the transient loading. For input capacitor selection, the ceramic capacitors larger than 1μF is recommend. The capacitor must conform to the RMS current requirement. The maximum RMS ripple current is calculated as :

$$I_{RMS} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}\,(V_{IN} - V_{OUT})}}{V_{IN}}$$

Output Capacitor Selection

The capacitor′s ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient′s edge. Typically, if the ESR requirement is satisfied, the capacitance is adequate to filtering. The output ripple voltage can be calculated as:

$$\Delta V_{OUT} = \Delta I_C \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{OSC}}\right)$$

Where f_{OSC} = operating frequency, C_{OUT} = output capacitance and ΔI_C = ΔI_L = ripple current in the inductor.

The ceramic capacitor with low ESR value provides the low output ripple and low size profile. Connect a 1μF/2.2μF ceramic capacitor at output terminal for good performance and place the input and output capacitors as close as possible to the device.

Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8003.

1. For the main current paths as indicated in bold lines in Figure 1, keep their traces short and wide.

2. Put the input capacitor as close as possible to the device pins (VDD and GND).

3. LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.

4. Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8003.

5.Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

6. An example of 2-layer PCB layout is shown in Figure 2 to Figure 3 for reference.

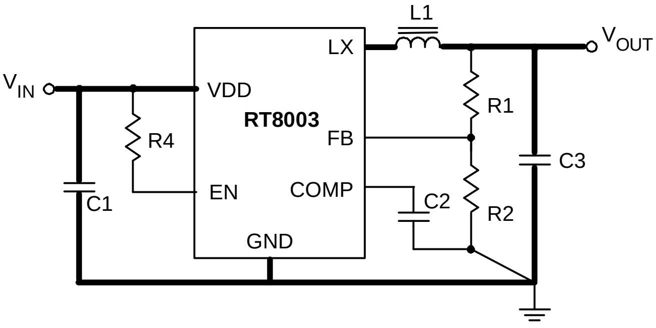


Figure 1

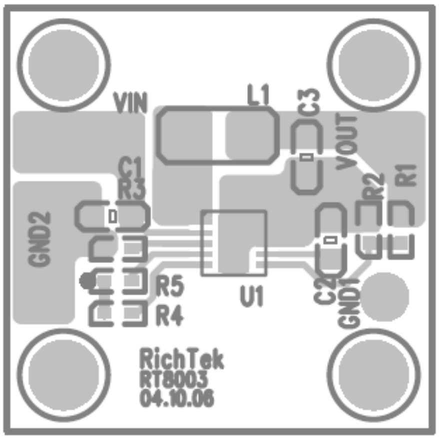


Figure 2. Top Layer

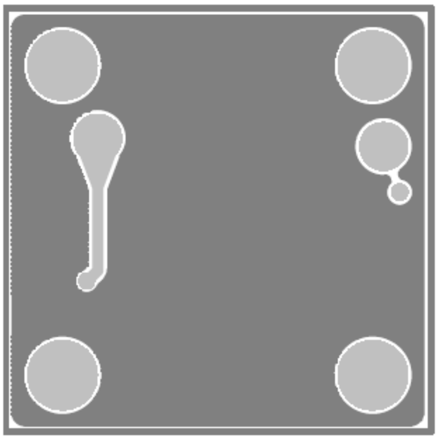
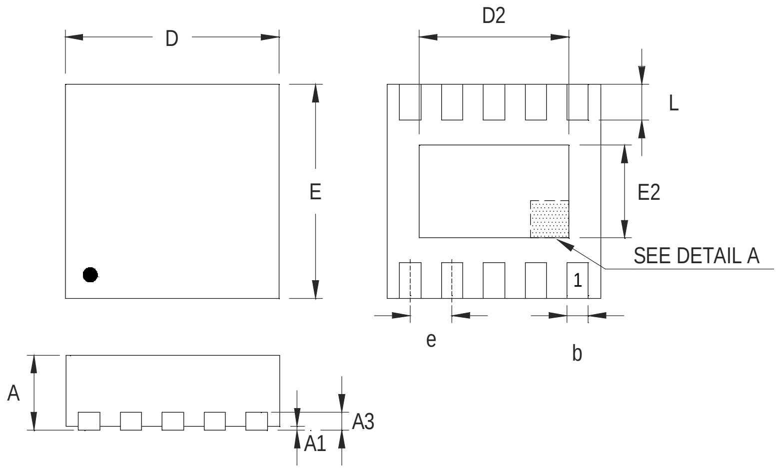
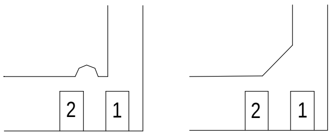


Figure 3. Bottom Layer

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 10L DFN 3x3 Package

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