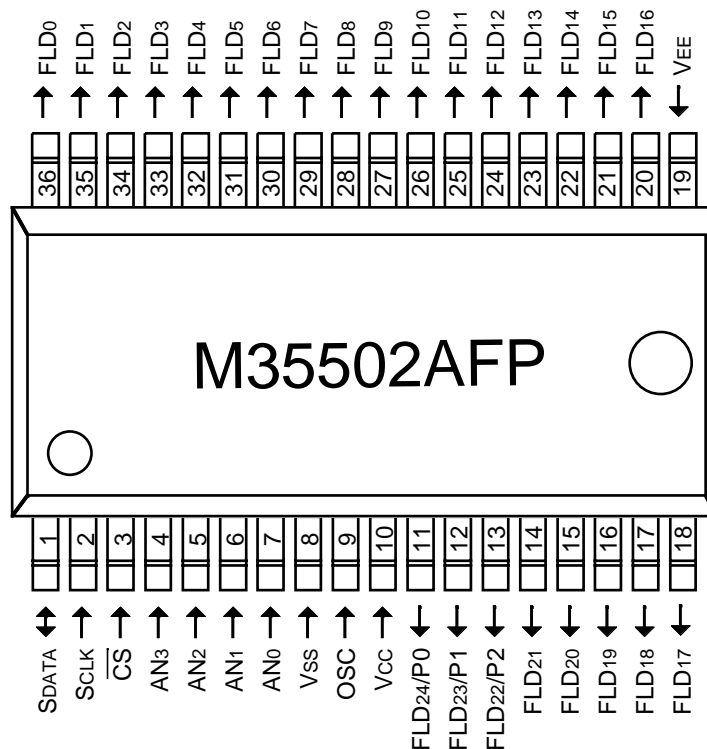


DESCRIPTION/FEATURES

- High-breakdown-voltage output port 25
 - Segment output 8 to 20
 - Digit output 5 to 16
 (Ports P0 to P2 are also used as normal output ports)
 - Output breakdown $V_{CC} - 45 V$
 - Output current -18 mA (at DIG selecting),
 -7 mA (at SEG selecting)
 - Pull-down resistor built-in
 - Dimmer switch 4 levels
- A-D converter 8-bit X 4 channels
 - Absolute accuracy $\pm 3 \text{ LSB}$
- Serial I/O 3 (CS controller, external clock)
 - Noise filter built-in
 (in serial input pin and clock pin, 2 MHz sampling)
 - FLD display data input
 - A-D conversion data output
 - Command input
- Package 36P2R-G
- Oscillation circuit CR oscillation circuit (external capacitor)
 - Oscillation frequency 2 MHz
- Power source voltage 4.0 to 5.5 V

PIN CONFIGURATION (TOP VIEW)



Package type: 36P2R-G

Fig.1 Pin configuration of M35502AFP

FUNCTIONAL BLOCK

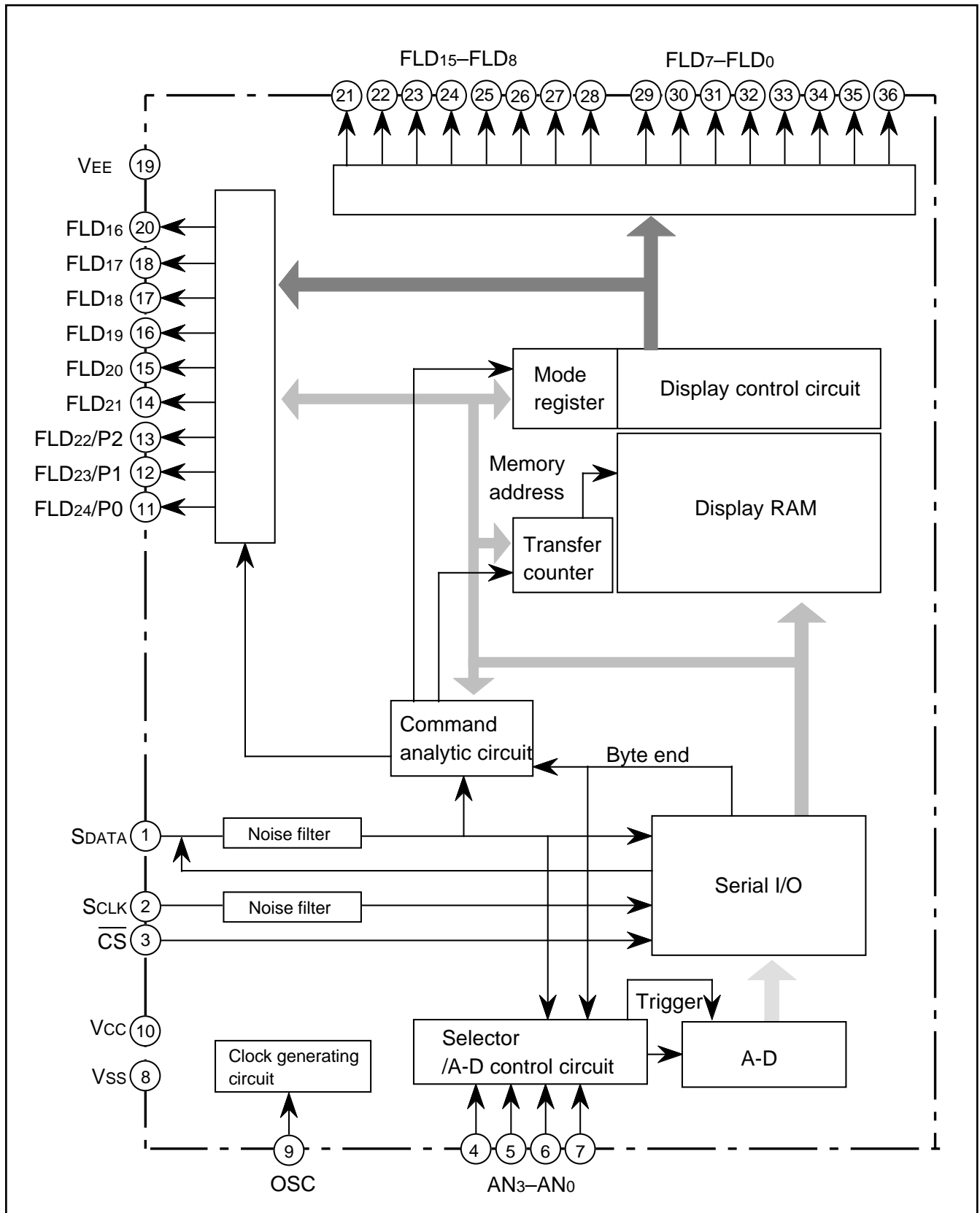


Fig.2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Input	Output	Function
VCC, VSS	Power source			• Apply voltage of 5 V to Vcc, and 0 V to Vss.
VEE	Pull-down power source			• Applies voltage supplied to pull-down resistors.
OSC	Clock input	Input		• Connect an external capacitor to this pin.
CS	Chip select	CMOS input		• Serial transfer is possible by inputting "L" signal. • Pull-up resistor is built in.
SCLK	Serial clock	CMOS input Noise filter		• Clock for serial transfer is input. • Read a clock twice with 2 MHz sampling clock and judge if it is a noise or not.
SDATA	Serial input/output	CMOS input Noise filter	N-channel open-drain	• Serial data is input/output. • In input mode, read a clock twice with 2 MHz sampling clock and judge if it is a noise or not.
FLD24/P0 – FLD22/P2	Digit/Port		P-channel open-drain	• Pin for ordinary output or digit output. • At reset this port is set to VEE level through a pull-down resistor.
FLD21– FLD0	Segment/Digit		P-channel open-drain	• Pin for digit output or segment output. • At reset this port is set to VEE level through a pull-down resistor.

PORT BLOCK

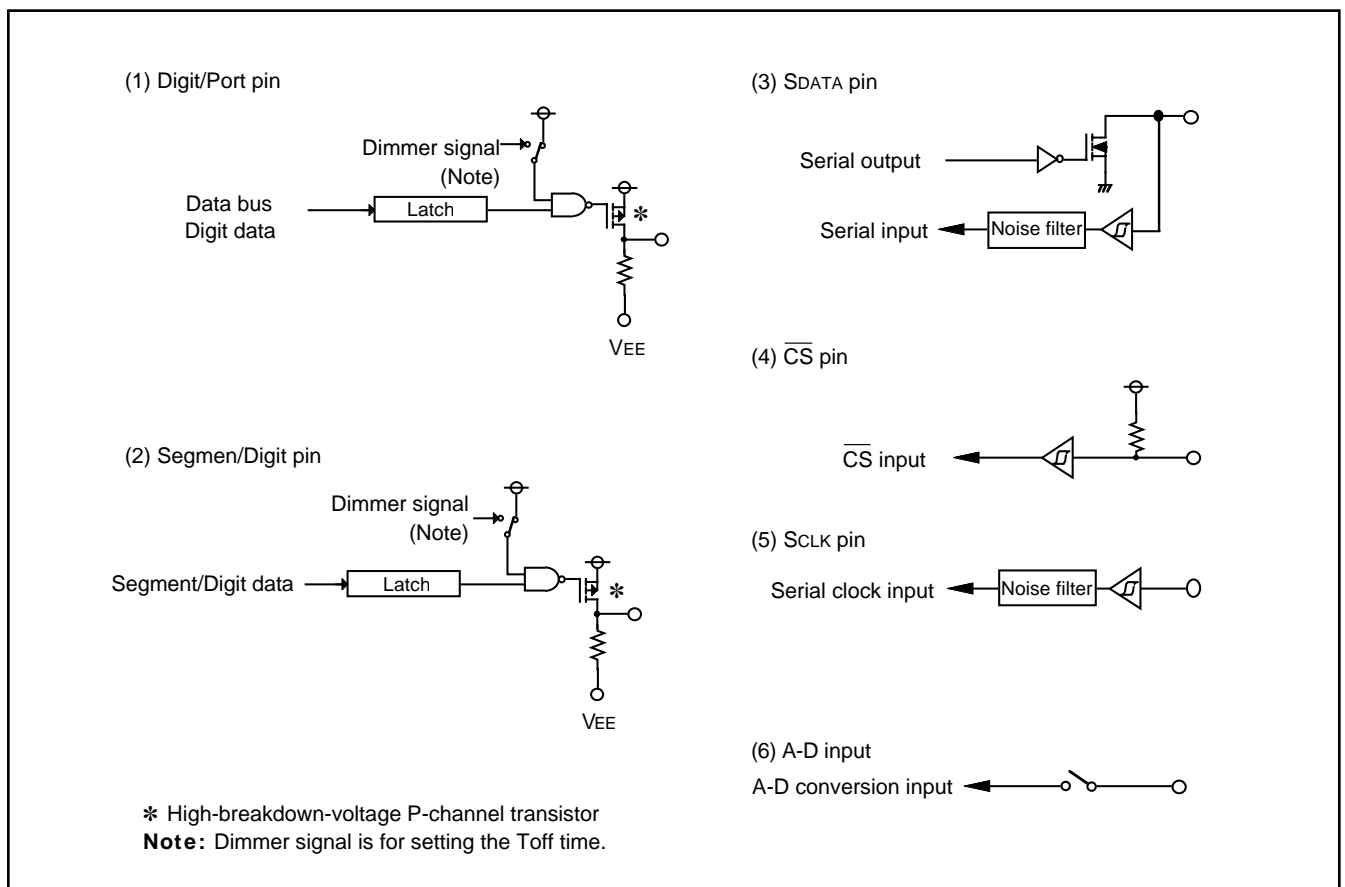


Fig.3 Port block diagram

COMMAND STYLE

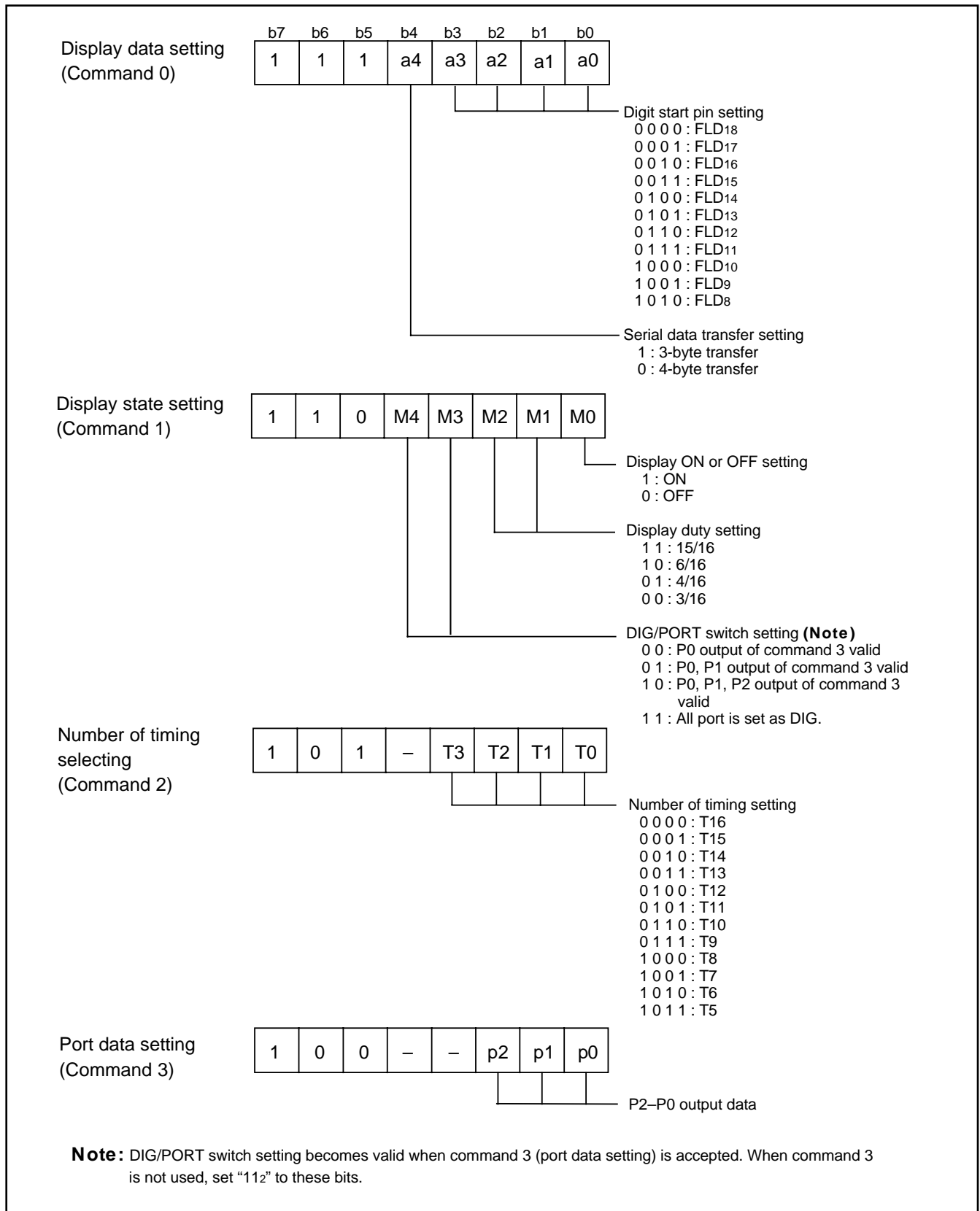


Fig.4 Command style

SERIAL I/O PROTOCOL

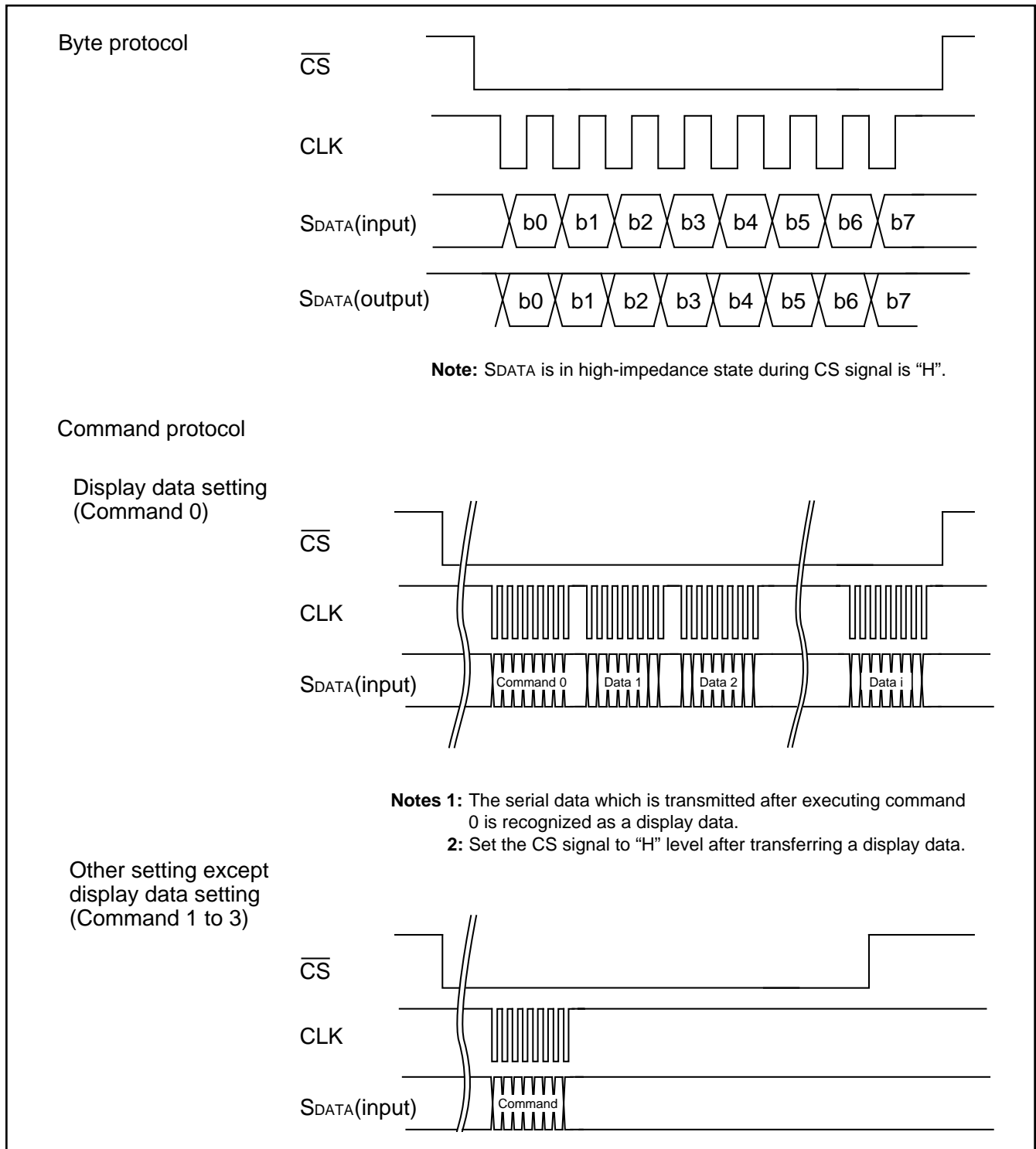
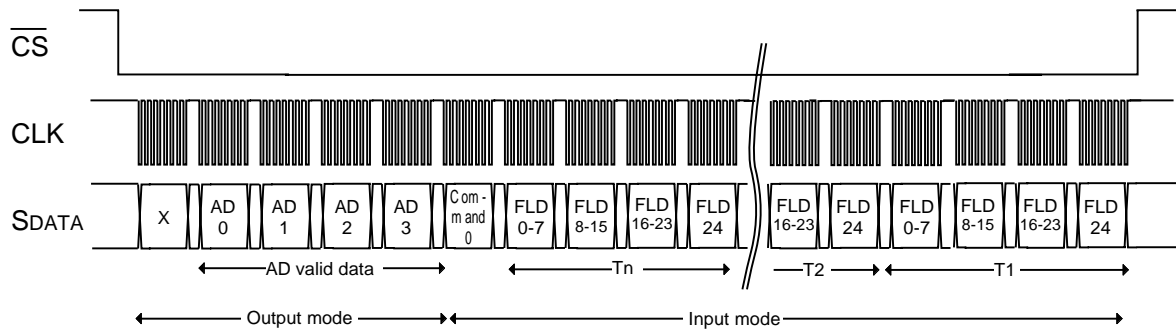


Fig.5 Serial I/O protocol

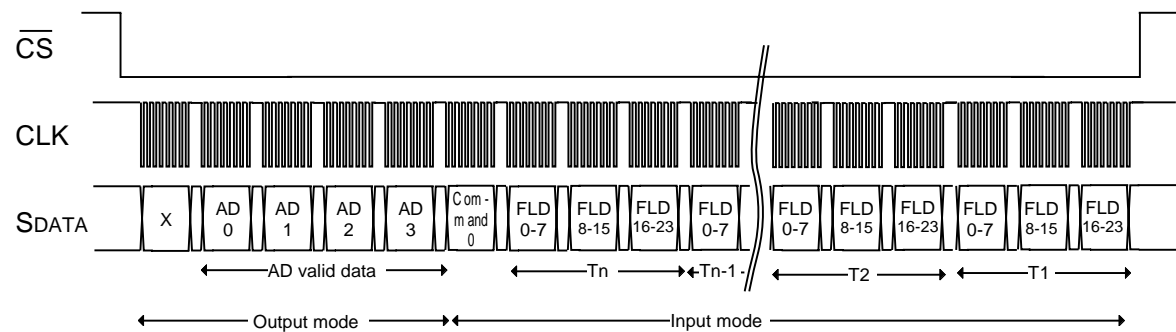
SERIAL COMMUNICATION FORMAT (DISPLAY DATA, A-D OUTPUT)

When using 25 high-breakdown-voltage ports (segment + grid) (4-byte transfer)



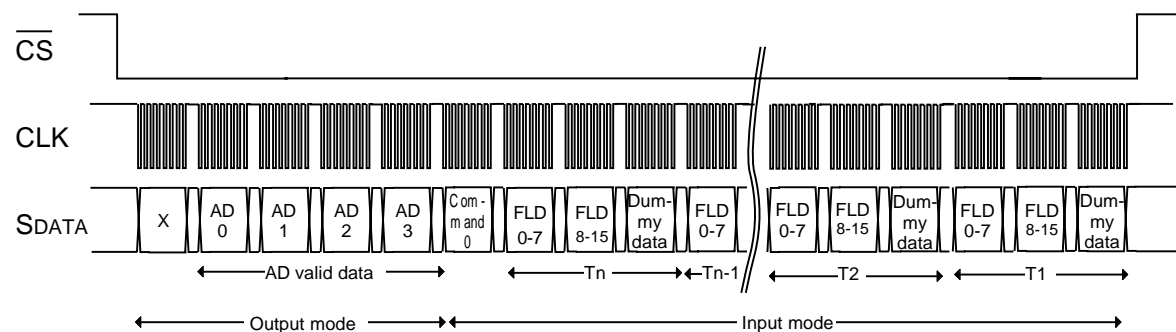
The SDATA pin becomes output mode from after the \overline{CS} pin falling until the 5th byte of serial data.
The SDATA becomes command input mode from the 6th byte of serial data.

When using 24 high-breakdown-voltage ports (segment + grid) (3-byte transfer)



The SDATA pin becomes output mode from after the \overline{CS} pin falling until the 5th byte of serial data.
The SDATA becomes command input mode from the 6th byte of serial data.

When using 16 high-breakdown-voltage ports (segment + grid) or less (3-byte transfer)



Transfer dummy data to the third byte of each timing.
The SDATA pin becomes output mode from after the \overline{CS} pin falling until the 5th byte of serial data.
The SDATA becomes command input mode from the 6th byte of serial data.

Fig.6 Serial communication format

FLD DISPLAY TIMING

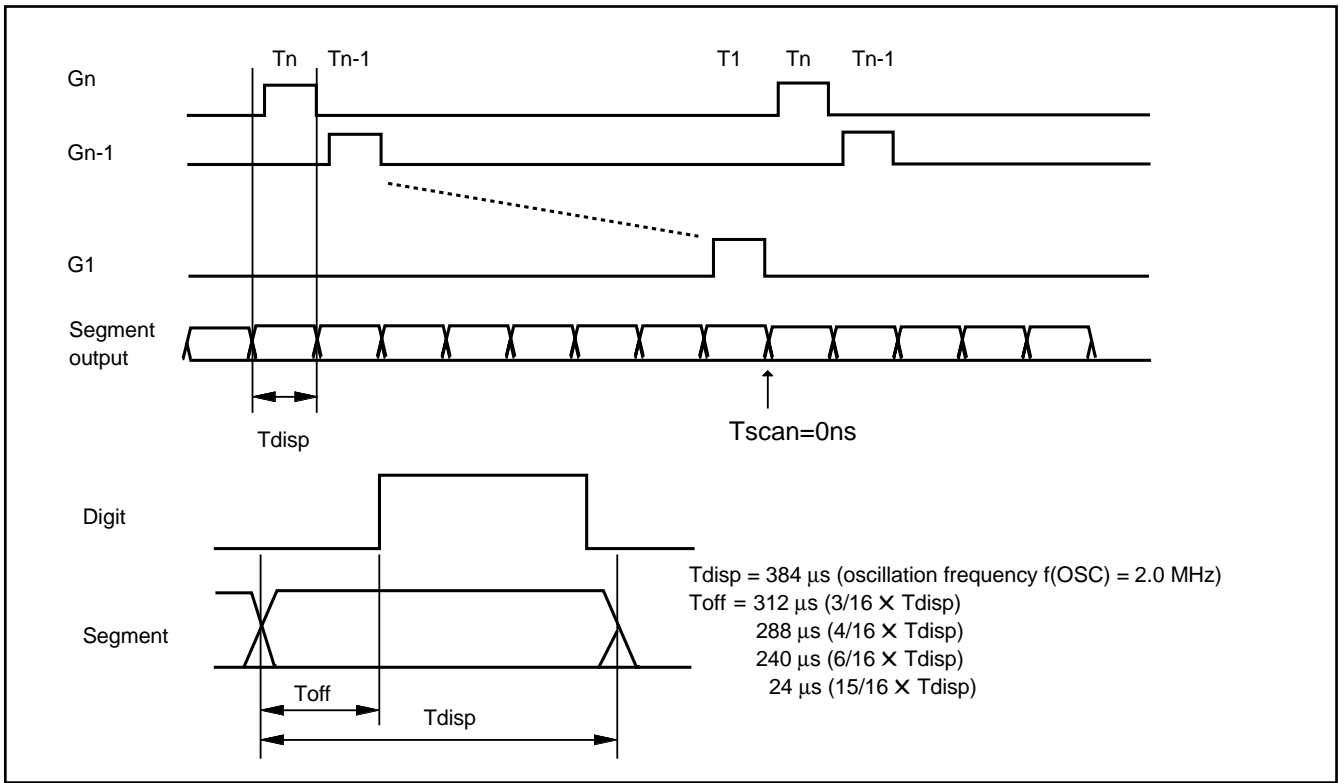


Fig.7 FLD display timing diagram

SEGMENT/DIGIT SETTING EXAMPLE

	PORT	FLD	Grid: 5 Segment: 8	Grid: 7 Segment: 8	Grid: 10 Segment: 8	Grid: 7 Segment: 18
1		FLD0	SEG1	SEG1	SEG1	SEG1
2		FLD1	SEG2	SEG2	SEG2	SEG2
3		FLD2	SEG3	SEG3	SEG3	SEG3
4		FLD3	SEG4	SEG4	SEG4	SEG4
5		FLD4	SEG5	SEG5	SEG5	SEG5
6		FLD5	SEG6	SEG6	SEG6	SEG6
7		FLD6	SEG7	SEG7	SEG7	SEG7
8		FLD7	SEG8	SEG8	SEG8	SEG8
9		FLD8	GRID5	GRID7	GRID10	SEG9
10		FLD9	GRID4	GRID6	GRID9	SEG10
11		FLD10	GRID3	GRID5	GRID8	SEG11
12		FLD11	GRID2	GRID4	GRID7	SEG12
13		FLD12	GRID1	GRID3	GRID6	SEG13
14		FLD13		GRID2	GRID5	SEG14
15		FLD14		GRID1	GRID4	SEG15
16		FLD15			GRID3	SEG16
17		FLD16			GRID2	SEG17
18		FLD17			GRID1	SEG18
19		FLD18				GRID7
20		FLD19				GRID6
21		FLD20				GRID5
22		FLD21				GRID4
23	P2	FLD22				GRID3
24	P1	FLD23				GRID2
25	P0	FLD24				GRID1

Fig.8 Segment/Digit setting example

BIT ALLOCATION FOR DISPLAY RAM

ADDRESS	b7	b6	b5	b4	b3	b2	b1	b0		b7	b6	b5	b4	b3	b2	b1	b0			
00 ¹⁶								FLD 24	T1	20 ¹⁶							FLD 24	T9		
01 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		21 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17		FLD 16	
02 ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8		22 ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9		FLD 8	
03 ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0		23 ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1		FLD 0	
04 ¹⁶								FLD 24		24 ¹⁶									FLD 24	
05 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		T2	25 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18		FLD 17	FLD 16
06 ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8			26 ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10		FLD 9	FLD 8
07 ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0			27 ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2		FLD 1	FLD 0
08 ¹⁶								FLD 24	28 ¹⁶									FLD 24		
09 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	T3		29 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
0A ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8			2A ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
0B ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0			2B ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
0C ¹⁶								FLD 24			2C ¹⁶								FLD 24	
0D ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		T4	2D ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
0E ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8			2E ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
0F ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0			2F ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
10 ¹⁶								FLD 24			30 ¹⁶								FLD 24	
11 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	T5		31 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
12 ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8			32 ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
13 ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0			33 ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
14 ¹⁶								FLD 24			34 ¹⁶								FLD 24	
15 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		T6	35 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
16 ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8			36 ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
17 ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0			37 ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
18 ¹⁶								FLD 24			38 ¹⁶								FLD 24	
19 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	T7		39 ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
1A ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8			3A ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
1B ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0			3B ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
1C ¹⁶								FLD 24			3C ¹⁶								FLD 24	
1D ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		T8	3D ¹⁶	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
1E ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8			3E ¹⁶	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
1F ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0			3F ¹⁶	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	

Fig.9 Bit allocation for display RAM

CLOCK GENERATING CIRCUIT

Oscillating circuit is built up by connecting a capacitor between pins OSC and Vss.

When supplying a clock externally, input it to the OSC pin.

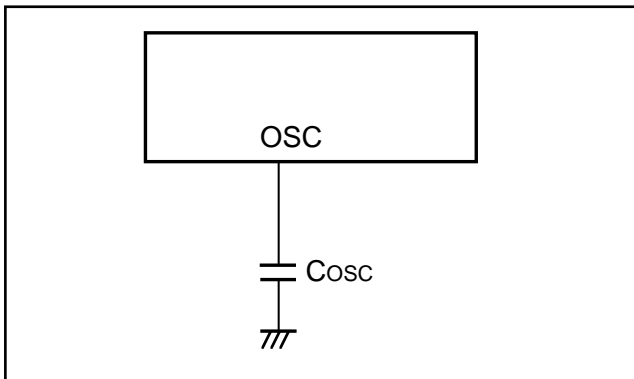


Fig.10 CR generating circuit

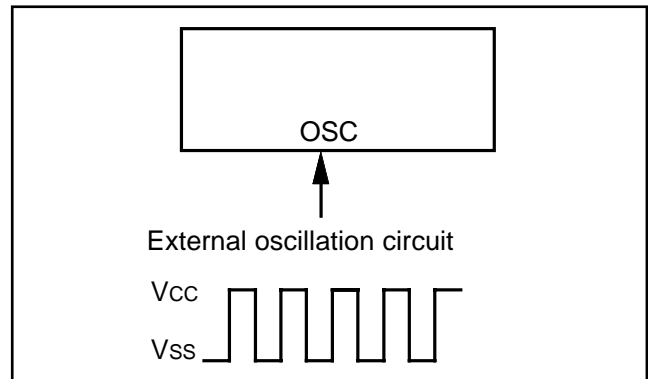


Fig.11 External clock input circuit

HANDLING OF UNUSED PINS

Handle unused pins as the follow.

Table 2 Handling of unused pins

Pin	Handling
Segment	Open
Digit	Open
Analog input	Connect to Vcc or Vss through a resistor.

POWER-ON RESET

Reset can be performed automatically during power on (power-on reset) by the built-in power-on reset circuit.

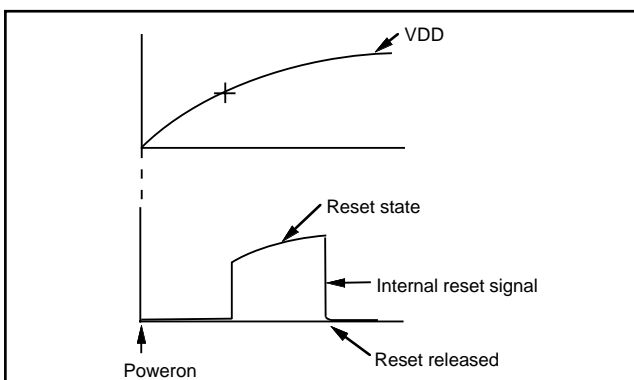


Fig.12 Power-on reset

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage	<ul style="list-style-type: none"> All voltage are based on Vss. Output transistors are cut off. 	-0.3 to 6.5	V
VEE	Pull-down power source voltage		VCC-45 to VCC+0.3	V
Vi	Input voltage AN0 – AN3		-0.3 to VCC+0.3	V
Vi	Input voltage CS, SDATA, SCLK		-0.3 to VCC+0.3	V
Vo	Output voltage FLD0 – FLD24		VCC-45 to VCC+0.3	V
		<ul style="list-style-type: none"> A waveform: 450 μs or more frequency and 30 μs or less pulse width. Connect only capacitor load (CL = 200pF). 	VCC-50 to VCC+0.3	
Vo	Output voltage SDATA	<ul style="list-style-type: none"> All voltage are based on Vss. Output transistors are cut off. 	-0.3 to VCC+0.3	V
Pd	Power dissipation	Ta = 25 °C	600	mW
Topr	Operating temperature		-20 to 85	°C
Tstg	Storage temperature		-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (VCC = 4.0 to 5.5 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VCC	Power source voltage	4.0	5.0	5.5	V
VSS	Power source voltage		0		V
VEE	Pull-down power source voltage	VCC-38		VCC	V
VIH	"H" input voltage CS, SCLK, SDATA	0.75VCC		VCC	V
VIL	"L" input voltage CS, SCLK, SDATA	0		0.25VCC	V

RECOMMENDED OPERATING CONDITIONS (VCC = 4.0 to 5.5 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ΣIOH(peak)	"H" total peak output current FLD0 – FLD24 (Note 1)			-240	mA
ΣIOH(avg)	"H" total average output current FLD0 – FLD24			-120	mA
IOH(peak)	"H" peak output current FLD0 – FLD24 (at DIG selecting) (Note 2)			-40	mA
IOH(peak)	"H" peak output current FLD0 – FLD24 (at SEG selecting) (Note 2)			-20	mA
IOL(peak)	"L" peak output current SDATA			10	mA
IOH(avg)	"H" peak output current FLD0 – FLD24 (at DIG selecting) (Note 3)			-18	mA
IOH(avg)	"H" average output current FLD0 – FLD24 (at SEG selecting) (Note 3)			-7	mA
IOL(avg)	"L" average output current SDATA			5.0	mA
f(OSC)	Clock input oscillation frequency (Note 4)	1.4	2.0	2.6	MHz
f(SCLK)	Serial I/O external clock frequency		250		kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

4: When the oscillation frequency has a 50 % duty cycle.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
VOH	"H" output voltage	DIG output	$I_{OH} = -18$ mA	$V_{CC}-2.0$			V
		SEG output	$I_{OH} = -7$ mA	$V_{CC}-2.0$			V
VOL	"L" output voltage	SDATA	$I_{OL} = 5$ mA			2.0	V
VT+ — VT-	Hysteresis	SDATA, SCLK, CS	$V_{CC} = 5.0$ V		0.5		V
I _{IH}	"H" input current	SDATA, SCLK, CS	$V_I = V_{CC}$			5.0	μA
I _{IL}	"L" input current	SDATA, SCLK	$V_I = V_{SS}$			-5.0	μA
		CS			-500		μA
		OSC			-4.0		μA
I _{LOAD}	Output load current	FLD ₀ – FLD ₂₄	$V_{EE} = V_{CC}-36$ V $V_{OL} = V_{CC}$ Output transistors "off"	250	500	750	μA
I _{LEAK}	Output leakage current	FLD ₀ – FLD ₂₄	$V_{EE} = V_{CC}-38$ V $V_{OL} = V_{CC}-38$ V Output transistors "off"			-10	μA

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
VRAM	RAM hold voltage		When clock is stopped	2.0		5.5	V
I _{CC}	Power source current		$V_{CC} = 5$ V, $f(X_{IN}) = 2.0$ MHz Output transistors "off" at A-D converter operating		1.5	2.5	mA

A-D CONVERTER CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy (excluding quantization error)		$V_{CC} = 5.12$ V			±3	LSB
T _{conv}	Conversion time					100	t _c (OSC)
V _{IA}	Analog input voltage			0		V_{CC}	V
I _{IA}	Analog port input current				0.5	5.0	μA
RLADDER	Ladder resistor				35		kΩ

TIMING REQUIREMENTS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_c(\text{OSC})$	Reset input "L" pulse width	384			ns
$t_{wH}(\text{OSC})$	Clock input "H" pulse width	120			ns
$t_{wL}(\text{OSC})$	Clock input "L" pulse width	120			ns
$t_c(\text{SCLK})$	Serial clock input cycle time (Note)	5			CLKs
$t_{wH}(\text{SCLK})$	Serial clock input "H" pulse width (Note)	2			CLKs
$t_{wL}(\text{SCLK})$	Serial clock input "L" pulse width (Note)	3			CLKs
$t_{su}(\text{SDATA-SCLK})$	Serial input setup time (Note)	2			CLKs
$t_h(\text{SCLK-SDATA})$	Serial input hold time (Note)	3			CLKs
$t_{su}(\text{CS})$	Serial input setup time	50 $t_c(\text{OSC})$			ns
$t_h(\text{CS})$	Serial input hold time	50 $t_c(\text{OSC})$			ns
$t_{re}(\text{SCLK})$	Serial clock interval time	50 $t_c(\text{OSC})$			ns

Note: The unit means a number of noise filter sampling clock ($t_c(\text{OSC})$).

SWITCHING CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_d(\text{SCLK-SOUT})$	Serial I/O output delay time (Note 1)				3	CLKs
$t_v(\text{SCLK-SOUT})$	Serial I/O output valid time		0			ns
$t_r(\text{Pch})$	High-breakdown-voltage P-channel open-drain output rising time	$C_L = 100\text{pF}$ $V_{EE} = V_{CC} - 36\text{ V}$		1.8		μs
COSC	External capacitor size (Note 2)			18	80	pF

Note 1: The unit means a number of noise filter sampling clock ($t_c(\text{OSC})$).

2: An external capacitor size varies with a mounted condition.

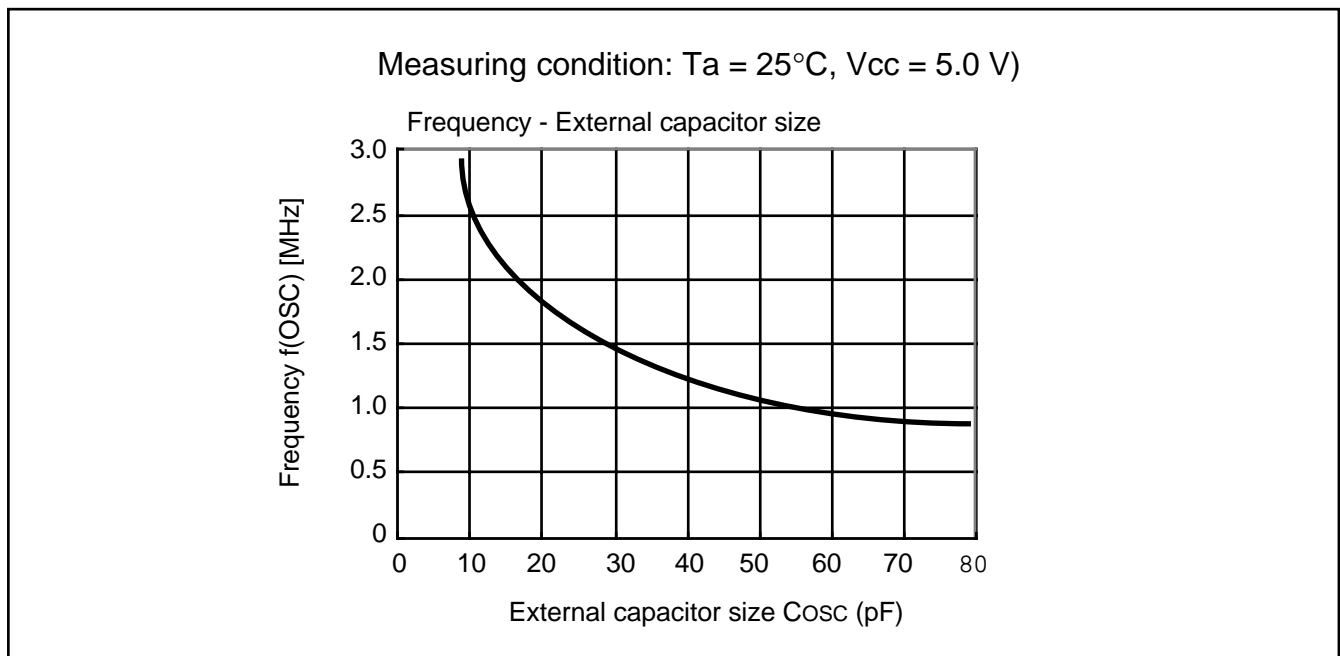


Fig. 13 Standard characteristic example of $f(\text{OSC})$ - C_{osc}

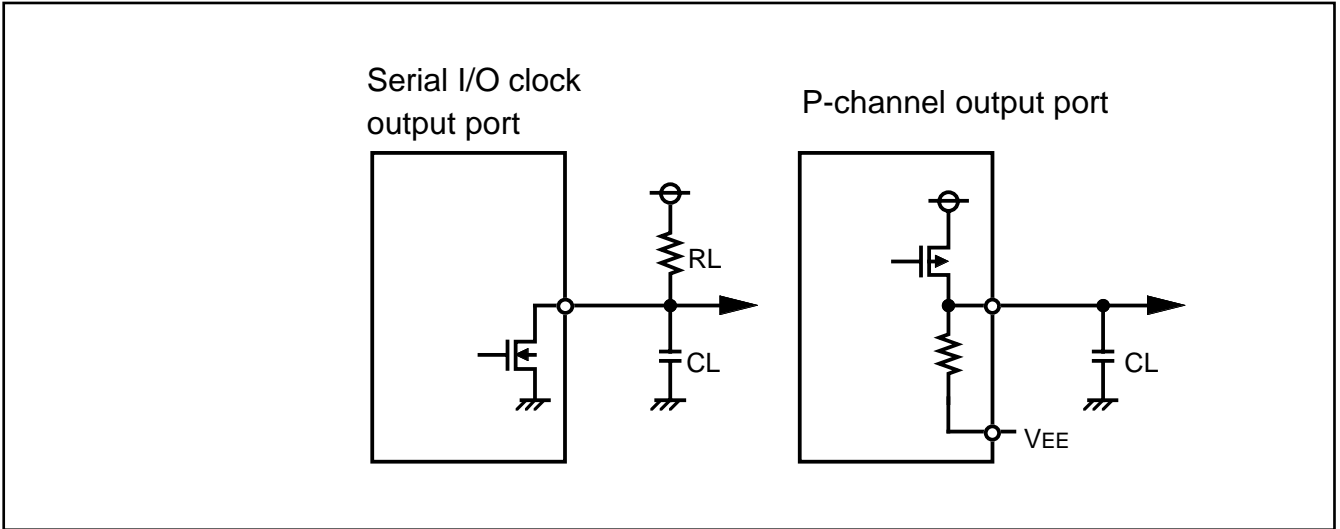


Fig.14 Output switching characteristics measurement circuit diagram

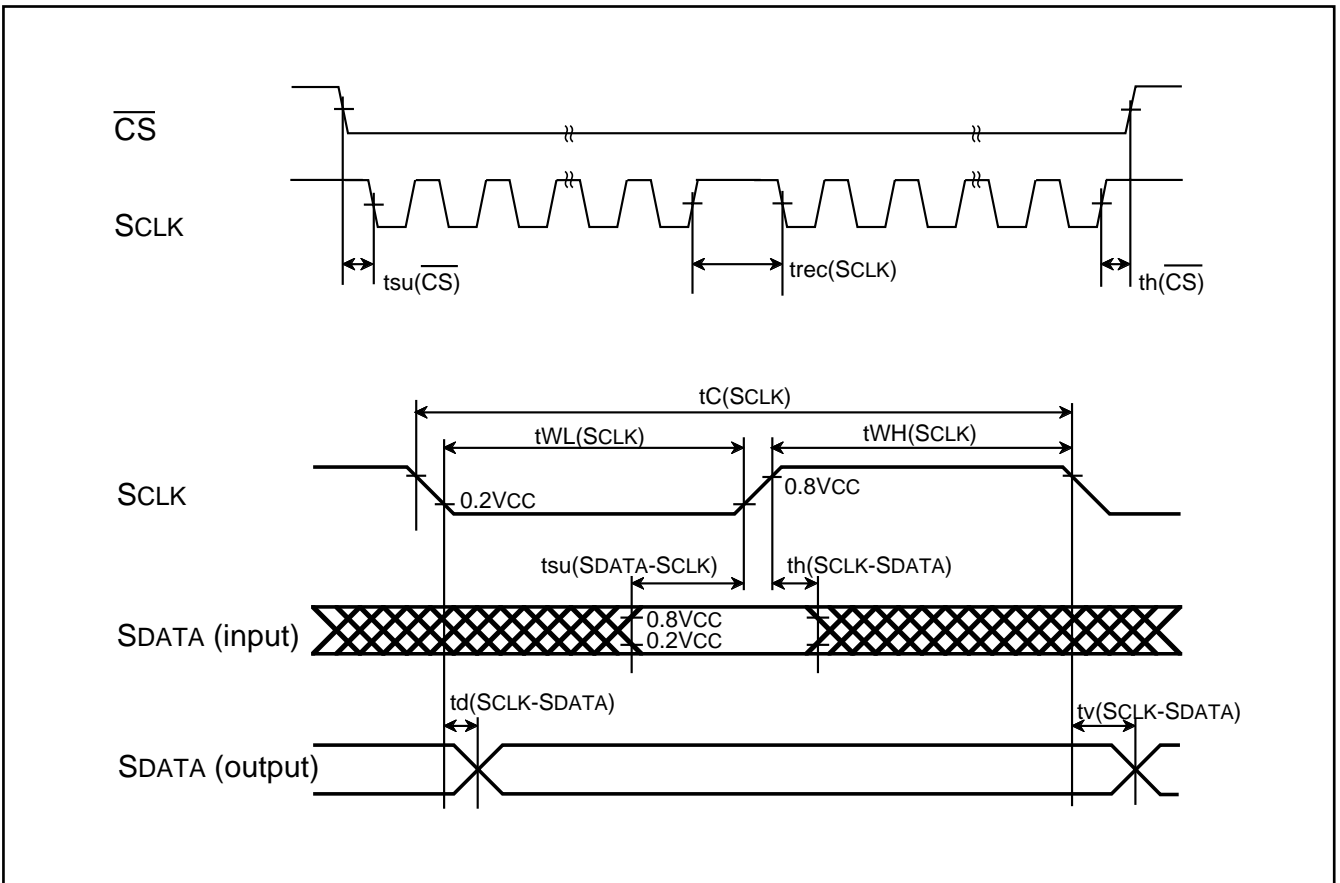


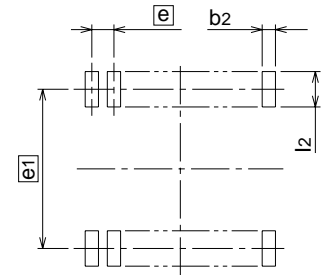
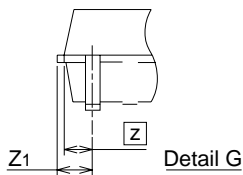
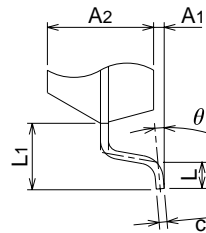
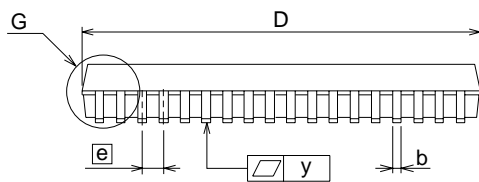
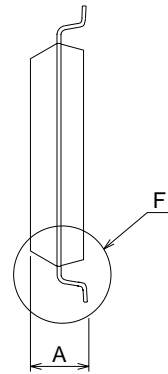
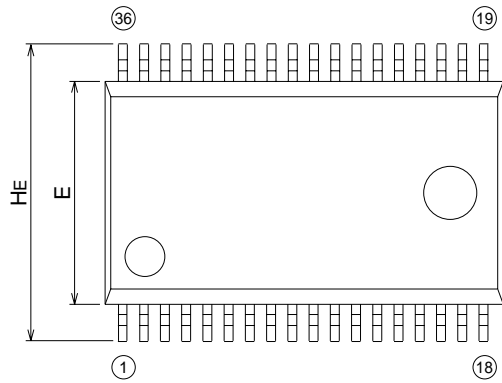
Fig.15 Timing diagram

PACKAGE OUTLINE

36P2R-G

Plastic 36pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP36-P-450-0.80	—	0.53	Alloy 42



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.3
A1	0	0.1	0.2
A2	—	2.0	—
b	0.25	0.3	0.4
c	0.10	0.15	0.22
D	14.8	15.0	15.2
E	8.2	8.4	8.6
e	—	0.8	—
HE	10.1	10.4	10.7
L	0.3	0.5	0.7
L1	—	1.0	—
Z	—	0.7	—
Z1	—	—	0.85
y	—	—	0.15
θ	0 _i	—	10 _i
b2	—	0.5	—
e1	—	11.43	—
l2	1.27	—	—



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REVISION DESCRIPTION LIST

M35502AFP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	990726
1.1	Font error is revised.	000414