SANYO

1M (128k words × 8bits) Serial Flash EEPROM

Features

CMOS Flash EEPROM Technology
Single 3.3-Volt Read and Write Operations
Sector Erase Capability: 256 Bytes per sector
Operating Frequency: 10MHz
Low Power Consumption
    Active Current (Read): 25 mA (Max.)
    Standby Current: 20 μA (Max.)
Serial Peripheral Interface (S.P.I.) mode 0.

High Read/Write Reliability
    Sector-write Endurance Cycles: 10^4
    10 Years Data Retention
Self-timed Erase and Programming
Byte Programming: 35 μs (Max.)
End of Write Detection: Status Register Read
Hardware Data Protection
Packages Available: MSOP8(225mil)

Product Description

The LE25FV101T is a 128K x 8 CMOS sector erase, byte programmable serial Flash EEPROM. The LE25FV101T is manufactured using SANYO's proprietary, high performance CMOS Flash EEPROM technology. Breakthroughs in EEPROM cell design and process architecture attain better reliability and manufacturability compared with conventional approaches. The LE25FV101T erases and programs with a 3.3-volt only power supply. LE25FV101T conforms to Serial Peripheral Interface (S.P.I.).

Featuring high performance programming, the LE25FV101T typically byte programs in 35 μs. The LE25FV101T typically sector (256 bytes) erases in 4ms. Both program and erase times can be optimized using interface feature such as Status Register to indicate the completion of the write cycle. To protect against an inadvertent write, the LE25FV101T has on chip hardware data protection scheme. Designed, manufactured, and tested for a wide spectrum of applications, the LE25FV101T is offered with a guaranteed sector write endurance of 10^4 cycles. Data retention is rated greater than 10 years.

The LE25FV101T is best suited for applications that require re-programmable nonvolatile mass storage of program or data memory.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the command register through serial input (SI). The addresses and data of Commands are latched to be used to operate functions such as Read, Sector_Erase, Byte_Program and so on.

Fig.3 and Fig.4 contain the timing waveforms of serial input and output. By setting $\overline{CS}$ to LOW, the device is selected. And commands, addresses, and dummy bits can be let in serially through SI port. When the device is in Read or Status Register Read mode, SO pin is in Low-impedance state. And the requested data can be read out from MSB (most significant bit) synchronously with the falling edge of SCK.
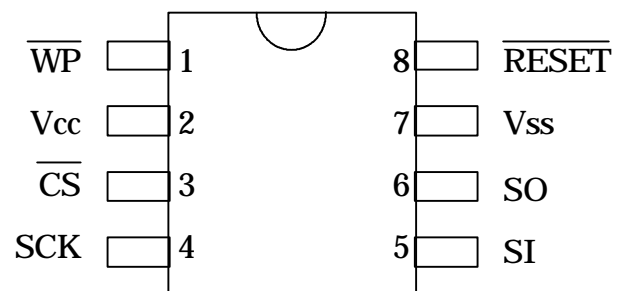

Figure1: Pin Assignment for 8-pin MSOP

LE25FV101T
3.3V-only 1M-Bit Serial Flash EEPROM

Preliminary Specifications
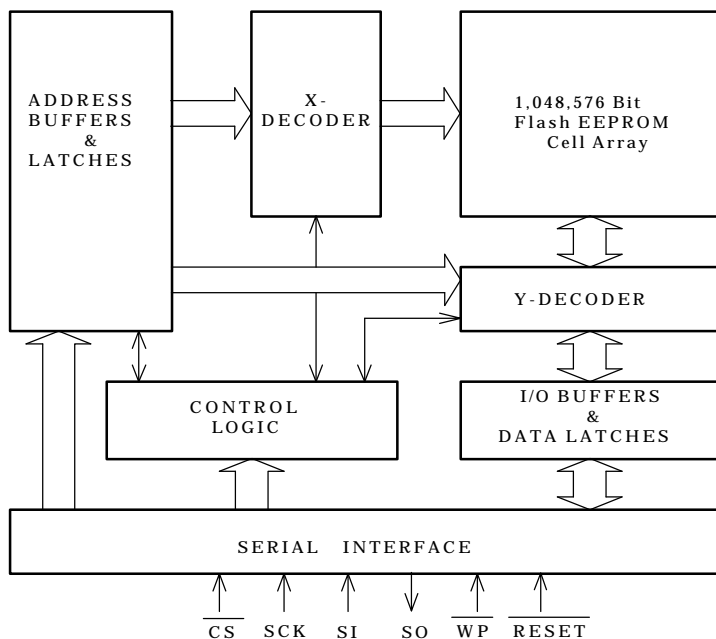
Figure2: Functional Block Diagram of LE25FV101T

Table1: Pin Description

Symbol	Pin Description	Functions
SCK	Serial Clock	To control the timing of serial data input and output. To latch input data and addresses synchronously at the rising edge of SCK, and read out output data synchronously at this falling edge.
SI	Serial Input	To input data or addresses serially from MSB to LSB (Least Significant Bit).
SO	Serial Output	To output data serially from MSB to LSB.
$\overline{CS}$	Chip Select	To activate the device when this pin is LOW. To deselect and put the device to standby mode when High.
$\overline{WP}$	Write Protect	To prevent inadvertent write when this pin is LOW. As $\overline{WP}$ is connected internally to the Vcc, leave this pin open when this function is not necessary.
Vcc	Power Supply	To provide 3.0V to 3.6V supply.
Vss	Ground	
$\overline{RESET}$	Reset	To prevent inadvertent writes by setting this pin to LOW during system power-up. As $\overline{RESET}$ is connected to Vcc internally, leave this pin open when this function is not necessary.

Table2: Commands Summary

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle
	OPcode	Address	Address	Address	Data / OPcode	Dummy
Read	FFH	A23-A16	A15-A8	A7-A0	X	X
Sector Erase	20H	A23-A16	A15-A8	X	D0H	X
Byte Program	10H	A23-A16	A15-A8	A7-A0	PD	X
Status Register	9FH					
Reset	FFH					

Definition for table 2:

1. X= don't care, H= number in hex.
2. A17-A23=don't care
3. PD= Program data
4. Reset Command is effective when the device is only in Erase or Program sequence (in tBP or tSE period).

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Command Definition

Table 2 contains a command list and a brief summary of the commands. The following is a detailed description of the options initiated by each command.

Read

Fig.5 shows the timing waveform of read operation. The read operation is initiated by READ command. After writing OPcode of "FFH" and following 24bit address and 16 dummy bits, SO is transformed into Low-impedance state, and the specified addresses' data are read out synchronously with SCK clock. While the SCK clock is continuously on, the device counts up the next address automatically and reads the data in order. When the address reaches its maximum, while the read operation still be continuing, the address is reset to the lowest one, and the device continues reading data from the beginning.

When $\overline{CS}$ is set High so as to deselect the device, the read operation terminates with the output in High-impedance state. Do not execute read operation while the device is in Byte_Program or Sector_Erase Cycle to prevent inadvertent writes.

Status_Register Read

Fig.6 shows the timing waveform of Status_Register Read.
Status_Register can be read while the device is in Program or Erase mode. As is shown in the table below, the LSB (Least Significant Bit) of Status_Register is set to $\overline{BSY}$ with other bits intact. By setting $\overline{CS}$ to LOW and writing "9FH" in command register, the contents of the Status_Register come out from MSB. The LSB of the Status_Register stands for if the device is busy or not. Therefore,"0" stands for busy and "1" for not in Program or Erase mode. When $\overline{CS}$ goes High, Status Register reading terminates with the output pin in High-impedance state.

7(MSB)	6	5	4	3	2	1	0(LSB)
X	X	X	X	X	X	X	$\overline{BSY}$

Sector_Erase

Fig.7 shows the timing waveform of Sector_Erase. Sector_Erase command consists of 6 bus cycles from 1st bus cycle to 6th bus cycle. This command stages the device for electrical erasing of all bytes within a sector. A sector contains 256 bytes. This sector erasability enhances the flexibility and usefulness of the LE25FV101T, since most applications only need to change a small number of bytes or sectors, not the entire chip. To execute the Sector_Erase operation, erase address, 2nd OPcode (D0H) and Dummy bits must be written to the command register after writing 1st OPcode of (20H). This two-step sequence ensures that only

memory contents within the addressed sector are erased and other sectors are not inadvertently erased. The erase operation begins with the rising edge of the $\overline{CS}$ pulse and terminates automatically by using an internal timer. Termination of this mode is found out by using Status Register Read.

Byte_Program

Fig.8 shows the timing waveform of Byte_Program. Byte_Program command consists of 6 bus cycles from 1st bus cycle to 6th bus cycle, and stages the device for Byte programmable. To execute the Byte_Program operation, program address, program data and Dummy bits must be written to the command register after writing the OPcode of (10H). The program operation begins with the rising edge of the $\overline{CS}$ pulse and terminates automatically by using an internal timer. Termination of this mode is found out by using Status Register Read.

Reset

Fig.9 shows the timing waveform of Reset operation. Reset operation is effective while the device is already in Program or Erase mode. But the data of specified address are not guaranteed. The Reset Command can be provided as a means to safely abort the Erase or Program Command sequences. Following 4th bus cycles (erase or program) with a write of (FFH) in 5th bus cycle will safely abort the operation. Memory contents will not be altered.

Hardware Write Protection

Setting $\overline{WP}$ to LOW prevents inadvertent writes by inhibiting write operation. As $\overline{WP}$ is connected internally to the Vcc, don't connect externally to any nodes when this function is not necessary. To prevent inadvertent writes during system power-up, LE25FV101T has power-on-reset circuit.

To perform power up more safely, the usage of $\overline{RESET}$ is recommended as follows. By holding $\overline{RESET}$ LOW during system power up and setting to High after Vcc reaches operation voltage, inadvertent writes can be prevented (see Fig.10). Don't use this function except during power up. As $\overline{RESET}$ is connected to Vcc internally, don't connect externally to any nodes when this function is not necessary.

Decoupling Capacitors

Ceramic capacitors (0.1 µF) must be added between V_{CC} and V_{SS} to each device to assure stable flash memory operation.

Absolute Maximum Stress Ratings

Storage Temperature ....-55 °C ~ 150 °C
Supply Voltage ....-0.5 V ~ 4.6 V
D.C. Voltage on Any Pin to Grand Potential ....-0.5 V ~ Vcc + 0.5 V

<div align="center">Permanent device damage may occur if ABSOLTE MAXIMUM RATINGS are exceeded.</div>

Operating Range

Ambient Temperature..0 °C ~ 70 °C
Vcc..3.0 V ~ 3.6 V

DC Operating Characteristics

Symbol	Parameter	Limit Min.	Limit Max.	unit	Test Condition
ICCR	Power Supply Current (Read)		10	mA	$\overline{CS}$ = VIL SO, $\overline{WP}$ open SI = VIL / VIH, f = 10MHz, VCC = VCC max.
ICCW	Power Supply Current (Write)		45	mA	VCC = VCC max.
ISB1	Standby Vcc Current (TTL input)		3	mA	$\overline{CS}$ = VIH SO, $\overline{WP}$, $\overline{RESET}$ open VCC = VCC max.
ISB2	Standby Vcc Current (CMOS input)		20	μA	$\overline{CS}$ = VCC–0.3V SO, $\overline{WP}$, $\overline{RESET}$ open VCC = VCC max.
ILI	Input Leakage Current		10	μA	VIN = VSS ~ VCC, VCC = VCC max.
ILO	Output Leakage Current		10	μA	VIN = VSS ~ VCC, VCC = VCC max.
VIL	Input Low Voltage	–0.3	0.4	V	VCC = VCC max.
VIH	Input High Voltage	2.4	Vcc+0.3	V	VCC = VCC min.
VOL	Output Low Voltage		0.2	V	IOL = 100 μA, VCC = VCC min.
VOH	Output High Voltage	Vcc-0.2		V	IOH = –100 μA, VCC = VCC min.

Power-up Timing

Symbol	Parameter	Minimum	Units
tPU_READ	Power-up to Read Operation(without using $\overline{RESET}$)	10	ms
tPU_WRITE	Power-up to Write Operation(without using $\overline{RESET}$)	10	ms
tPU_RST	From $\overline{RESET}$ goes High to Command Entry	1	μs

Capacitance (Ta = 25 °C, f = 1 MHz)

Symbol	Description	Maximum	Unit	Test Condition
CDQ	DQ Pin Capacitance	12	pF	VDQ = 0V
CIN	Input Capacitance	6	pF	VIN = 0V

Note: These parameters are periodically sampled and are not 100% tested.

AC Characteristics

Symbol	Parameter	Limit		unit
		Min.	Max.	
fCLK	Clock Frequency		10	MHz
tCSS	$\overline{CS}$ setup time	400		ns
tCSH	$\overline{CS}$ hold time	400		ns
tCPH	$\overline{CS}$ standby pulse width	250		ns
tCHZ	$\overline{CS}$ to Hi-Z output		250	ns
tDS	Data Setup time	30		ns
tDH	Data hold time	30		ns
tCLH	SCK High pulse width	45		ns
tCLL	SCK Low pulse width	45		ns
tCLZ	SCK to Lo-Z output	0		ns
tV	SCK to output valid		40	ns
tHO	Output data hold time	0		ns
tSE	Sector Erase Cycle Time		4	ms
tBP	Byte Program Cycle time		35	µs
tRST	Write Reset Recovery Time		4	µs

AC Test Conditions

Input Pulse Level.. 0 V ~ 3.0 V
Input Rise/Fall Time.. 5 ns
Input/Output Timing Level 1.5V
Input Load Levels.. 30 pF

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Figure 3: Serial Input Timing Diagram
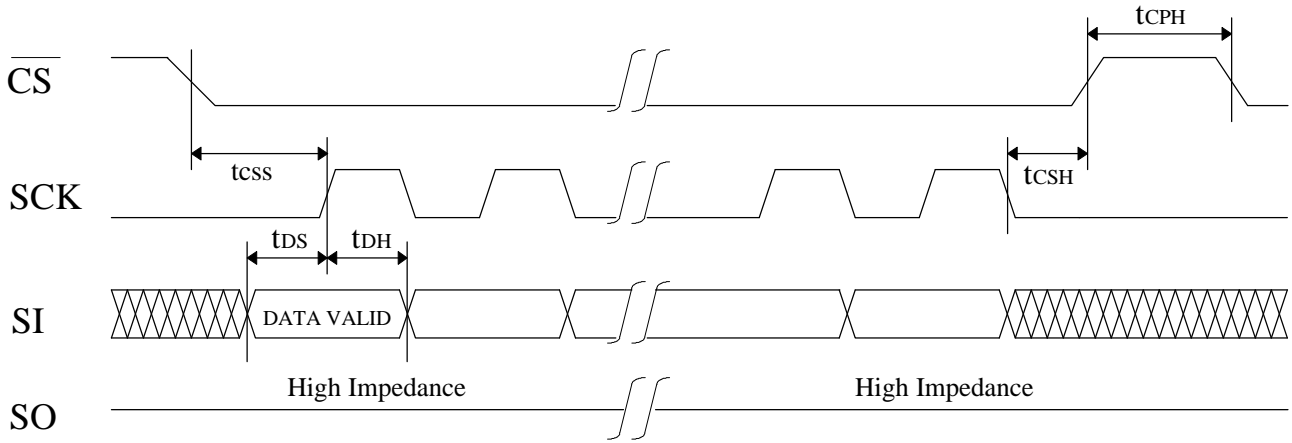
Figure 4: Serial Output Timing Diagram
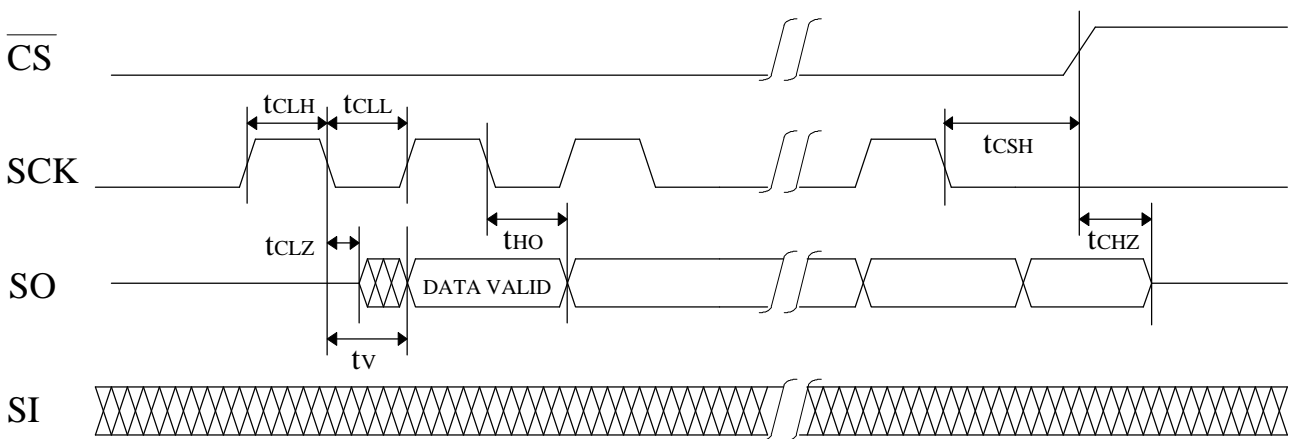
Figure 5: Read Cycle Timing Diagram
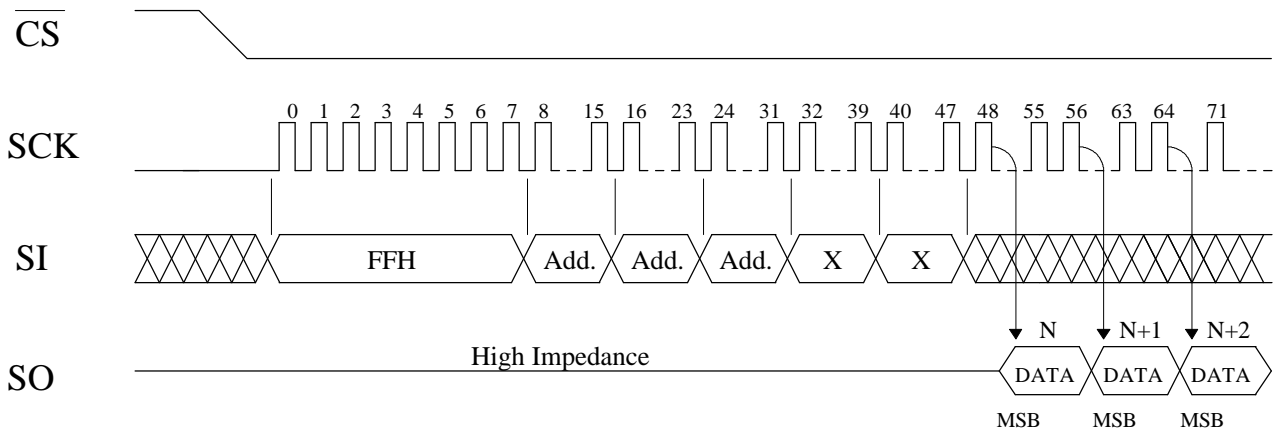
Figure 6: Status Register Read Timing Diagram
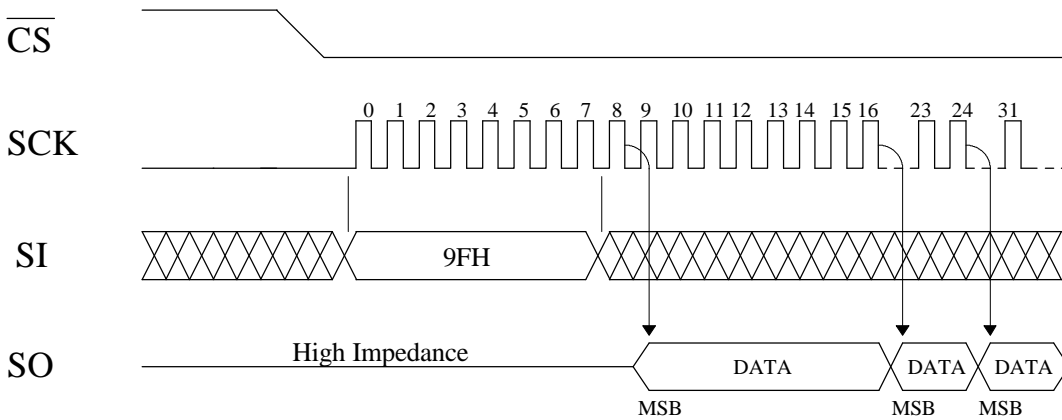
Figure 7: Sector_Erase Timing Diagram
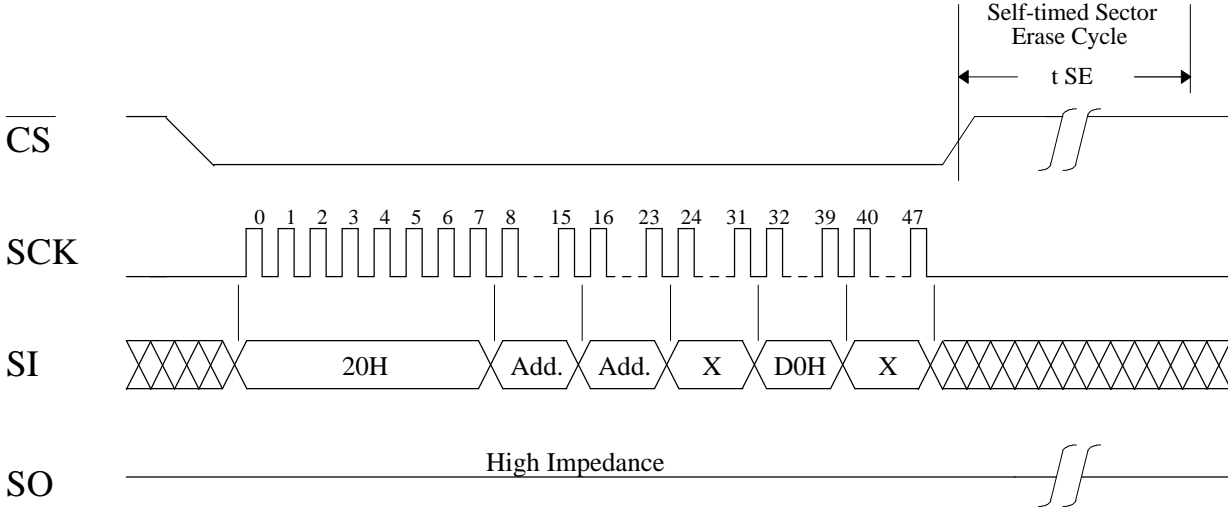

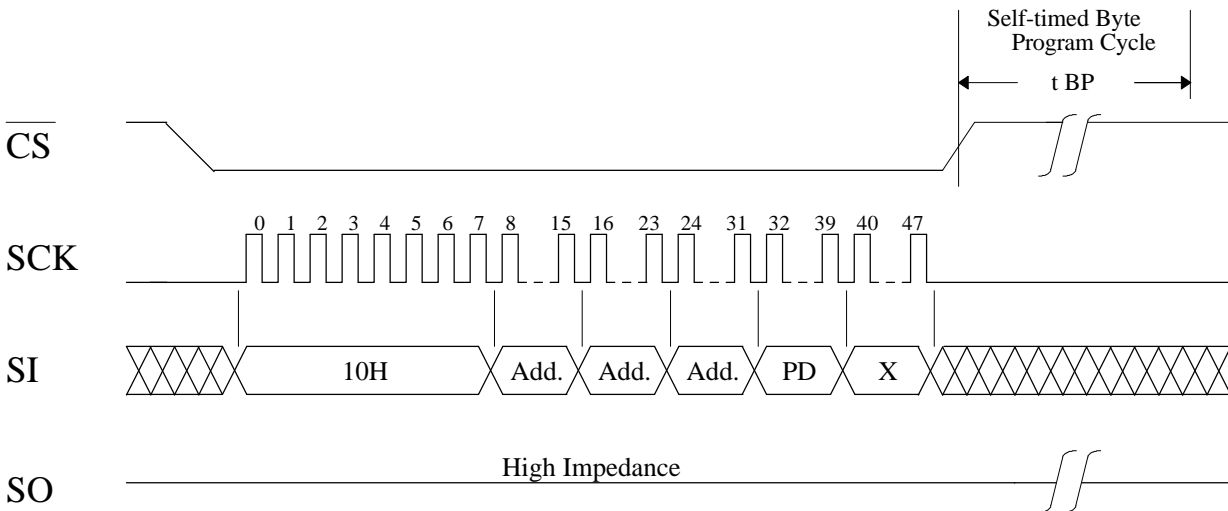**Figure 8: Byte_Program Timing Diagram**

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Figure 9: Reset Timing Diagram

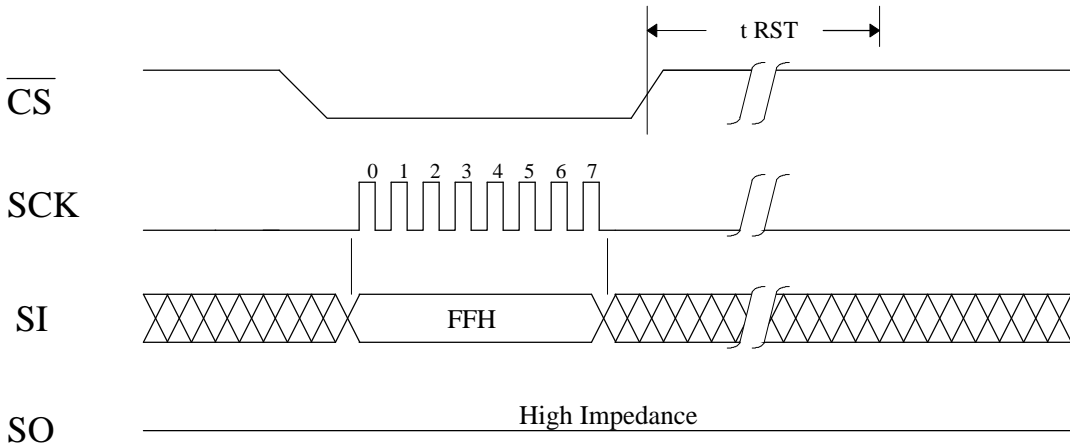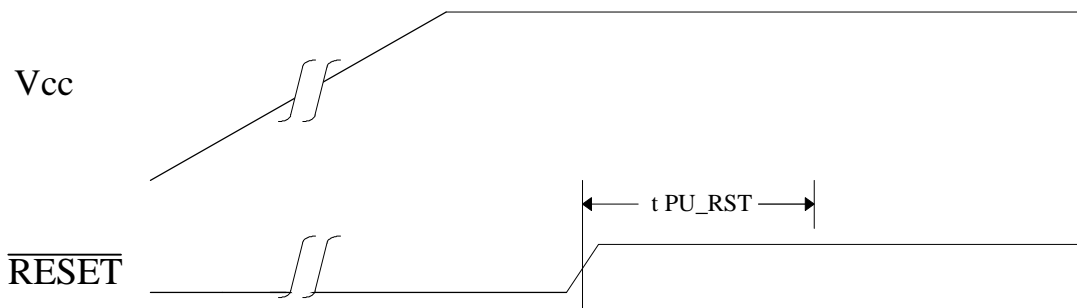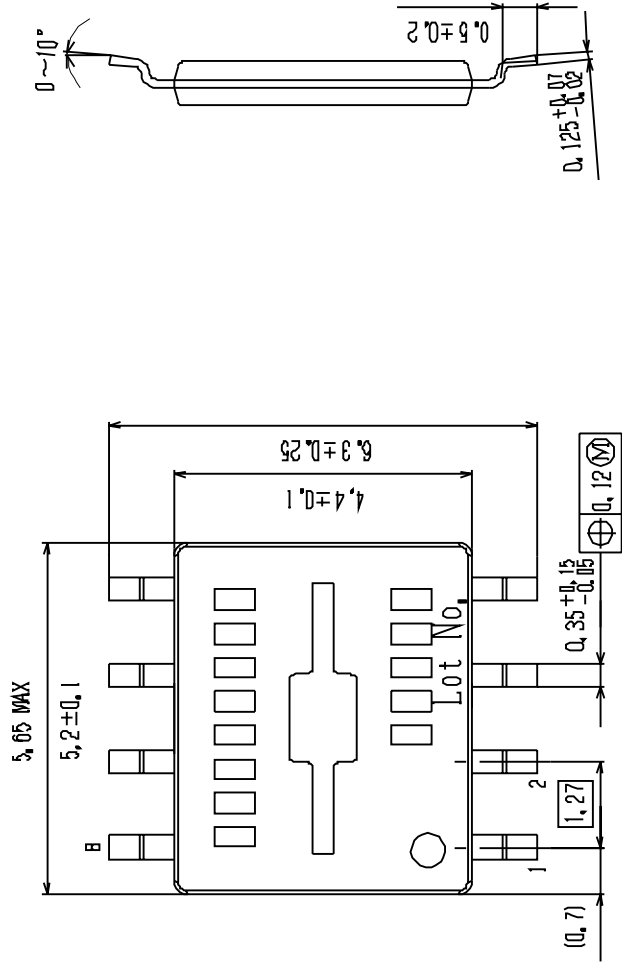Reset Command is effective when the device is only in Erase or Program sequence (in tBP or tSE period).

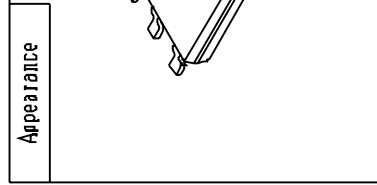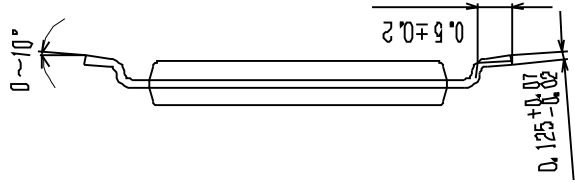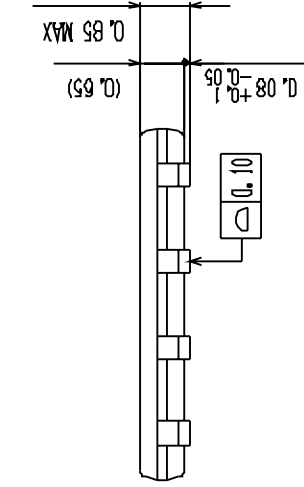**Figure 10: Command Entry Recover Timing from $\overline{RESET}$ goes High**

OUTLINE DRAWING

SANYO Package Code	E(A)J Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Weight(g)
MSOP8(225mil)X01	—	—	—	S-000	—

TENTATIVE

Appearance

MSOP8(225mil)X01

SANYO : Micro Small Outline Package 8Pin Plastic

0 ~ 10°

0.6±0.2

0.125+0.07/-0.02

6.3±0.25

4.4±0.1

5.2±0.1

5.65 MAX

B

0.35+0.15/-0.05

⊕ 0.12 Ⓜ

Lot No.

1.27

(0.7)

1 2

0.85 MAX

(0.65)

0.08+0.1/-0.05

□ 0.10

REVISION : 1