Integrated Circuit Systems, Inc.

ICS844002I-01
FemtoClocks™ Crystal-to-LVDS Frequency Synthesizer

General Description

The ICS844002I-01 is a 2 output LVDS Synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 156.25MHz, 125MHz and 62.5MHz. The ICS844002I-01 uses ICS' 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS844002I-01 is packaged in a small 20-pin TSSOP package.

Features

- Two LVDS outputs

- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input

- Supports the following output frequencies: 156.25MHz, 125MHz, 62.5MHz

- VCO range: 560MHz - 680MHz

- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.41ps (typical)

- Full 2.5V supply mode

- -40°C to 85°C ambient operating temperature

- Available in both, standard and RoHS/Lead-Free compliant packages

Frequency Select Function Table

F_SEL1	F_SEL0	M Divider Value	N Divider Value	Output Frequency (MHz) (25MHz Reference)
0	0	25	4	156.25
0	1	25	5	125
1	0	25	10	62.5
1	1	Not Used		Not Used

Pin Assignment

nc	1	20	V_DDO
V_DDO	2	19	Q1
Q0	3	18	nQ1
nQ0	4	17	GND
MR	5	16	V_DD
nPLL_SEL	6	15	nXTAL_SEL
nc	7	14	REF_CLK
V_DDA	8	13	XTAL_IN
F_SEL0	9	12	XTAL_OUT
V_DD	10	11	F_SEL1

ICS844002I-01
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm package body
G Package
Top View

Block Diagram

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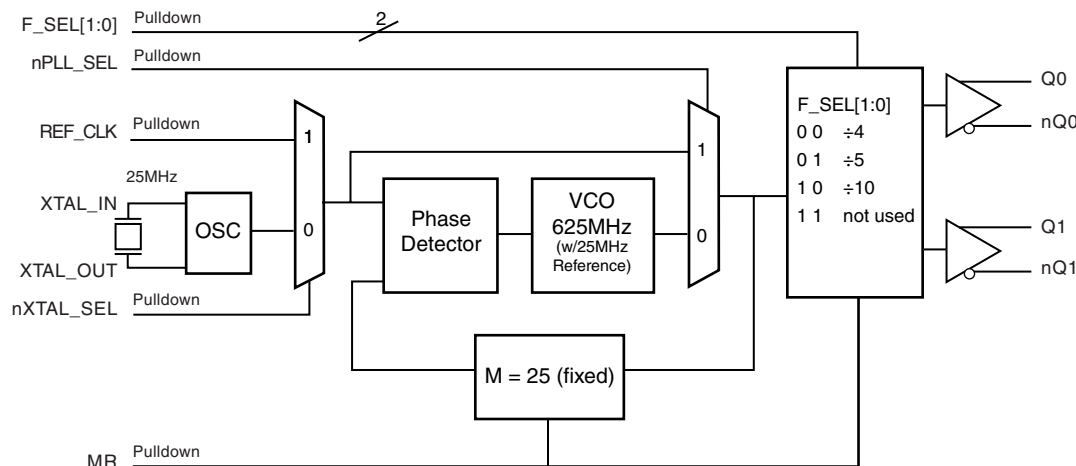
TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 7	nc	Unused		No connect.
2, 20	V$_{DDO}$	Power		Output supply pins.
3, 4	Q0, nQ0	Ouput		Differential output pair. LVDS interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	nPLL_SEL	Input	Pulldown	Selects between the PLL and REF_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8	V$_{DDA}$	Power		Analog supply pin.
9, 11	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
10, 16	V$_{DD}$	Power		Core supply pin.
12, 13	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
14	REF_CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
15	nXTAL_SEL	Input	Pulldown	Selects between crystal or REF_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels.
17	GND	Power		Power supply ground.
18, 19	nQ1, Q1	Output		Differential output pair. LVDS interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C$_{IN}$	Input Capacitance			4		pF
R$_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} 4.6V

Inputs, V_I -0.5V to V_{DD} + 0.5V

Outputs, I_O
   Continuous Current   10mA
   Surge Current   15mA

Package Thermal Impedance, θ_{JA} 73.2°C/W (0 lfpm)

Storage Temperature, T_{STG} -65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				85	mA
I_{DDA}	Analog Supply Current				9	mA
I_{DDO}	Output Supply Current				70	mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	REF_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL	$V_{DD} = V_{IN}$ = 2.625V			150	µA
I_{IL}	Input Low Current	REF_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA

TABLE 3C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		240		550	mV
ΔV_{OD}	V_{OD} Magnitude Change			40		mV
V_{OS}	Offset Voltage		0.7	1.1	1.5	V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

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TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		22.4	25	27.2	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	140		170	MHz
		F_SEL[1:0] = 01	112		136	MHz
		F_SEL[1:0] = 10	56		68	MHz
$t$sk(o)	Output Skew; NOTE 1, 2			5	20	ps
$t$jit(Ø)	RMS Phase Jitter (Random); NOTE 3	156.25MHz, (1.875MHz - 20MHz)		0.41		ps
		125MHz, (1.875MHz - 20MHz)		0.44		ps
		62.5MHz,(1.875MHz - 20MHz)		0.47		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at V_{DDO}/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
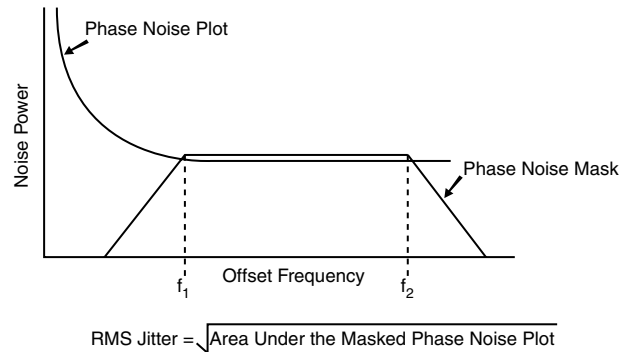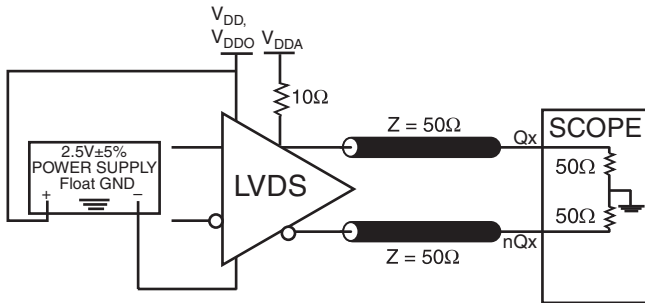NOTE 3: Please refer to the Phase Noise Plot.

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TYPICAL PHASE NOISE AT 156.25MHz

Ethernet Filter

156.25MHz
RMS Phase Jitter (Random)
1.875Mhz to 20MHz = 0.41ps (typical)

Raw Phase Noise Data

Phase Noise Result by adding
Ethernet Filter to raw data

NOISE POWER $\frac{dBc}{Hz}$

OFFSET FREQUENCY (Hz)
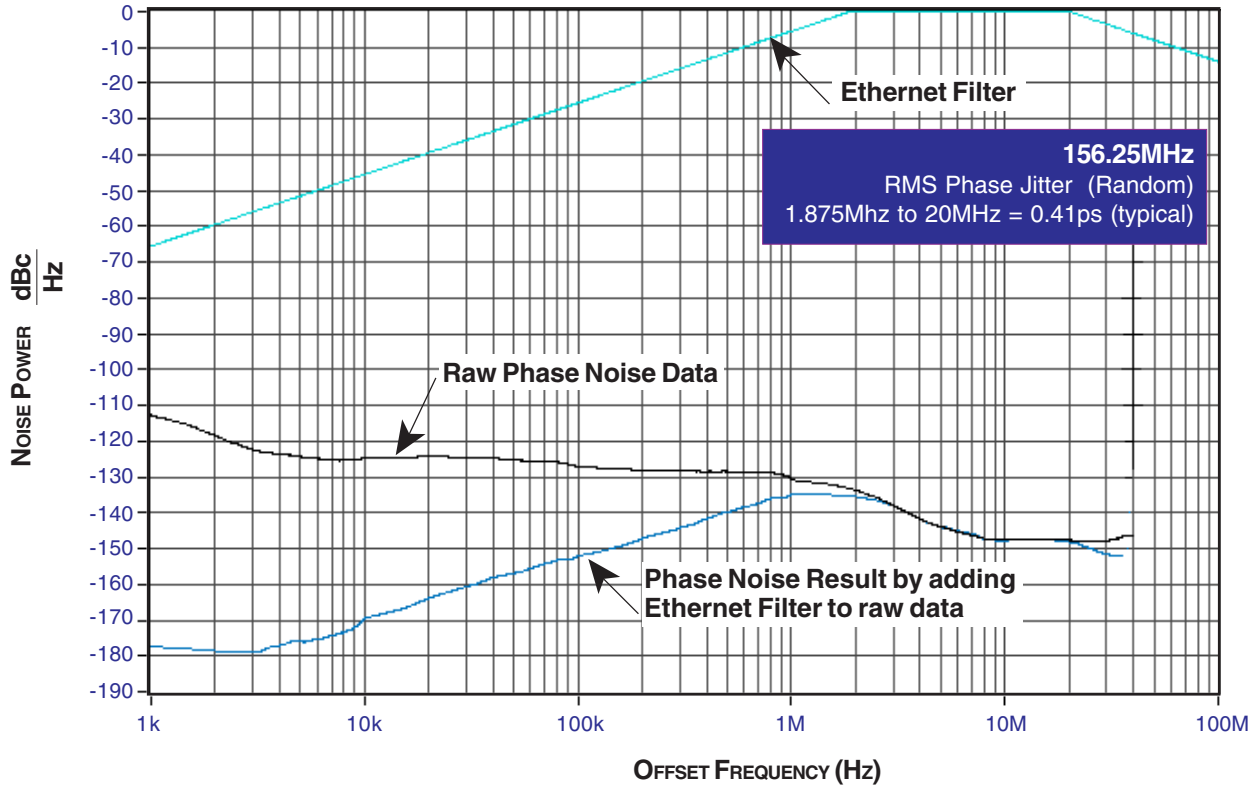
PARAMETER MEASUREMENT INFORMATION

2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT

$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$
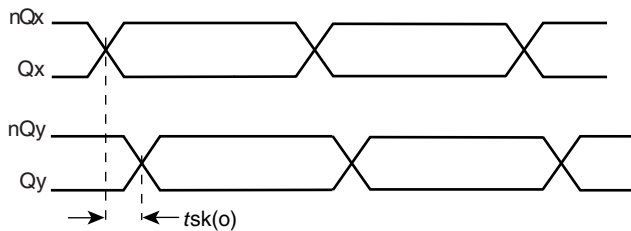
RMS PHASE JITTER

OUTPUT SKEW
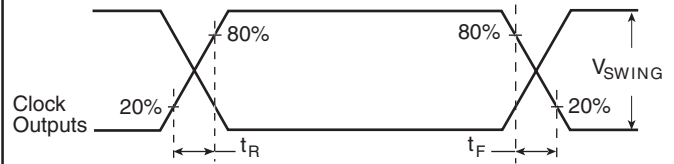
PROPAGATION DELAY
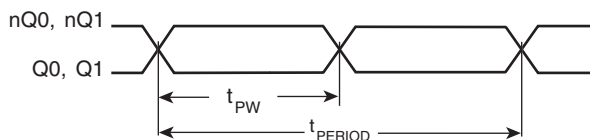
$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD
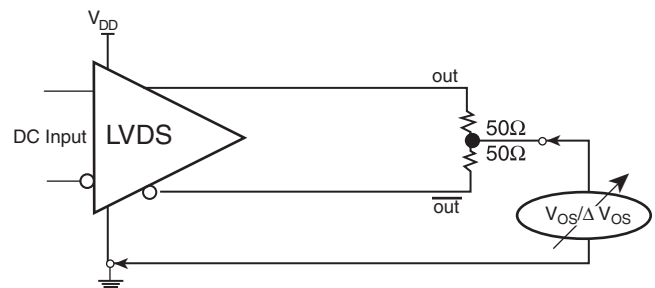
OFFSET VOLTAGE SETUP

DIFFERENTIAL OUTPUT VOLTAGE SETUP

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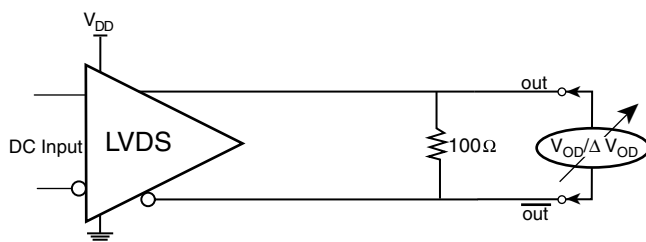
APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844002I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.
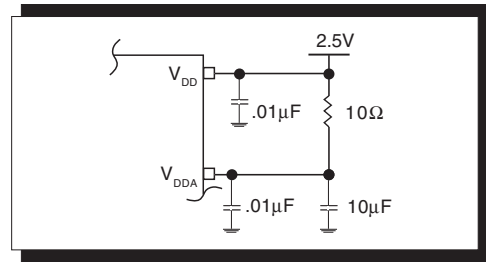
FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844002I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.
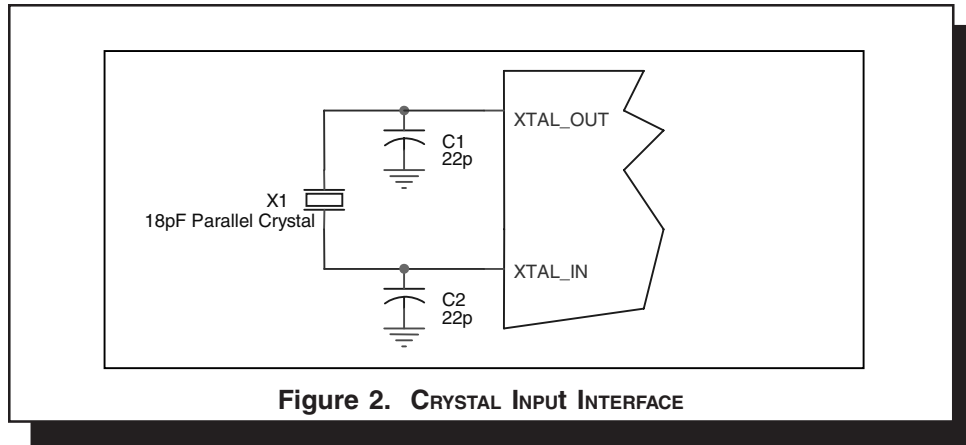

Figure 2. CRYSTAL INPUT INTERFACE

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RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT:

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS

LVDS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

2.5V LVDS DRIVER TERMINATION

Figure 3 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LDVS driver, it is recommended to terminate the unused outputs.
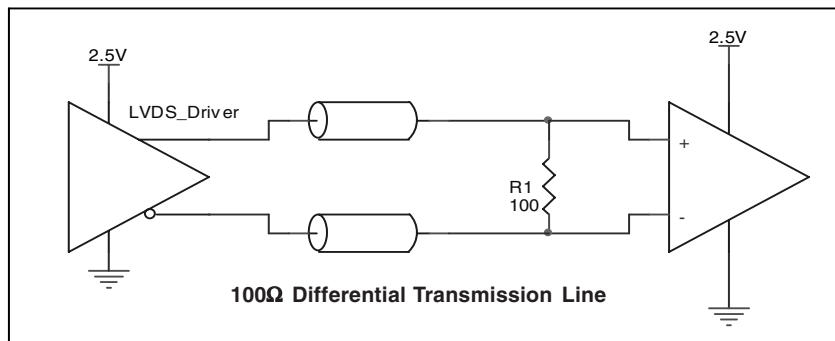

FIGURE 3. TYPICAL LVDS DRIVER TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844002I-01. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS844002I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

· Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.625V * 85mA = **223mW**

· Power (outputs)$_{MAX}$ = **V_{DDO_MAX} * I_{DDO_MAX} = 2.625V * 70mA = 184mW**

Total Power$_{\_MAX}$ = 223mW + 184mW = **407mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

q_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.407W * 66.6°C/W = 112°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

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RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS844002I-01 is: 2914

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP
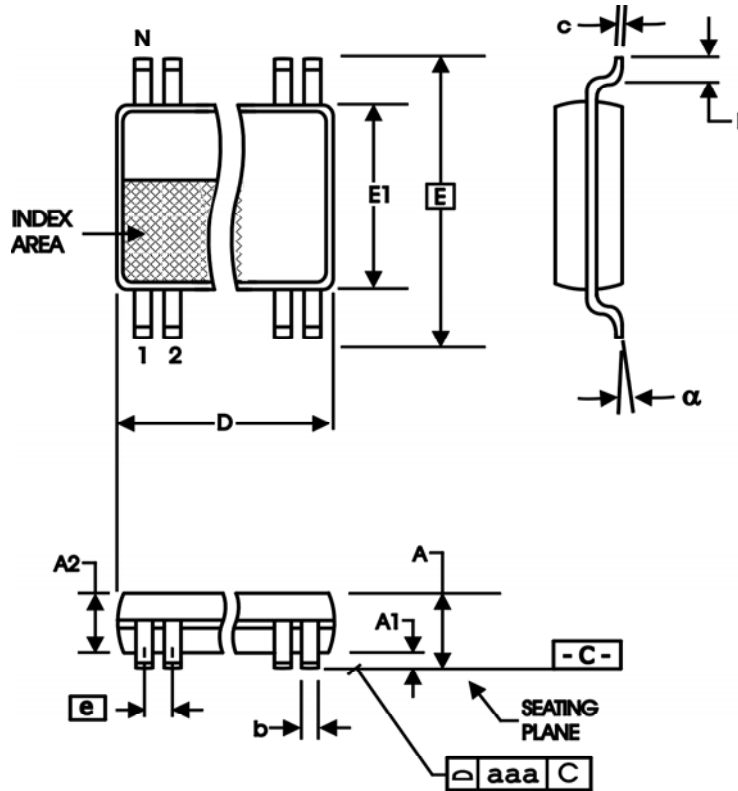
TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

ICS844002I-01

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TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844002AGI-01	ICS44002AI01	20 Lead TSSOP	tube	-40°C to 85°C
ICS844002AGI-01T	ICS44002AI01	20 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS844002AGI-01LF	ICS4002AI01L	20 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS844002AGI-01LFT	ICS4002AI01L	20 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.