

74LVTH125

Low Voltage Quad Buffer with 3-STATE Outputs

General Description

The LVTH125 contains four independent non-inverting buffers with 3-STATE outputs.

These buffers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH125 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 125
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V

Ordering Code:

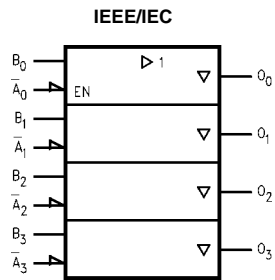
Order Number	Package Number	Package Description
74LVTH125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVTH125SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH125MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

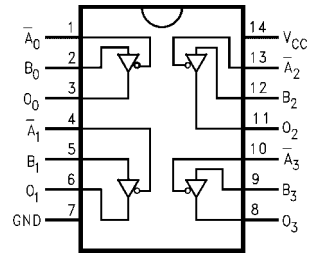
Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

74LVTH125 Low Voltage Quad Buffer with 3-STATE Outputs

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
\bar{A}_n, B_n	Inputs
O_n	3-STATE Outputs

Truth Table

Inputs		Output
\bar{A}_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance

Absolute Maximum Ratings ^(Note 2)				
Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	-0.5 to +4.6		V
V_I	DC Input Voltage	-0.5 to +7.0		V
V_O	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 3)	
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	± 64		mA
I_{GND}	DC Ground Current per Ground Pin	± 128		mA
T_{STG}	Storage Temperature	-65 to +150		$^{\circ}C$
Recommended Operating Conditions				
Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH Level Output Current		-32	mA
I_{OL}	LOW Level Output Current		64	mA
T_A	Free-Air Operating Temperature	-40	85	$^{\circ}C$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$, $V_{CC} = 3.0V$	0	10	ns/V
<p>Note 2: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.</p> <p>Note 3: I_O Absolute Maximum Rating must be observed.</p>				

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C			Units	Conditions	
			Min	Typ (Note 4)	Max			
V _{IK}	Input Clamp Diode Voltage	2.7			-1.2	V	I _I = -18 mA	
V _{IH}	Input HIGH Voltage	2.7–3.6	2.0			V	V _O ≤ 0.1V or	
V _{IL}	Input LOW Voltage	2.7–3.6			0.8	V	V _O ≥ V _{CC} - 0.1V	
V _{OH}	Output HIGH Voltage	2.7–3.6	V _{CC} - 0.2			V	I _{OH} = -100 μA	
		2.7	2.4				I _{OH} = -8 mA	
		3.0	2.0				I _{OH} = -32 mA	
V _{OL}	Output LOW Voltage	2.7			0.2	V	I _{OL} = 100 μA	
		2.7			0.5		I _{OL} = 24 mA	
		3.0			0.4		I _{OL} = 16 mA	
		3.0			0.5		I _{OL} = 32 mA	
		3.0			0.55		I _{OL} = 64 mA	
I _{I(HOLD)}	Bushold Input Minimum Drive	3.0	75			μA	V _I = 0.8V	
			-75				V _I = 2.0V	
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	3.0	500			μA	(Note 5)	
			-500				(Note 6)	
I _I	Input Current	3.6			10	μA	V _I = 5.5V	
		Control Pins	3.6				±1	V _I = 0V or V _{CC}
		Data Pins	3.6				-5	V _I = 0V
					1		V _I = V _{CC}	
I _{OFF}	Power Off Leakage Current	0			±100	μA	0V ≤ V _I or V _O ≤ 5.5V	
I _{PU/PD}	Power up/down 3-STATE Output Current	0–1.5V			±100	μA	V _O = 0.5V to 3.0V V _I = GND or V _{CC}	
I _{OZL}	3-STATE Output Leakage Current	3.6			-5	μA	V _O = 0.5V	
I _{OZH}	3-STATE Output Leakage Current	3.6			5	μA	V _O = 3.0V	
I _{OZH+}	3-STATE Output Leakage Current	3.6			10	μA	V _{CC} < V _O ≤ 5.5V	
I _{CCH}	Power Supply Current	3.6			0.19	mA	Outputs HIGH	
I _{CCL}	Power Supply Current	3.6			5	mA	Outputs LOW	
I _{CCZ}	Power Supply Current	3.6			0.19	mA	Outputs Disabled	
I _{CCZ+}	Power Supply Current	3.6			0.19	mA	V _{CC} ≤ V _O ≤ 5.5V Outputs Disabled	
ΔI _{CC}	Increase in Power Supply Current (Note 7)	3.6			0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND	

Note 4: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8		V	(Note 9)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C C _L = 50 pF, R _L = 500Ω					Units
		V _{CC} = 3.3V ± 0.3V			V _{CC} = 2.7V		
		Min	Typ (Note 10)	Max	Min	Max	
t _{PLH}	Propagation Delay Data to Output	1.0		3.5	1.0	4.5	ns
t _{PHL}		1.0		3.9	1.0	4.9	
t _{PZH}	Output Enable Time	1.0		4.0	1.0	5.5	ns
t _{PZL}		1.1		4.0	1.1	5.4	
t _{PHZ}	Output Disable Time	1.5		4.5	1.5	5.7	ns
t _{PLZ}		1.3		4.5	1.3	4.0	
t _{OSSL}	Output to Output Skew (Note 11)			1.0		1.0	ns
t _{OSLH}							

Note 10: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

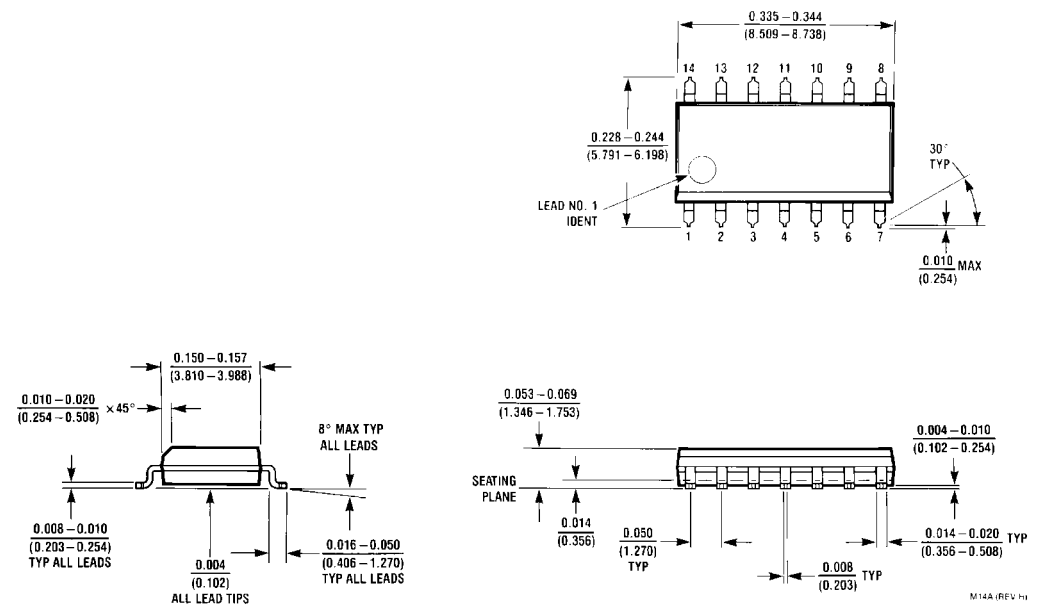
Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 12)

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 0V, V _I = 0V or V _{CC}	4	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	8	pF

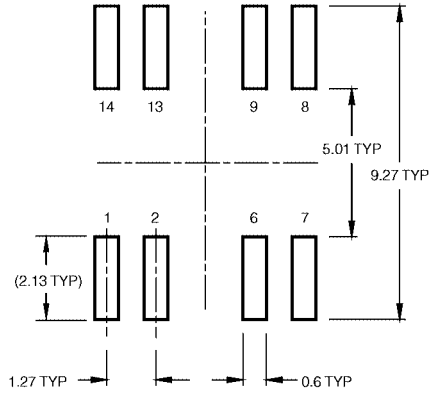
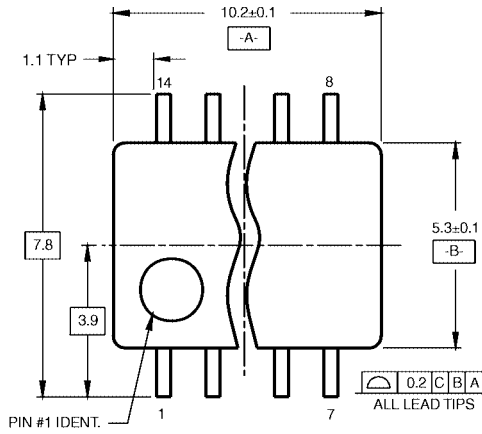
Note 12: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted

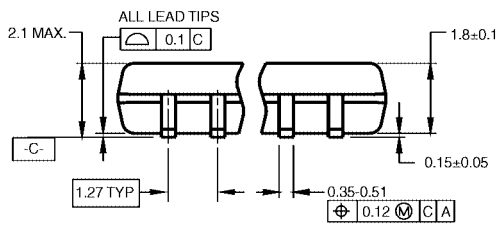


**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

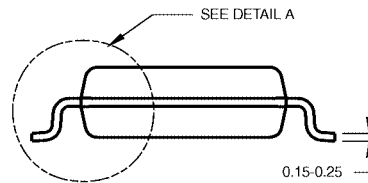
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

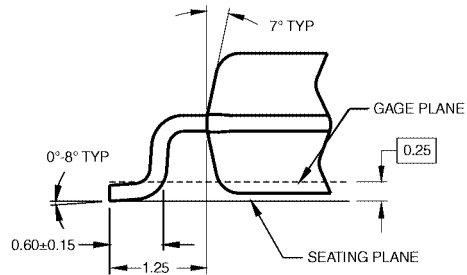


DIMENSIONS ARE IN MILLIMETERS



- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

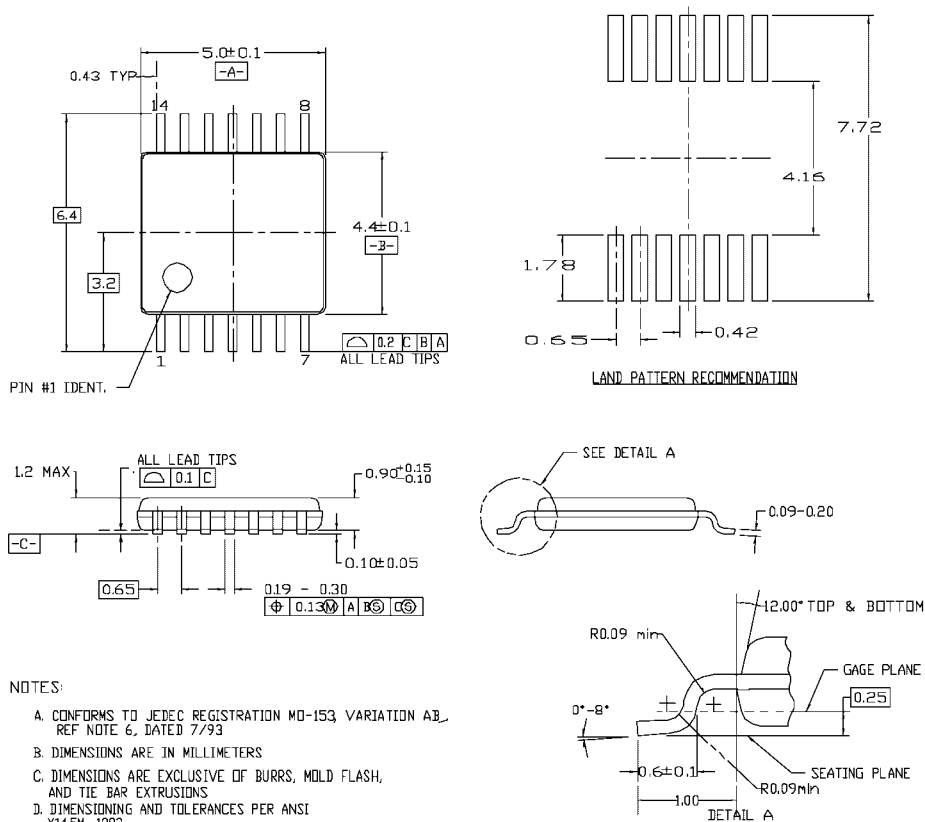
M14DRevB1



DETAIL A

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153 VARIATION AB, REF NOTE 6, DATED 7/93
 - B. DIMENSIONS ARE IN MILLIMETERS
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.