

FEATURES

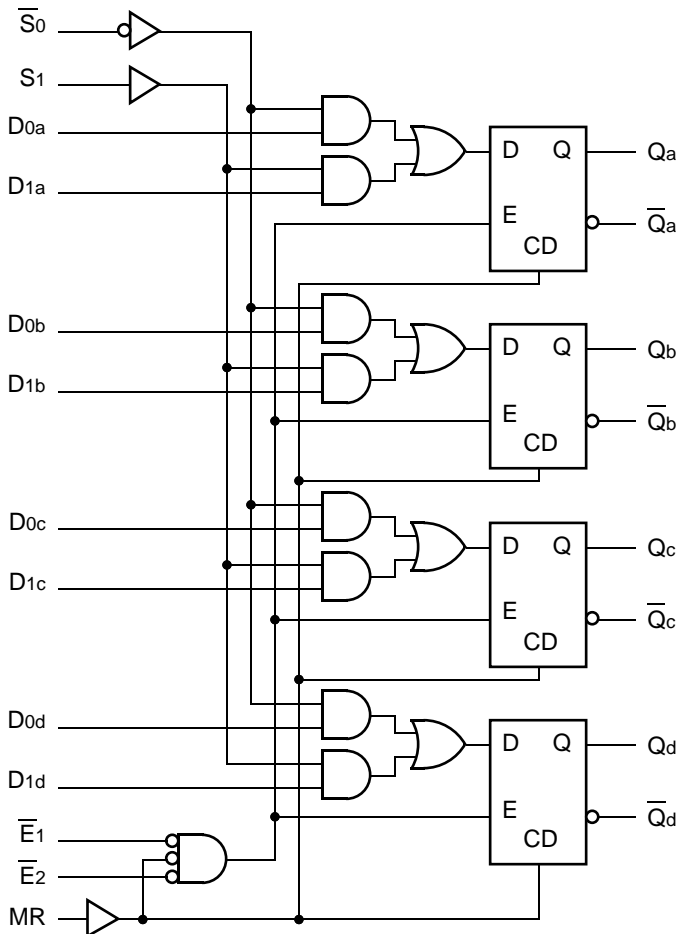
- Max. propagation delay of 1100ps
- Max. enable to output delay of 1400ps
- IEE min. of -80mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 50% faster than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

DESCRIPTION

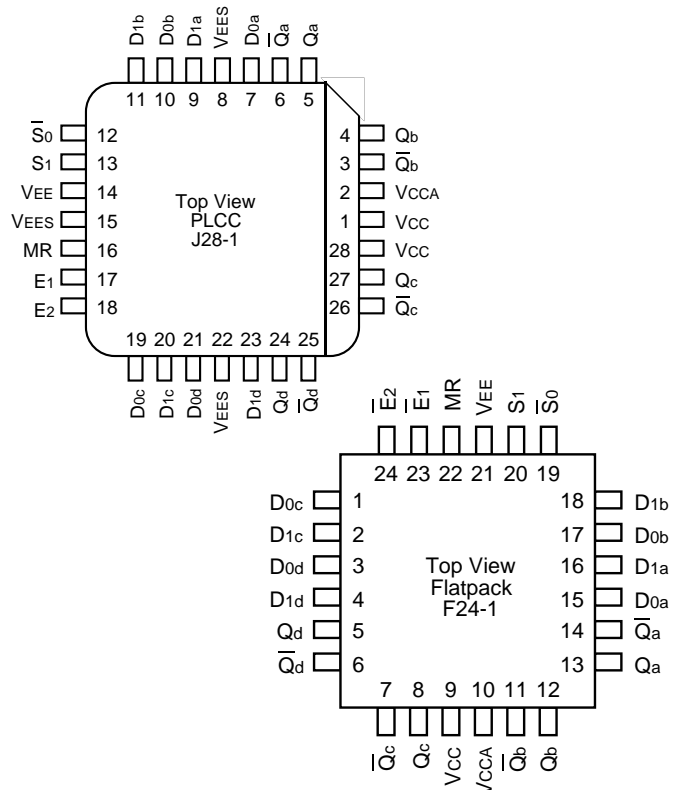
The SY100S355 offers four transparent latches with differential outputs and is designed for use in high-performance ECL systems. The Select inputs (\bar{S}_0 , S_1) select one of the two sources of input data (D_0 or D_1) to the latch. The Select inputs can also force the outputs to a logic LOW when the latch is in the transparent mode. The latches are in the transparent mode when both Enables (\bar{E}_1 , \bar{E}_2) are at a logic LOW state. In the transparent mode, the Select inputs can pass an input logic HIGH from D_0 or D_1 to the output.

If the Select inputs are tied together, then input data from either D_0 or D_1 is always passed through. A rising edge on either Enable input will latch the outputs with the most recent data at the latch inputs being stored. The Master Reset (MR) input overrides all other inputs and takes the Q outputs to a logic LOW. The inputs on this device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

Pin	Function
$\bar{E}_1 - \bar{E}_2$	Enable Inputs (Active LOW)
\bar{S}_0, S_1	Select Inputs
MR	Master Reset
$D_{na} - D_{nd}$	Data Inputs
$Q_a - Q_d$	Data Outputs
$\bar{Q}_a - \bar{Q}_d$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

TRUTH TABLE⁽¹⁾

Inputs							Outputs	
MR	\bar{E}_1	\bar{E}_2	S_1	\bar{S}_0	D1X	D0X	\bar{Q}_x	Qx
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched	
L	X	H	X	X	X	X	Latched	

NOTE:
 1. H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
IIH	Input HIGH Current	—	—	220	μA	VIN = VIH (Max.)
	\bar{S}_0, S_1					
	\bar{E}_1, \bar{E}_2					
	D_{na}, D_{nd}					
IEE	Power Supply Current	-80	-57	-40	mA	Inputs Open
	MR					

AC ELECTRICAL CHARACTERISTICS

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

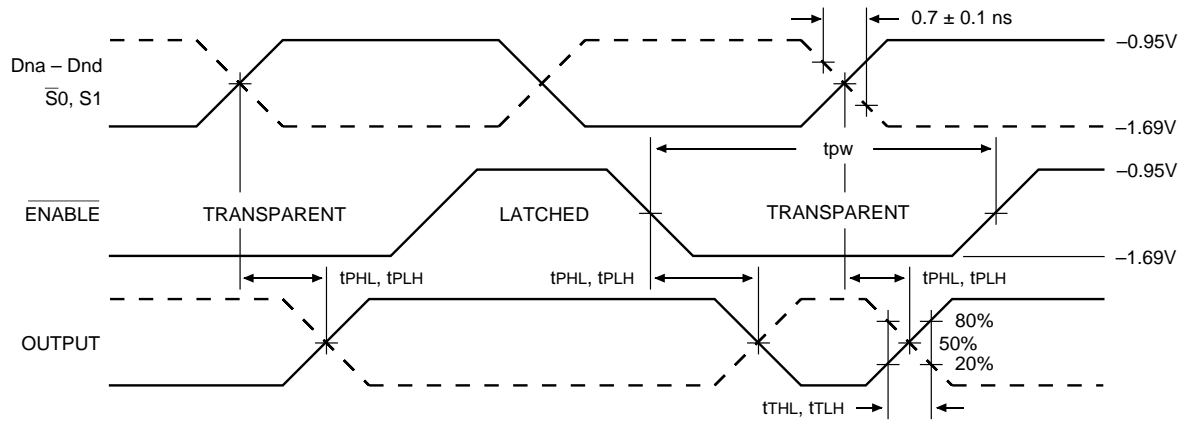
Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay D _{na} – D _{nd} to Output (Transparent Mode)	300	1200	300	1200	300	1200	ps	
tPLH tPHL	Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode)	300	1500	300	1500	300	1500	ps	
tPLH tPHL	Propagation Delay \bar{E}_1, \bar{E}_2 to Output	300	1500	300	1500	300	1500	ps	
tPLH tPHL	Propagation Delay MR to Output	300	1200	300	1200	300	1200	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time D _{na} – D _{nd}	700	—	700	—	700	—	ps	
	\bar{S}_0, S_1	1200	—	1200	—	1200	—		
	MR (Release Time)	1000	—	1000	—	1000	—		
t _H	Hold Time D _{na} – D _{nd}	400	—	400	—	400	—	ps	
	\bar{S}_0, S_1	400	—	400	—	400	—		
tPW (L)	Pulse Width LOW, \bar{E}_1, \bar{E}_2	1000	—	1000	—	1000	—	ps	
tPW (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps	

PLCC

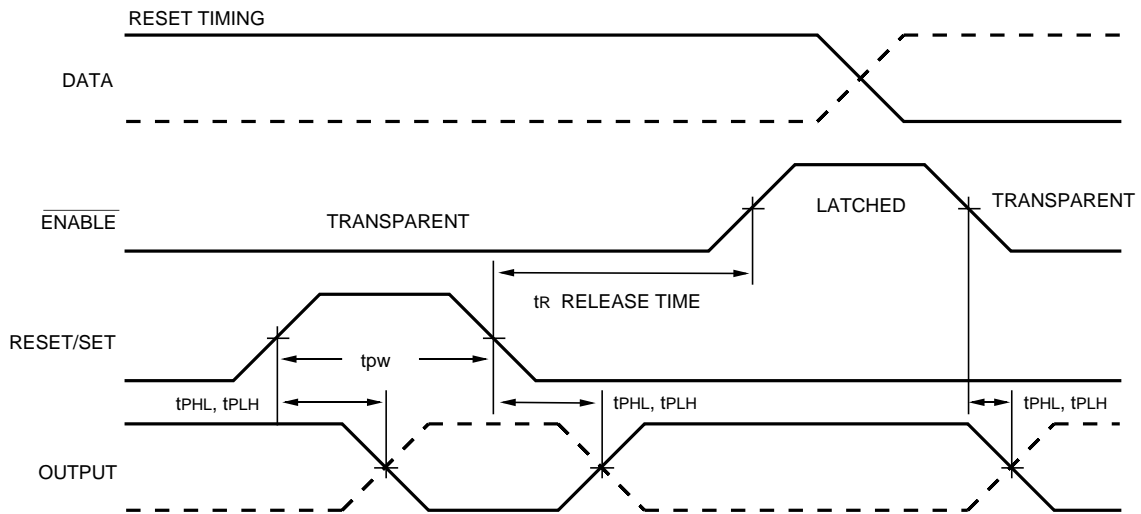
$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay D _{na} – D _{nd} to Output (Transparent Mode)	300	1100	300	1100	300	1100	ps	
tPLH tPHL	Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode)	300	1400	300	1400	300	1400	ps	
tPLH tPHL	Propagation Delay \bar{E}_1, \bar{E}_2 to Output	300	1400	300	1400	300	1400	ps	
tPLH tPHL	Propagation Delay MR to Output	300	1100	300	1100	300	1100	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time D _{na} – D _{nd}	700	—	700	—	700	—	ps	
	\bar{S}_0, S_1	1200	—	1200	—	1200	—		
	MR (Release Time)	1000	—	1000	—	1000	—		
t _H	Hold Time D _{na} – D _{nd}	300	—	300	—	300	—	ps	
	\bar{S}_0, S_1	300	—	300	—	300	—		
tPW (L)	Pulse Width LOW, \bar{E}_1, \bar{E}_2	1000	—	1000	—	1000	—	ps	
tPW (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps	

TIMING DIAGRAMS

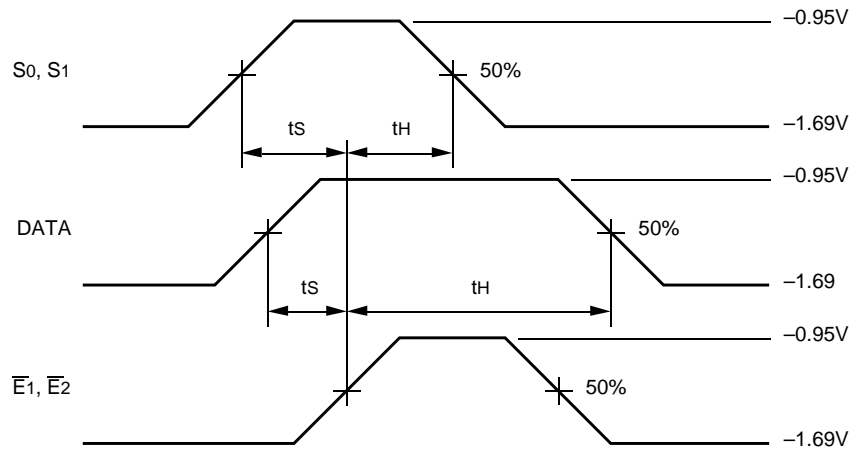


Enable Timing



Reset Timing

TIMING DIAGRAMS



Data Set-up and Hold Times

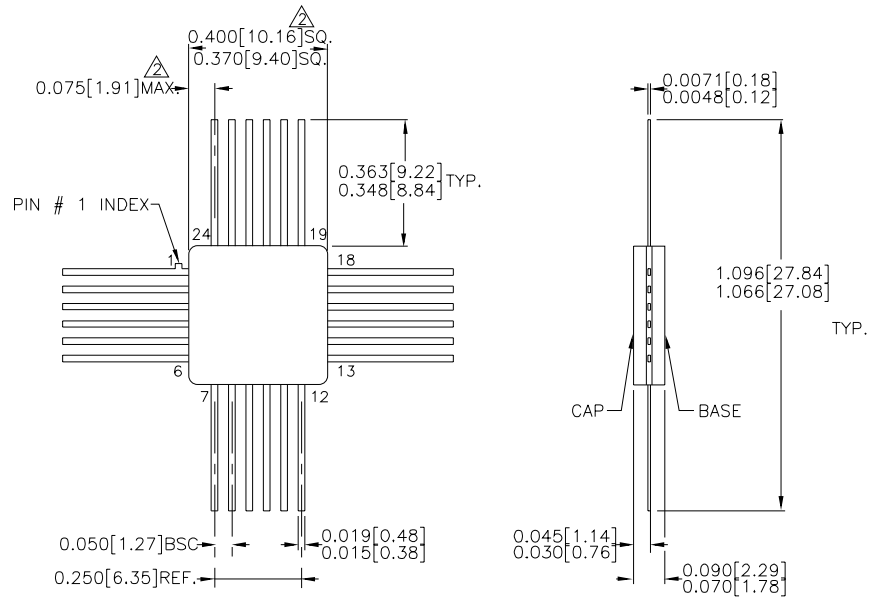
NOTES:

1. $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$
2. t_S is the minimum time before the transition of the clock that information must be present at the data input.
3. t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S355FC	F24-1	Commercial
SY100S355JC	J28-1	Commercial
SY100S355JCTR	J28-1	Commercial

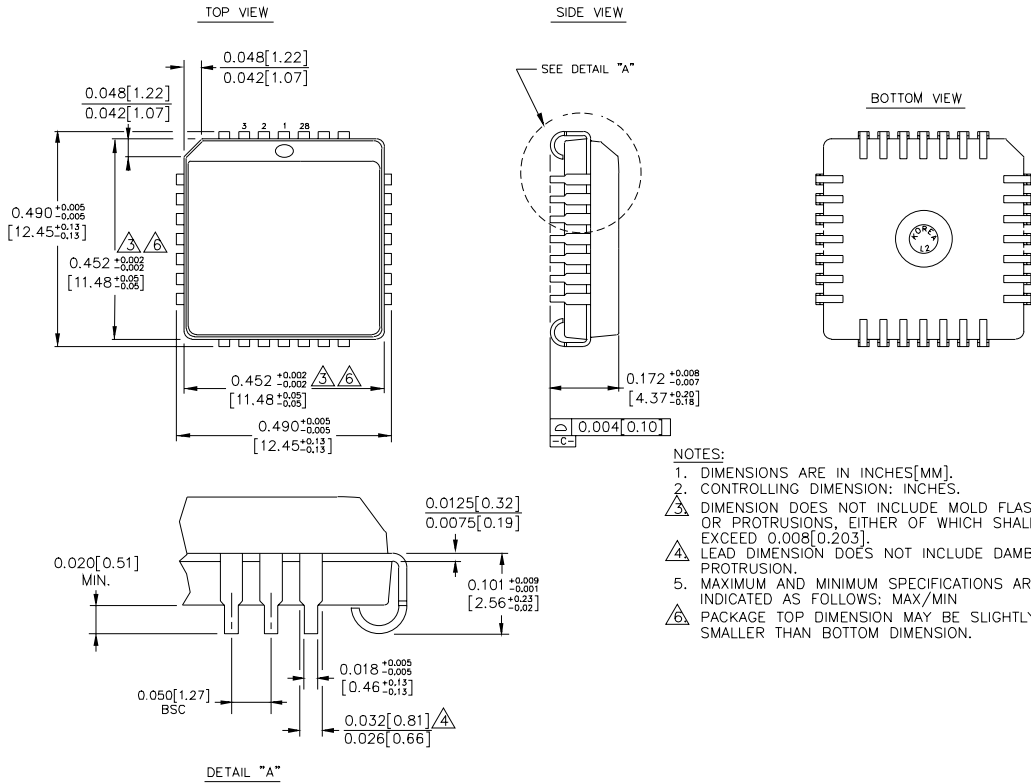
24 LEAD CERPACK (F24-1)



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



Rev. 03

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA

TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB <http://www.micrel.com>

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