

N-channel enhancement mode Logic level TrenchMOS™ transistor

IRLZ34N

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in switched mode power supplies and general purpose switching applications.

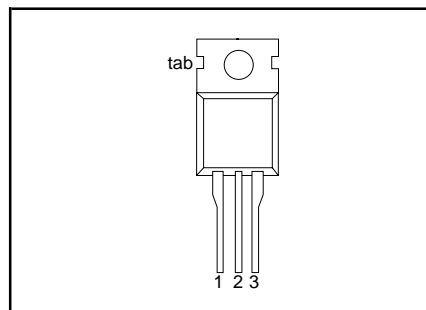
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	30	A
P_{tot}	Total power dissipation	68	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10\text{ V}$	35	mΩ

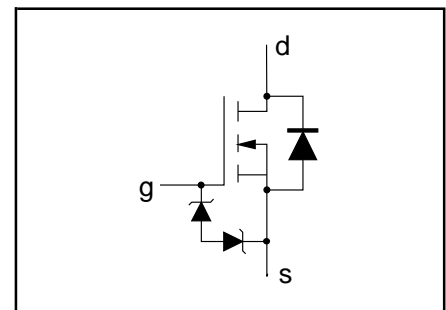
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ °C to }175\text{ °C}$	-	55	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ °C to }175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	$T_{mb} = 25\text{ °C}$	-	30	A
		$T_{mb} = 100\text{ °C}$	-	21	A
I_{DM}	Pulsed drain current	$T_{mb} = 25\text{ °C}$	-	110	A
P_D	Total power dissipation	$T_{mb} = 25\text{ °C}$	-	68	W
T_j, T_{stg}	Operating junction and storage temperature		-55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	2.2	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient		60	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

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ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.25 mA; T _j = -55 °C	55 50	- -	- -	V V
V _{(BR)GSS}	Gate-source breakdown voltage	I _G = ±1 mA;	10	-	-	V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA T _j = 175 °C T _j = -55 °C	1.0 0.5 -	1.5 - -	2.0 - 2.3	V V V
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 5 V; I _D = 17 A V _{GS} = 10 V; I _D = 17 A T _j = 175 °C	- - -	28 26 -	46 35 74	mΩ mΩ mΩ
g _{fs}	Forward transconductance	V _{DS} = 25 V; I _D = 15 A	12	40	-	S
I _{GSS}	Gate source leakage current	V _{GS} = ±5 V; V _{DS} = 0 V T _j = 175 °C	- -	0.02 -	1 20	μA μA
I _{DSS}	Zero gate voltage drain current	V _{DS} = 55 V; V _{GS} = 0 V; T _j = 175 °C	- -	0.05 -	10 500	μA μA
Q _{g(tot)}	Total gate charge	I _D = 30 A; V _{DD} = 44 V; V _{GS} = 5 V	-	22.5	-	nC
Q _{gs}	Gate-source charge		-	6	-	nC
Q _{gd}	Gate-drain (Miller) charge		-	11	-	nC
t _{d on}	Turn-on delay time	V _{DD} = 30 V; I _D = 25 A;	-	14	21	ns
t _r	Turn-on rise time	V _{GS} = 5 V; R _G = 10 Ω	-	77	110	ns
t _{d off}	Turn-off delay time	Resistive load	-	55	80	ns
t _f	Turn-off fall time		-	48	65	ns
L _d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L _d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L _s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C _{ISS}	Input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz	-	1050	1400	pF
C _{OSS}	Output capacitance		-	205	245	pF
C _{rSS}	Feedback capacitance		-	113	150	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

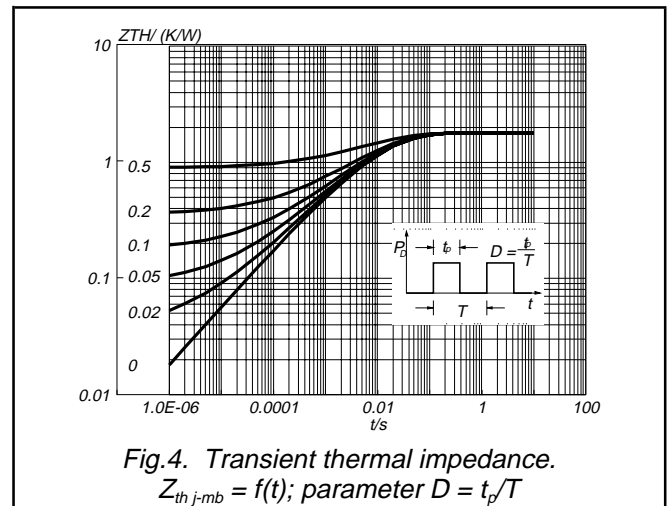
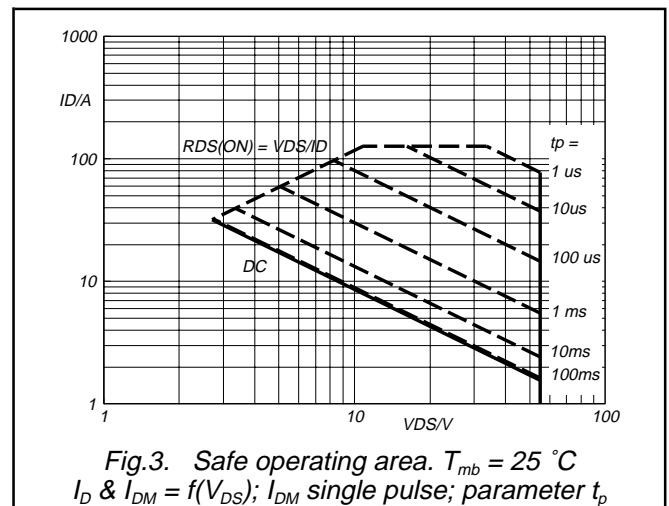
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _S	Continuous source current (body diode)		-	-	30	A
I _{SM}	Pulsed source current (body diode)		-	-	110	A
V _{SD}	Diode forward voltage	I _F = 25 A; V _{GS} = 0 V I _F = 34 A; V _{GS} = 0 V	- -	0.95 1.0	1.2 -	V V
t _{rr}	Reverse recovery time	I _F = 34 A; -di _F /dt = 100 A/μs;	-	40	-	ns
Q _{rr}	Reverse recovery charge	V _{GS} = -10 V; V _R = 30 V	-	0.16	-	μC

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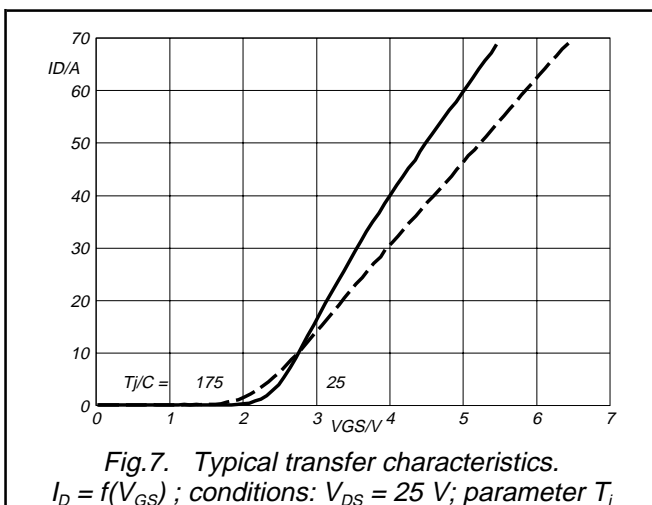
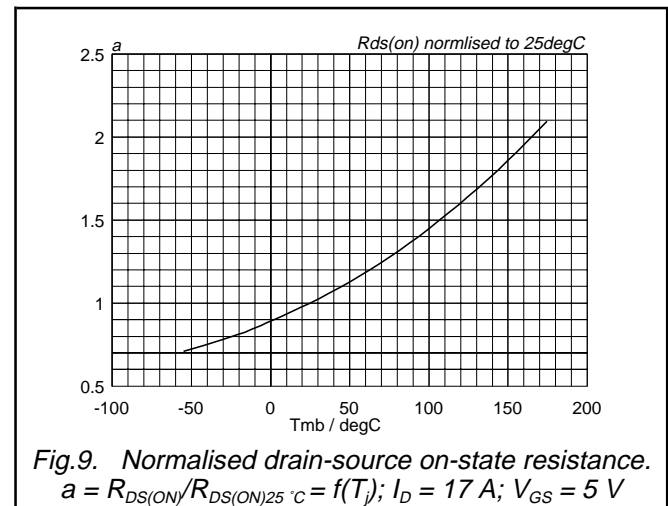
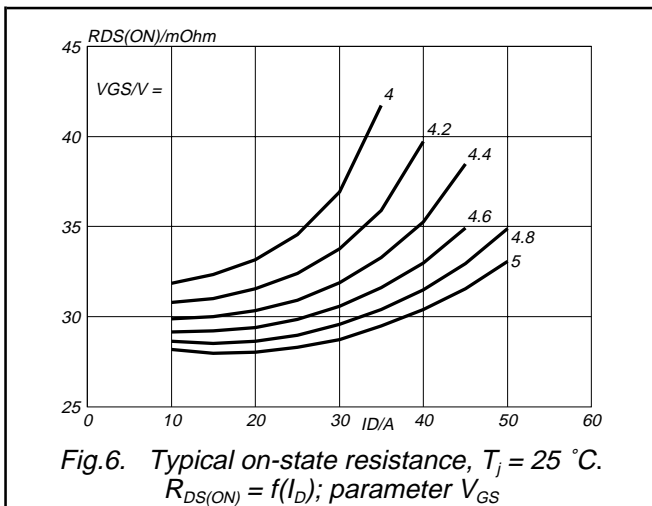
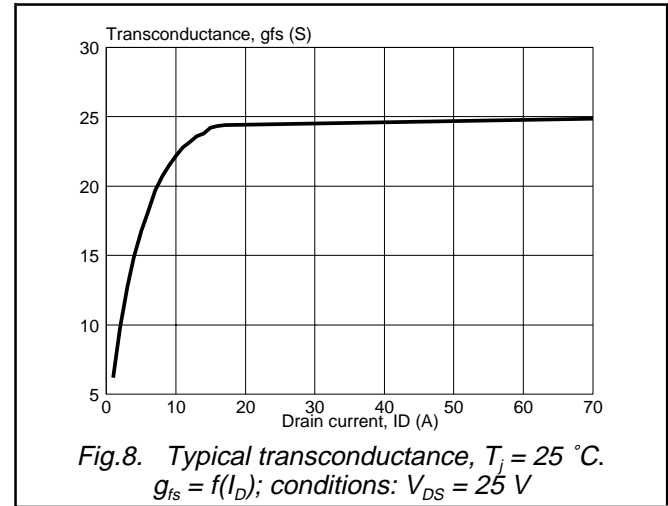
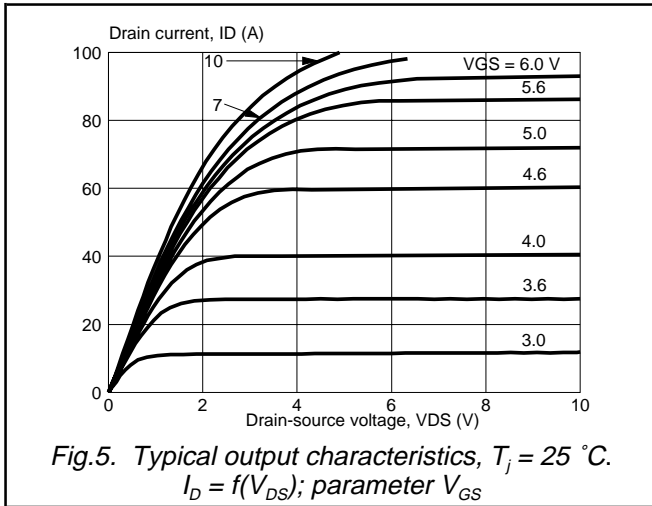
AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 20\text{ A}; V_{DD} \leq 25\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\ \Omega; T_{mb} = 25\text{ }^\circ\text{C}$	-	45	mJ



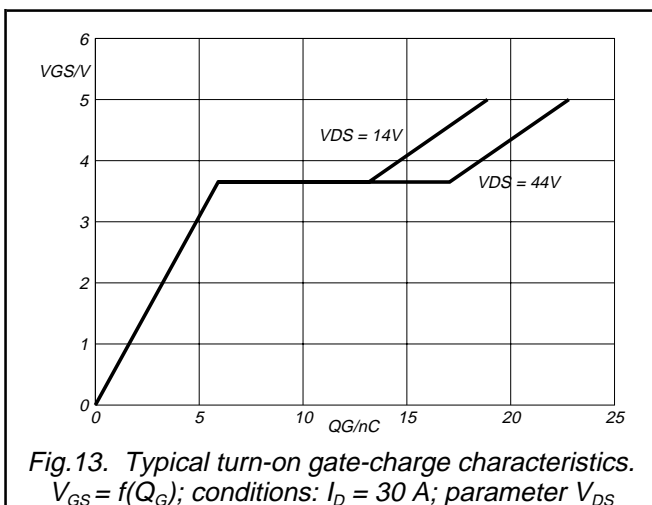
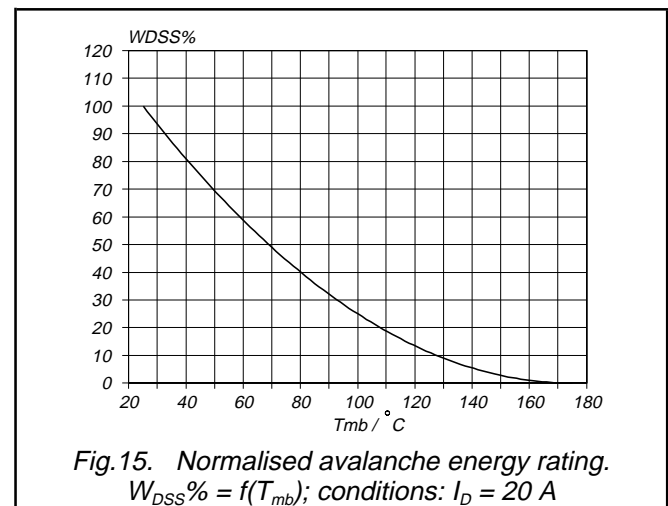
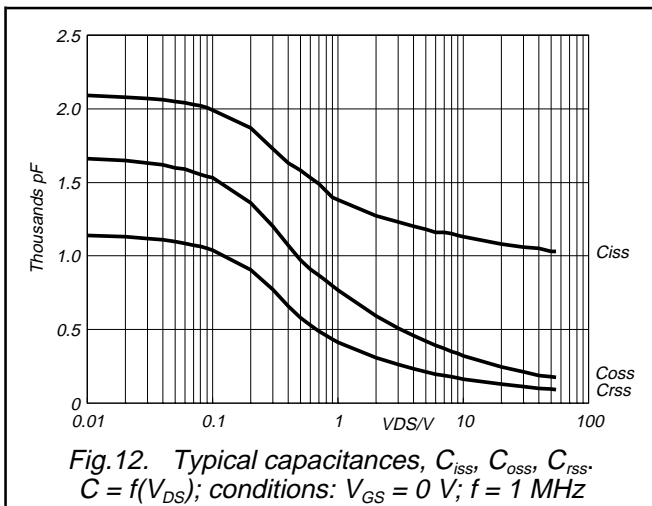
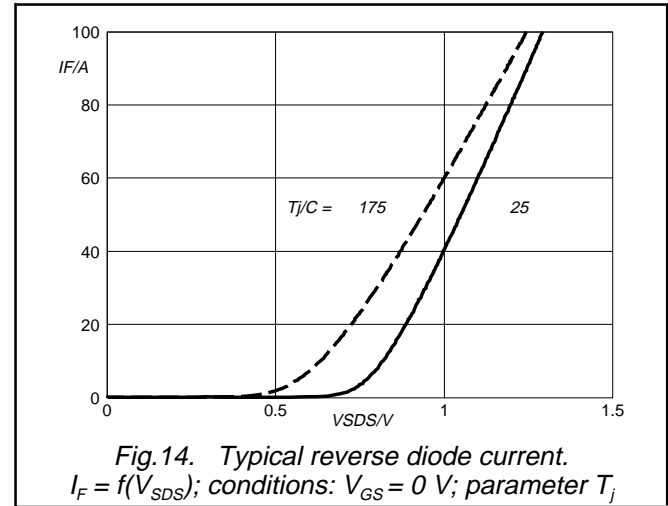
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MECHANICAL DATA

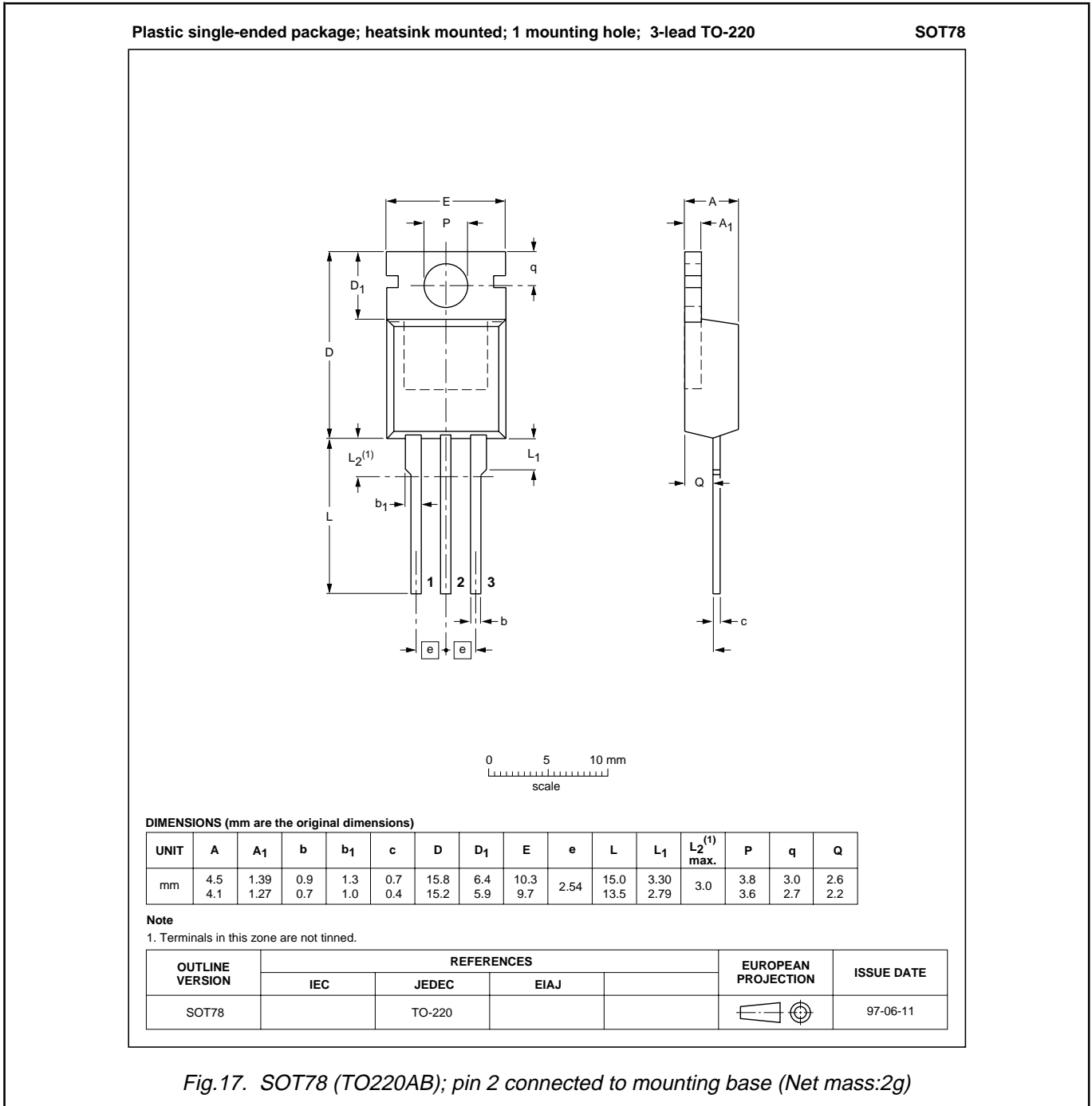


Fig. 17. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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