IC MEDIA
The Leader in CMOS Image Sensors

ICM200E

2 Megapixel (UXGA) Digital Color CMOS Image Sensor

Preliminary Data Sheet V1.1

General Description

The ICM200E (formerly ICM109W+) 2 megapixel (UXGA) digital color CMOS image sensor incorporates IC Media's industry-leading, wide acceptance angle pixel architecture, which is optimized for very low profile camera module applications with near CCD-quality color reproduction and low light sensitivity. The ICM200E image sensor has an UXGA-format RGB color pixel array (1600Hx1200V) capable of operating at up to 20 frames per second (fps) at full UXGA resolution and at progressively higher frame rates operating at sub-sampled SVGA and QSVGA resolutions.

The ICM200E image sensor's registers are programmed through an efficient, two-wire serial control interface (SIF) enabling flexible control of the sensor's operating modes. It outputs 10-bit raw RGB pixel samples synchronized to the associated pixel clock (PCLK) as well as vertical and horizontal synchronization signals (VSYNC/HSYNC). Few required external passive devices and low power consumption make the ICM200E image sensor ideally suited for compact form factor, battery-operated mobile consumer devices.

Feature Overview

- Wide acceptance angle pixel architecture enabling compact camera module form factors
- Very high sensitivity
- Excellent color reproduction for vibrant pictures
- Low active and stand-by power consumption
- Low light operating mode with image enhancing programmable pixel averaging
- Fast global reset for mechanical shutter
- Low complexity, two-wire serial control interface
- On-chip 11-bit column analog-to-digital converters with correlated double sampling and built-in automatic calibration
- Programmable exposure time, frame rate, sub-sampling, window size, analog and digital gain, horizontal and vertical image inversion, and dead pixel removal.

Applications

- Cellular phone cameras
- Personal digital assistants
- Digital still cameras and camcorders
- Notebook and desktop PC cameras
- Video telephony and conferencing equipment
- Security systems
- Industrial and environmental systems

Key Performance Parameters

Parameter	Typical Value
Optical format	1/2.6 inches
Active pixels	1600x1200
Physical pixels	1620x1220
Pixel size	3.45 μm x 3.45 μm
Sensor area	5.52 mm x 4.14 mm
Sensitivity	1.4 V/Lux-sec
Dynamic range	59 dB
Signal-to-noise ratio	45 dB
RGB gain	1/256 to 64x for individual Bayer pattern pixels
Exposure time	Min: 37.5 μs @ 20 fps
	Max: 72 s @ 0.2 fps
Fast global reset	1.5 ms @ 5 fps
Subsampling	SVGA (800x600)
	QSVGA (400x300)
Frame rate	Up to 20 fps @ UXGA
	Up to 40 fps @ SVGA
	Up to 60 fps @ QSVGA
Internal clock	6 MHz crystal
External clock	4 to 96 MHz with bypass PLL
Power supply	2.5 V (digital)
	2.8 V (analog)
Power consumption	130 mW (UXGA @ 15 fps)
Power down mode power	60 μW
Operating temperature	0 to 40 °C
Packaging	Bare die in wafer form
	48-pin CLCC14.22

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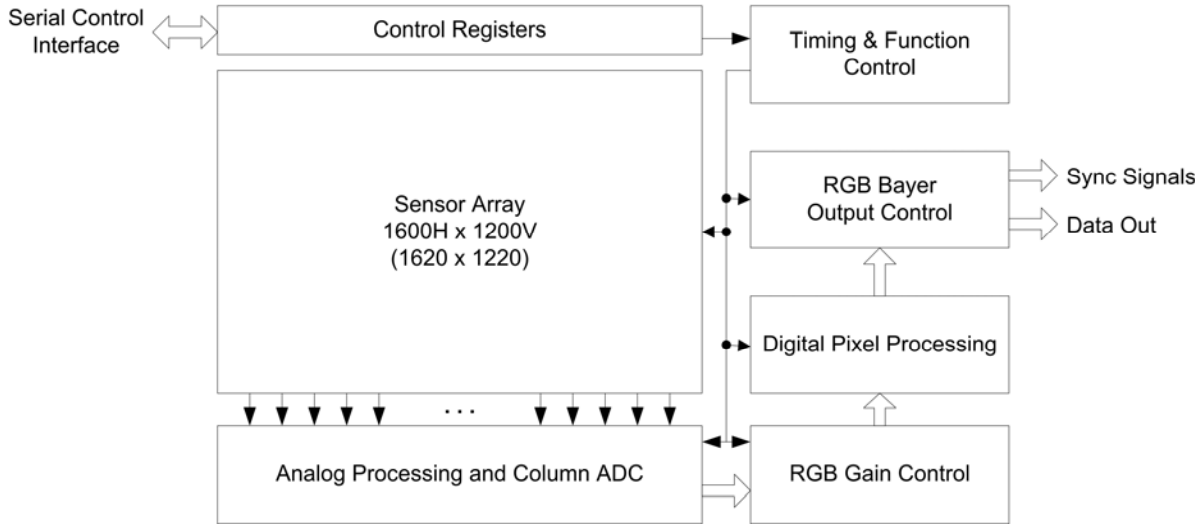


Figure 1. Sensor Block Diagram

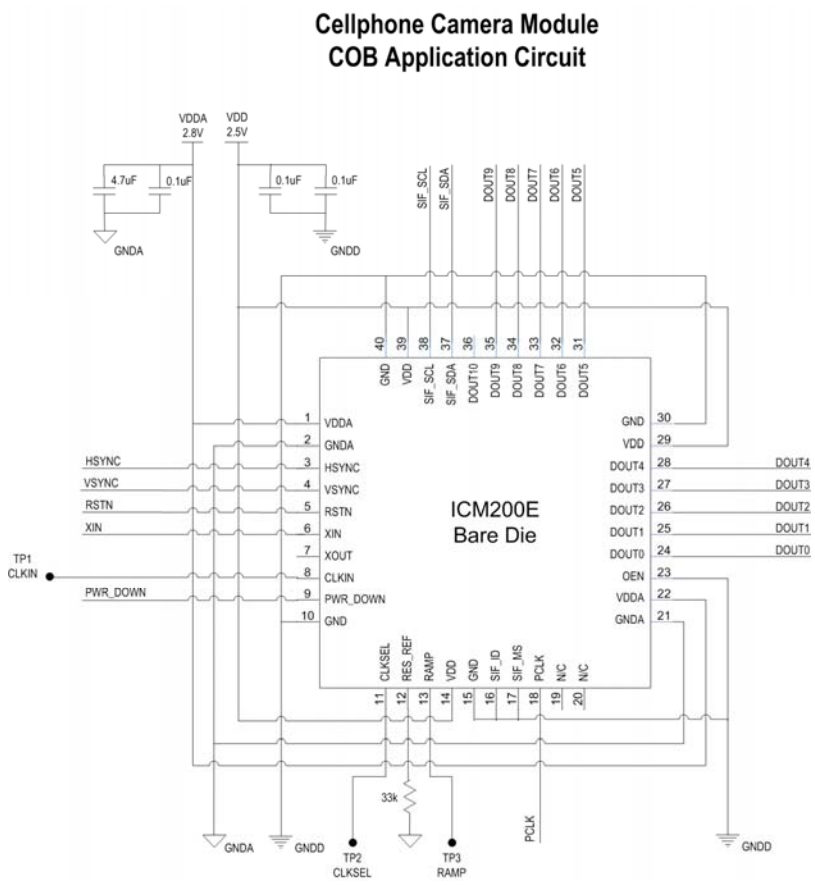


Figure 2. Cellular Telephone Camera Module COB Application Circuit

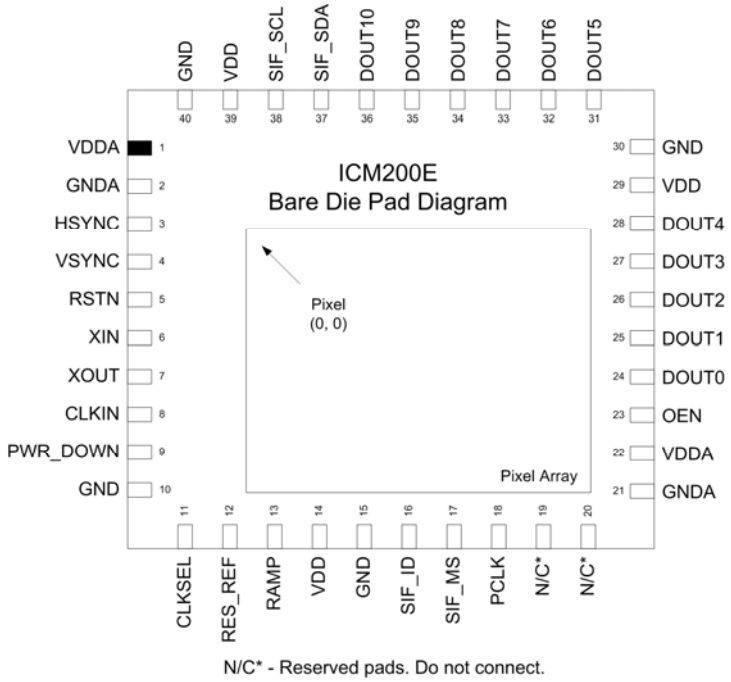


Figure 3. Bare Die Pad

Table 1. Bare Die Pad Assignments

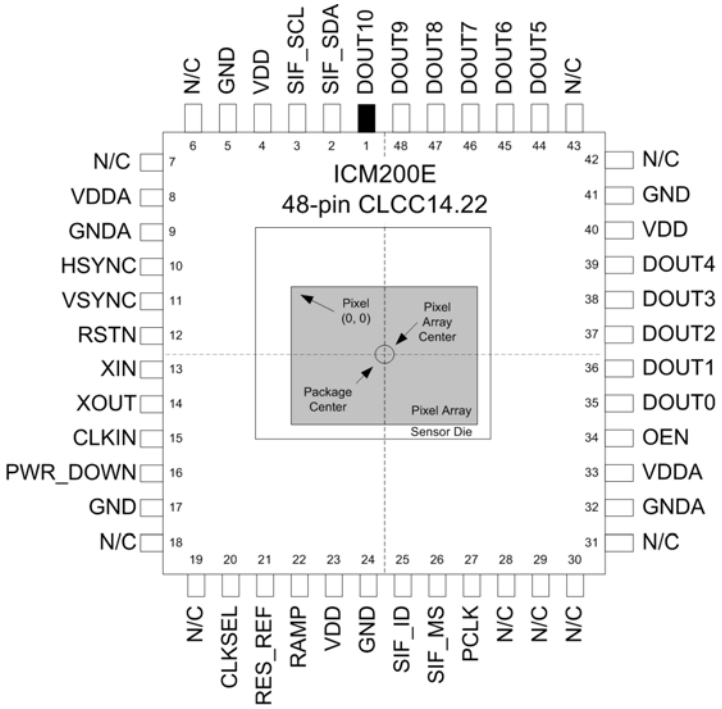
Pin	Name	Class*	Function
1, 22	VDDA	P	Sensor analog power
2, 21	GNDA	P	Sensor analog ground
3	HSYNC	D, I/O, N	Horizontal sync signal
4	VSYNC	D, I/O, N	Vertical sync signal
5	RSTN	D, I, U	Chip reset, active low
6	XIN	A, I	Crystal oscillator in, or external clock in; if external clocks are used, leave XOUT (pad 7) unconnected.
7	XOUT	A, O	Crystal oscillator out
8	CLKIN	D, I, N	External clock source; bypass PLL
9	PWR_DOWN	D, I, N	Power down control, 0: power down, 1: active
10, 15, 30, 40	GND	P	Sensor digital ground
11	CLKSEL	D, I, N	Clock source selection 0: clock through PLL, use XIN (pad 6) 1: bypass PLL, use CLKIN (pad 8)
12	RES_REF	A, I	Resistor to ground = 33 kΩ @ 48 MHz ADC clock
13	RAMP	A, O	Analog ramp output
14, 29, 39	VDD	P	Sensor digital power
15, 30, 40	GND	P	Sensor digital ground
16	SIF_ID	D, I, N	LSB of SIF slave address

Table 1. Bare Die Pad Assignments (continued)

Pin	Name	Class*	Function
17	SIF_MS	D, I	Indicates whether the SIF interface is in master mode (autoload mode) or in slave mode. When the MSSEL pin is pulled down during power up, the sensor's SIF interface is operated as a SIF slave device waiting to be controlled by an external SIF master, such as a microprocessor. When the MSSEL pin is pulled up during power up, the sensor's SIF interface is first acting as a SIF master device trying to read from an external SIF EEPROM. After that, the SIF interface returns to slave mode. Selection: 0 = slave and 1= master.
18	PCLK	D, O	Pixel clock output
19	N/C	D, O	Reserved, do not connect
20	N/C	D, O	Reserved, do not connect
23	OEN	D, I, N	Output enable: 0: enable, 1: disable
24	DOUT[0]	D, I/O	Data output bit 0 determines whether the sensor's HYSYNC and VSYNC signals will work under master mode or slave mode. If pulled up, the sensor will output the HYSNYC and VSYNC signals to the backend chip, which is the master mode; if pulled down, the sensor will accept the HSYNC and VYSNC signals from the backend chip to control the sensor's internal frame timing, which is the slave mode.
25	DOUT[1]	D, I/O	Data output bit 1; if pull up or pull down is applied to this pin, AD_IDL[0] (Sub ID) is 1 or 0 respectively.
26	DOUT[2]	D, I/O	Data output bit 2; if pull up or pull down is applied to this pin, AD_IDL[1] (Sub ID) is 1 or 0 respectively.
27	DOUT[3]	D, I/O	Data output bit 3; if pull up or pull down is applied to this pin, AD_IDL[2] (Sub ID) is 1 or 0 respectively.
28	DOUT[4]	D, I/O	Data output bit 4; if pull up or pull down is applied to this pin, AD_IDL[3] (Sub ID) is 1 or 0 respectively.
31	DOUT[5]	D, I/O	Data output bit 5; if pull up or pull down is applied to this pin, TIMING_CONTROL_LOW[1] (HSYNC polarity) is 1 or 0 respectively.
32	DOUT[6]	D, I/O	Data output bit 6; if pull up or pull down is applied to this pin, the initial value of TIMING_CONTROL_LOW[2] (VSYNC polarity) is 1 or 0 respectively.
33	DOUT[7]	D, O	Data output bit 7
34	DOUT[8]	D, O	Data output bit 8
35	DOUT[9]	D, O	Data output bit 9
36	DOUT[10]	D, O	Data output bit 10
37	SIF_SDA	D, I/O	SIF data
38	SIF_SCL	D, I/O	SIF clock

* **Class Codes:** A – analog signal, D – digital signal, I – input, O – output, P – power or ground, U – internal pull-up, N – internal pull-down, N/C – no connection.

Figure 4. 48-Pin CLCC14.22 Package



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Functional Description

ICM200E image sensor is a single-chip digital color-imaging device. It includes a 1600x1200 sensor array, 1620 column-level ADCs, and correlated double sampling circuitry. Writing into the SIF interface, which can address the register file consisting of 8-bit registers, sets all the programmable parameters. The output format is 10-bit raw RGB data, together with horizontal and vertical synchronization signals.

Image Sensor Array

The image array consists of 1620x1220 physical pixels. Each pixel has a light sensitive photo diode and a set of control transistors. At the beginning of the pixel exposure cycle, a row of pixels is pre-charged to its maximum value. Then the row is exposed to light for several lines worth of time and sampled by the ADC. A correlated double sampling (CDS) process subtracts the reset value (sampled right after sampling the current signal) from the signal value. The CDS output is approximately proportional to the amount of received light, ranging from 0 to 1023.

There are 10 dummy rows and columns surrounding the array. Of the 10 dummy pixels, 7 of them on the outside edges are covered with dark filters. The other three dummy pixels are active pixels covered by Red, Green and Blue Color filters in a Bayer pattern. These three pixels are used for color interpolation.

The 1600x1200 (UXGA) size active signal pixel array, Pixel(10, 10) through Pixel(1609, 1209), is also covered by an array of Red, Green and Blue color filters in a Bayer pattern. See Figure 5 for a detailed layout of the sensor array.

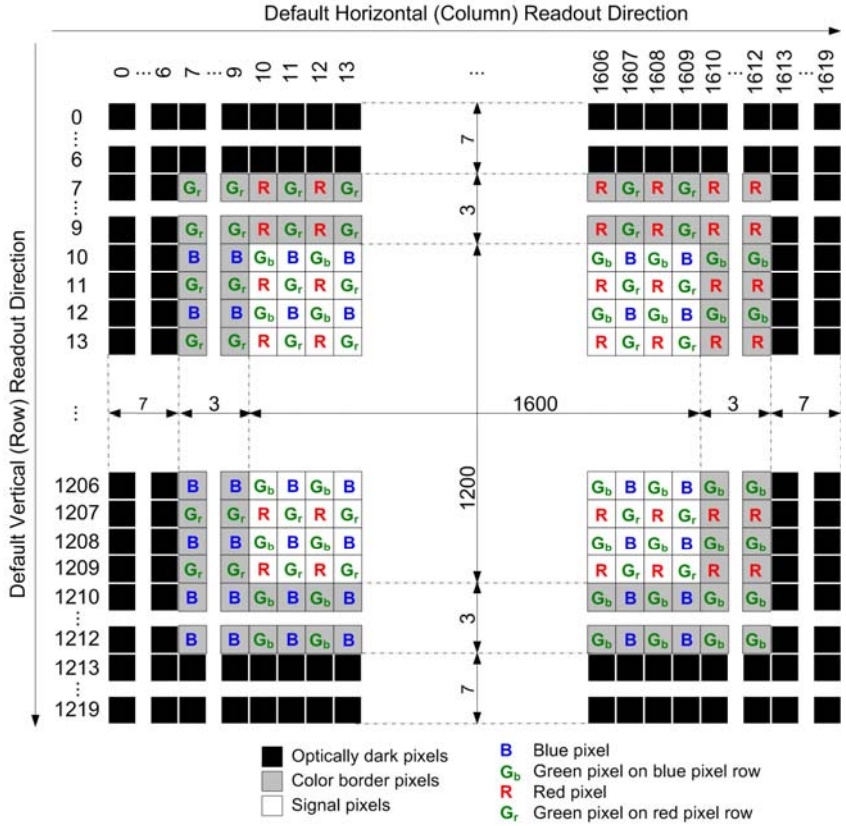

Figure 5. Image Sensor Array

Exposure Time

To accommodate different lighting requirements, you can change the exposure time by adjusting registers 0x1C and 0x1D. The exposure time is measured in terms of the time to read out one line of data.

The time for processing one line is equal to the pixel clock period times the frame width. The frame width is stored in registers 0x0C and 0x0D. The default exposure time for one line width of 1800 is 75 μs when the pixel clock is at 48 MHz.

Digital Gain Control

The ICM200E digital gain control feature is one of the methods you can use to control image quality. Adjusting the digital gain is generally used for minor changes, either to balance color or to adjust the overall image luminance. The default gain range is from 1/256 to 8 of the four Bayer pattern pixels as indicated by the format of 3.8. The format is defined by register 0x52[3:0].

Gain changes require changes to two types of registers, the immediate gain values (registers 0x20-0x28), and the magnitude of change register. The magnitude of change register is register 0x52[3:0]. The default notation is in the 3.8 format, which can be modified to as high as 6.5 by selecting register 0x52[3:0].

Pixel Timing and Function Control

The ICM200E has a software-controlled pixel analog data path. This feature allows fine-tuning of the sensor's performance and makes the sensor highly adaptable to a wide range of applications. The pixel analog data path timing is controlled by the default settings or by downloading a pixel configuration table. Register 0x02[4] makes the selection. Pixel configuration tables are sequentially downloaded into registers 0x04, 0x05, and 0x06 while incrementing the 0x03 address pointer.

Auto Analog Gain Calibration

The analog gain can be calibrated by adjusting the maximum analog input and the maximum ADC output so that they have the same dynamic range. To enable automatic gain calibration, write 0x1 into register 0x00[1].

Low Light Mode

The ICM200E implements an operating mode for low light conditions. The Low Light mode uses a special purpose pixel analog data path configuration with a fixed 3x analog gain. The low light mode is initialized by sequentially downloading a low light pixel configuration table. Setting register 0x91[3:0] to 0x00 enables low light mode. Restore normal operation by loading the default pixel configuration table, followed by setting register 0x02[4] to 0x1. The default operating mode is resumed by writing 0x1 into register 0x00[1].

Fast Global Reset/M-Shutter

The ICM200E implements a fast global reset feature in support of low cost mechanical shutters. With fast global reset, the ICM200E image sensor array can be reset in 1.5ms @ 5fps (PCLK=12 MHz). An example fast global reset image capture sequence is described in Figure 6.

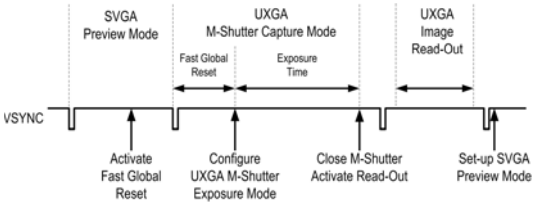

Figure 6. Fast Global Reset

Subsampling Schemes

The ICM200E image sensor allows viewfinder and other reduced data output modes. It supports reduced resolution in both SVGA and QSVGA formats. In addition, the ICM200E image sensor provides an averaging mode in each of the reduced resolution formats to further increase the signal-to-noise (S/N) ratio. The resolution for UXGA is 1600x1200, which is the native resolution of the ICM200E. There is no sub-sampling relationship at UXGA.

Output Data Format

During normal operation, the output format is 10-bit raw data that ranges from 0 to 1023. In addition to the data pins, the chip also outputs VSYNC, HSYNC, and PCLK. The length and polarity of the VSYNC and HSYNC signals can

be adjusted through the registers. The line and frame timing can be adjusted through registers 0xA1 and 0xA2 for width and registers 0xA3 and 0xA4 for height.

Clock and PLL

The ICM200E image sensor has a built-in phase-locked loop (PLL). It enables the sensor's flexibility to work under different external clock frequencies. The pixel clock, PCLK, is a multiple of the external clock. Although the output data is 10 bits, the internal ADC is 11 bits to minimize quantization noise. Therefore, the ADC clock is running at twice the frequency of the PCLK.

Power Down Mode

When the POWERDN pin is de-asserted, the chip goes into power down mode. In this state, the internal clock is stopped. The POWERDN pin is not synchronized with the clock. The power down takes effect immediately. On the assertion of the POWERDN pin, the sensor must wait at least 10 μs to leave the power down mode to prevent the sensor from operating in an unstable state.

Serial Control Interface (SIF)

The serial control interface of the ICM200E image sensor is fully compatible with the I2C interface. Register programming is through the SIF interface (SCL and SDA pins). The default 7-bit SIF device address is 0x20. The SIF ID pin can configure the last bit of the device address. The ICM200E image sensor can operate in either SIF master mode or in slave mode right after power up, depending on the pull-up or pull-down of the MSSEL pin.

When the MSSEL pin is pulled-down during power up, the ICM200E image sensor's SIF interface is operated as a SIF slave device waiting to be controlled by an external SIF master such as a microprocessor. When MSSEL is pulled-up during power up, the SIF interface is first acting as a SIF master device trying to read from an external SIF EEPROM. After that, it will return to slave mode. If the sensor's slave address is 0x21, then the EEPROM address will be 0x51. If the sensor's slave address is 0x20, then the EEPROM address will be 0x50.

In the auto-loading mode, the ICM200E image sensor will not respond to ACK for the serial bus command until the EEPROM has completed loading.

SIF Registers

Table 2. SIF Registers Descriptions

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x00 PART_CONTROL			
Processing control [0] Reserved * [1] Reserved * [2] Exposure time control. Writing a 0x1 will activate the new value set in the AD_EXPOSE_TIME register when read back from it. A 0x0 means that either the exposure time change is finished (in video mode), or that the entire frame is transmitted. A 0x1 means that either the exposure time change is still in progress. [3] 0x0: Normal mode. 0x1: Subsampling mode. [6:4] Frame rate for different main clock frequencies. [7] Latent change. Writing a 0x1 means that the changed latent registers now start taking effect. When the entire operation is done, the read back value of this bit will change from 0x1 to 0x0.	0x00	Y	Y

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x01 TIMING_CONTROL_LOW **0x02 TIMING_CONTROL_HIGH**			
Timing control [0] Column count enable. Set to 0x0 when filling the register file. Set to 0x1 for normal operation. [1] HSYNC polarity, 0x0: active low, 0x1: active high. The DOUT[5] pin determines the initial value. [2] VSYNC polarity, 0x0: active low, 0x1: active high. The DOUT[6] pin determines the initial value. [3] Reserved * [4] Timing select, 0x0: register file timing, 0x1: default timing [8] IRST select, 0x0: from register file, 0x1: from IRST_NUMBER register [10] Reserved * [12] Out-of-array exposure pointer control, 0x0: points to row 1217, 0x1: points to row 1221 (a non-existent row) [13] Column stop. Setting to 0x0: causes the sensor column counter to stop at 1599 when it is exceeding the real array. Setting to 0x1: causes the sensor column counter to keep counting.	0x0011	N	N
0x03 TABLE_ADDR			
Reserved*	0x00	N	N
0x04 WTRAM_DATA_L **0x05 WTRAM_DATA_M** **0x06 WTRAM_DATA_H**			
Reserved*	0x000000	N	N
0x07 TABLE_LEN			
Reserved*	0x00	N	N
0x08 RAM_WRITE_ACTION			
Reserved*	0x01	N	N
0x09 IRST_NUMBER_LOW **0x0A IRST_NUMBER_HIGH**			
Reserved*	0x0000	N	N
0x0B			
Reserved*			
0x0C AD_WIDTHL **0x0D AD_WIDTHH**			
[10:0] Defines the frame width. The frame width must be more than AD_COL_BEGIN+ 1620.	0x0708 (1800)	Y	Y
0x0E AD_HEIGHTL **0x0F AD_HEIGHTH**			
[15:0] Defines the frame height. The frame height must be more than AD_ROW_BEGIN + 1220.	0x0514 (1300)	Y	Y

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x10 AD_COL_BEGINL **0x11 AD_COL_BEGINH**			
[10:0] Beginning of the active line in terms of column position. [11] Mirror image enable. [12] Up-down image enable. AD_COL_BEGIN must be more than AD_HSYNC_END.	0x0064 (100)	Y	Y
0x12 **0x13**			
Reserved*			
0x14 AD_ROW_BEGINL **0x15 AD_ROW_BEGINH**			
[15:0] The beginning of the active frame in terms of row position (changed to 0x0010H for QSVGA sub-sampling mode). AD_ROW_BEGIN must be more than AD_VSYNC_END.	0x000A	Y	Y
0x18 AD_HSYNC_ENDL **0x19 AD_HSYNC_ENDH**			
[10:0] Defines the HSYNC pulse width, which is the end of the horizontal sync in terms of column position.	0x0040 (64)	Y	Y
0x1A AD_VSYNC_ENDL **0x1B AD_VSYNC_ENDH**			
[15:0] Defines the VSYNC pulse width, which is the end of the vertical sync in terms of row position.	0x0003 (3)	Y	Y
0x1C AD_EXPOSE_TIMEL **0x1D AD_EXPOSE_TIMEH**			
[15:0] Exposure time in terms of the number of rows.	0x0513 (1299)	N	Y
0x1E **0x1F**			
Reserved*			
0x20 AD_M1_L **0x21 AD_M1_H**			
10:0] Gain coefficient (B). Unsigned 3.8 (default) format.	0x0100 (256)	Y	Y
0x22 AD_M2_L **0x23 AD_M2_H**			
[10:0] Gain coefficient (G) on the blue line. Unsigned 3.8 (default) format.	0x0100 (256)	Y	Y

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x24 AD_M3_L **0x25 AD_M3_H**			
[10:0] Gain coefficient (G) on the red line. Unsigned 3.8 (default) format.	0x0100 (256)	Y	Y
0x26 AD_M4_L **0x27 AD_M4_H**			
[10:0] Gain coefficient (R). Unsigned 3.8 (default) format.	0x0100 (256)	Y	Y
0x28 through 0x3F			
Reserved*			
0x40 AD_DARK_DATA_L **0x41 AD_DARK_DATA_H**			
[9:0] When auto dark correction is disabled, serves as the subtrahend for dark correction	0x0000	N	Y
0x42 AD_HighLimit **0x43**			
[9:0] Apply dead pixel removal algorithm only to those pixel above HighLimit.	0x03FF (1023)	N	N
0x44 AD_LowLimit **0x45**			
[9:0] Apply dead pixel removal algorithm only to those pixels below LowLimit.	0x0000	N	N
0x46 AD_DSLOP_BEGINL_C **0x47 AD_DSLOP_BEGINH_C**			
Reserved*	0x0000	N	N
0x48 AD_DSLOP_ENDL_C **0x49 AD_DSLOP_ENDH_C**			
Reserved*	0x0000	N	N
0x50 AD_DARK_DATA_EXTRA			
Reserved*	0x00	N	Y
0x51 AD_OUTMODE			
[0]: Column average for subsampling (2-point average). [1]: Column average for subsampling (4-point average). [2]: Four-point average (column and row) for UXGA mode.	0x00	N	Y

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x52 AD_INOUTSEL			
[3:0] RGB gain format for registers AD_M1, AD_M2, ADM3, and AD_M4. 0x0: Default, unsigned 3.8 format 0x1: Default, unsigned 4.7 format 0x2: Default, unsigned 5.6 format 0x3: Default, unsigned 6.5 format Others: Unsigned 3.8 format [7:4] Output format 0x0: Normal mode 0x1: Dead pixel removal mode 0x2: SVGA subsampling mode 0x3: QSVGA subsampling mode 0x4: Control signal 0x5: Sensor row 0x6: Sensor column Others: Normal mode	0x00	N	Y
0x53 AD_RAMPSEL			
Reserved*	0x00	N	N
0x54 AD_DSRSTL **0x55 AD_DSRSTH**			
Reserved*	0x0000	N	N
0x56 AD_DSDATAL **0x57 AD_DSDATAH**			
Reserved*.	0x07D0 (2000)	N	N
0x82 AD_IDL **0x83 AD_IDH**			
[3:0] Sub ID, Read from pins DOUT [4:1] during reset [15:4] Device ID. Can be configured using the SIF interface.	0xD090 (53392)	N	N
0x90 AD_RSTSEL			
Reserved*	0x80	N	N
0x91 AD_SLOPEREG			
Reserved*	0x8A (138)	N	N
0x92 AD_TXRSTSEL			
Reserved*	0x22 (34)	N	N
0x93 AD_SUBPH_PULSE			
Reserved*	0x10 (16)	N	N
0x94 AD_BITCONTROL			
Reserved*	0xC0 (192)	N	N

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x97 AD_WT_BEGINL **0x98 AD_WT_BEGINH**			
Reserved*	0x0000	N	N
0x99 AD_WT_ENDL **0x9A AD_WT_ENDH**			
[10:0] Register file end point. When it is reached, the waveform will remain fixed until the start of the next row.	0x07F8 (2040)	N	N
0x9B AD_SUB_EN_TIMEL **0x9C AD_SUB_EN_TIMEH**			
Reserved*	0x05BE (1470)	N	N
0x9D SEN_HEIGHT_REFL **0x9E SEN_HEIGHT_REFH**			
Maximum increase step of exposure time in terms of lines: frame height - SEN_HEIGHT_REF. [15:0] Exposure time in terms of number of rows. Changing the value of this register changes the maximum exposure time increase step.	0x04C8 (1224)	Y	Y
0x9F			
Reserved*	0x00	Y	Y
0xA0			
Reserved*	0x00	Y	Y
0xA1 AD_WIDTHL_C **0xA2 AD_WIDTHH_C**			
Reserved*	0x0708 (1800)	N	Y
0xA3 AD_HEIGHTL_C **0xA4 AD_HEIGHTH_C**			
Reserved*	0x0514 (1300)	N	Y
0xA5 AD_COL_BEGINL_C **0xA6 AD_COL_BEGINH_C**			
Reserved*	0x0064 (100)	N	Y
0xA7 AD_ROW_BEGINL_C **0xA8 AD_ROW_BEGINH_C**			
Reserved*	0x000A (10)	N	Y
0xA9 AD_HSYNC_ENDL_C **0xAA AD_HSYNC_ENDH_C**			
Reserved*	0x0040 (64)	N	Y

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0xAB AD_VSYNC_ENDL_C **0xAC AD_VSYNC_ENDH_C**			
Reserved*	0x0003 (3)	N	Y
0xAD AD_PART_CONTROL_C			
Reserved*	0x00	N	Y
0xAE AD_WT_BEGINL_C **0xAF AD_WT_BEGINH_C**			
Reserved*	0x0000	N	Y
0xB0 AD_WT_ENDL_C **0xB1 AD_WT_ENDH_C**			
Reserved*	0x07F8 (2040)	N	Y
0xB2 and 0xB3			
Reserved*	0x0000	Y	Y
0xB4 AD_PLL			
[7:0] The PLL setting for the ADC clock. For example, at 6 MHz input, selecting 0x03 would run the system ADC clock at 24 MHz. Note: The maximum ADC clock is 96MHz for 30 fps operation. The default value is 0x01, for a "2x" PLL multiplier. Setting / PLL Multiplier 0x00 / 1x 0x01 / 2x 0x02 / 3x 0x03 / 4x … 0x1F / 32x	0x01	N	Y
0xB5			
Reserved*	0x00	Y	Y
0xB6 AD_F_MAX_ADDRL **0xB7 AD_F_MAX_ADDRH**			
Reserved*	0x04B9 (1209)	Y	Y
0xB8 AD_F_OVERL **0xB9 AD_F_OVERH**			
Reserved*	0x04BA (1210)	Y	Y
0xBA AD_F_LIMITAL **0xBB AD_F_LIMITAH**			
Reserved*	0x04BB (1211)	Y	Y

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0xBC AD_F_LIMITBL **0xBD AD_F_LIMITBH**			
Reserved*	0x0002 (2)	Y	Y
0xBE AD_F_LIMITCL **0xBF AD_F_LIMITCH**			
Reserved*	0x04BA (1210)	Y	Y

* Reserved bits must *not* be changed.

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Specification		Rating
Supply voltage	V_{DDA}	3.0 V
	V_{DD}	2.8 V
Input voltage		-0.3 V to V_{DD} +0.3V
Output voltage		-0.3 V to V_{DD} +0.3V
Storage temperature		0 to 65°C
ESD rating	Human body model [1]	2,000 V
	Machine model [2]	200 V
Latch-up protection [3]		125 mA
Convection or IR reflow temperature [4]		260°C for 40 seconds

Notes: [1] EIA/JESD22-A114
[2] EIA/JESD22-A115
[3] EIA/JESD78
[4] IPC/JEDEC-J-STD-020C

Electrical Characteristics

DC Characteristics

(V_{DD}=2.5V, V_{DDA}=2.8V, T_A=25°C)

Table 4. DC Characteristics

Symbol	Parameter	Rating			Unit
		Minimum	Typical	Maximum	
V_{DDA}	Absolute Analog Power Supply	-0.3		3.0	V
V_{INA}	Absolute Analog Input Voltage	-0.3		V_{DDA} + 0.3	V
V_{OUTA}	Absolute Analog Output Voltage	-0.3		V_{DDA} + 0.3	V
T_{STG}	Storage Temperature	0	25	65	°C
V_{DDA}	Analog Operating Power Supply	2.7	2.8	2.9	V
V_{DD}	Digital Operating Power Supply	2.3	2.5	2.8	V
V_{IN}	Operating Input Voltage	0		V_{DD}	V
I_{DDA}	Analog Supply Current (15 fps @ 72 MHz)		13		mA
I_{DD}	Digital Supply Current (15 fps @ 72 MHz)		38		mA
I_{IL}	Input Low Current	-1		1	μA
I_{IH}	Input High Current	-1		1	μA
I_{OZ}	Tri-state Leakage Current	-10		10	μA
C_{IN}	Input Capacitance		3		pF
C_{OUT}	Output Capacitance		3		pF
C_{BID}	Bi-directional Buffer Capacitance		3		pF

Table 4. DC Characteristics (continued)

Symbol	Parameter	Rating			Unit
		Minimum	Typical	Maximum	
V_{IL}	Input Low Voltage			0.3 * V_{DD}	V
V_{ILS}	Schmitt Input Low Voltage		1.1		V
V_{IH}	Input High Voltage	0.7 * V_{DD}			V
V_{IHS}	Schmitt Input High Voltage		1.8		V
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.0			V
R_L	Input Pull-up/down Resistance		50		KΩ

AC Characteristics

Table 5. AC Characteristics

Parameter	Minimum	Typical	Maximum	Condition	Pin
Setup time	No input pin needed for Setup and Hold time requirements.				
Hold time	SDA/SCL are subject to I2C protocol.				
Rise time			4.8 ns	50pf load	PCLK, HSYNC, VSYNC, DOUT[10:0]
Fall time			4.5 ns	50pf load	PCLK, HSYNC, VSYNC, DOUT[10:0]
Clock duty	40	50	60		%
DCG range		16			

Sensor Timing

The following sections discuss the timing requirements and formats of the ICM200E image sensor. Note that the timing requirements are relative to the pixel clock and the format depends on the subsampling mode.

Reset Timing

The reset signal RSTN must be asserted for more than two stable clock cycles. In addition, the VDD voltage ramp must be above 90% of its specified value for more than two stable clock cycles as shown in Figure 7.

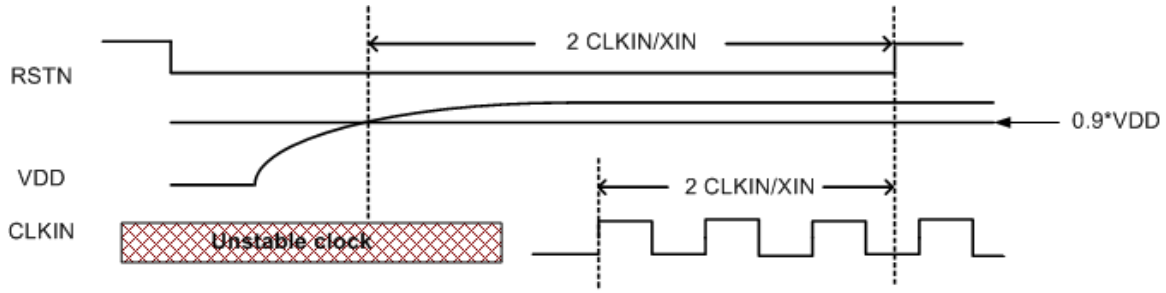

Figure 7. Reset Timing

Pixel Output Timing

The pixel data and timing output signals are DOUT [9:0], PCLK, VSYNC, and HSYNC. Data should be latched at the rising edge of the PCLK. The VSYNC and HSYNC signals are asserted and de-asserted at the falling edge of the PCLK. See Figure 8.

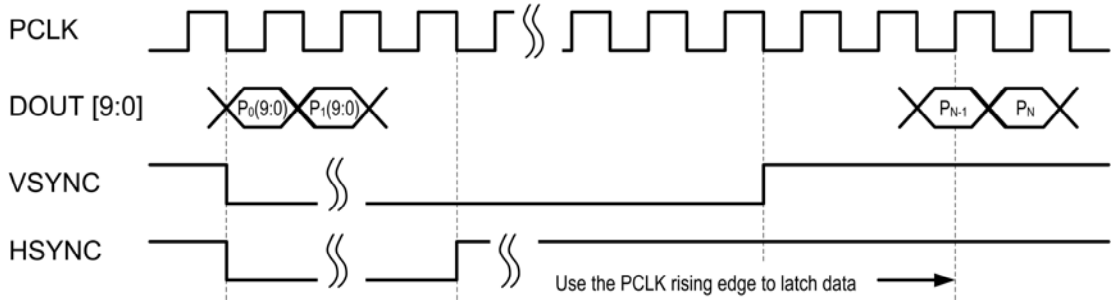

Figure 8. Pixel Output Timing

UXGA Mode Line Timing

For the default UXGA line timing, a line starts when the HSYNC signal is de-asserted. The HSYNC signal will be low for 64 PCLK clock cycles. At 100 PCLK clock cycles, DOUT [9:0] will output 10 cycles of dummy pixel data, followed by 1600 cycles of image data, and followed by another 10 dummy pixel data. Another 80 cycles later, the HSYNC signal will be de-asserted to start a new line. See Figure 9.

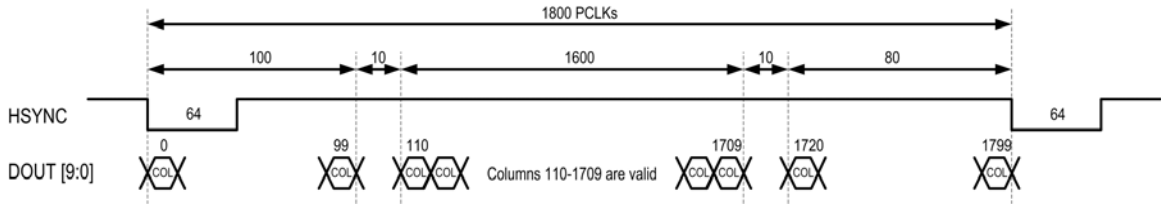

Figure 9. Default UXGA Line Timing for 1800 PCLKs

UXGA Mode Frame Timing

For the default UXGA frame timing, frame timing is derived from one line-time unit, which is 1800 PCLKs. The frame timing starts when the VSYNC signal is de-asserted. The VSYNC signal will be low for 3 line-time units. Sixteen line-time units from the start of the frame, DOUT [9:0] will output 10 lines of dummy pixel data, followed by 1200 lines of image data, and followed by another 10 lines of dummy pixel data. The VSYNC signal will be de-asserted again to start a new frame after another 64 line-time units. See Figure 10.

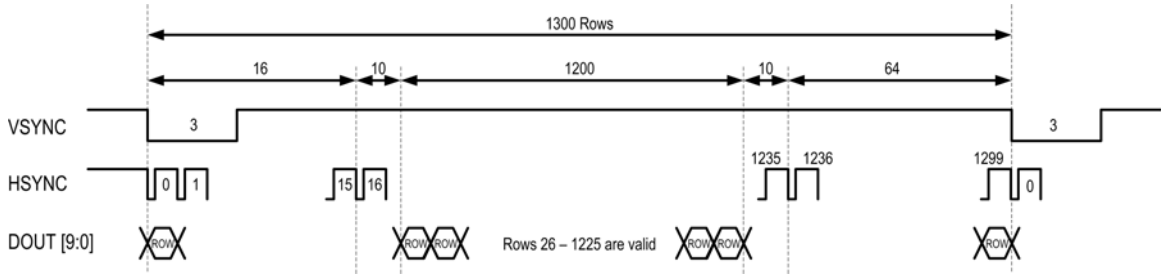

Figure 10. Default UXGA Frame Timing - Set Registers 0x4/0x15 to 0x0010 (H)

SVGA Subsampling Mode Timing

For the default SVGA line timing, a line starts when the HSYNC signal is de-asserted. The HSYNC signal will be low for 32 PCLK clock cycles. After 50 PCLK clock cycles, DOUT [9:0] will output six cycles of dummy pixel data followed by 800 cycles of image data, and followed by another 4 cycles of dummy pixel data. Another 40 cycles later, the HSYNC signal will be de-asserted to start a new line. See Figure 11.

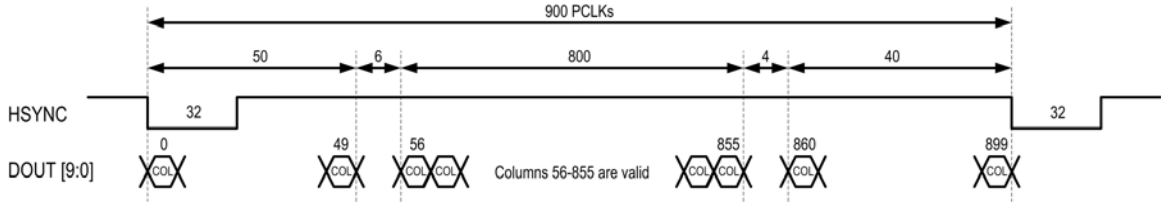

Figure 11. Default SVGA Line Timing for 900 PCLKs

SVGA Subsampling Mode Frame Timing

For the default SVGA frame timing, the timing unit for the frame is derived from one line-time unit, which are 900 PCLKs. Frame timing starts when the VSYNC signal is de-asserted. The VSYNC signal will be low for 3 line-time units. Eight line-time units from the start of the frame, DOUT [9:0] will output 6 lines of dummy pixel data, followed by 600 lines of image data, and followed by another 4 lines of dummy pixel data. The VSYNC signal will be de-asserted again to start a new frame after another 32 line-time units. See Figure 12.

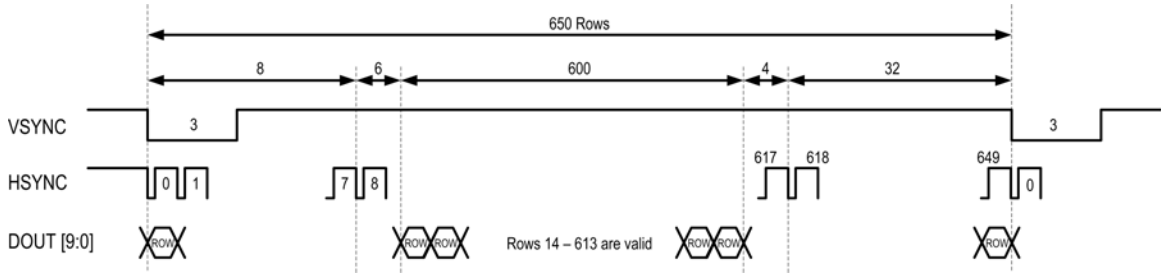

Figure 12. Default SVGA Frame Timing – Set Registers 0x14/0x15 to 0x0010 (H)

QSVGA Subsampling Mode Timing

For the default QSVGA line timing, a line starts when the HSYNC signal is de-asserted. The HSYNC signal will be low for 16 PCLK clock cycles. After 25 PCLK clock cycles, DOUT [9:0] will output 4 cycles of dummy pixel data followed by 400 cycles of image data, and followed by another 2 cycles of dummy pixel data. Another 19 cycles later, the HSYNC signal will be de-asserted to start a new line. See Figure 13.

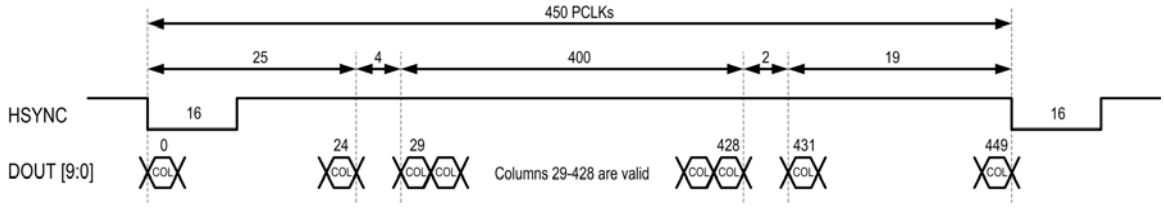

Figure 13. Default QSVGA Line Timing for 450 PCLKs

QSVGA Subsampling Mode Frame Timing

For the default QSVGA frame timing, the timing unit for the frame is derived from one line-time unit, which is 450 PCLKs. The frame timing starts when the VSYNC signal is de-asserted. The VSYNC signal will be low for 3 line-time units. Four line-time units from the start of the frame, DOUT [9:0] will output 3 lines of dummy pixel data followed by 300 lines of image data, and followed by another 2 lines of dummy pixel data. The VSYNC signal will be de-asserted again to start a new frame after another 15 line-time units. See Figure 14.

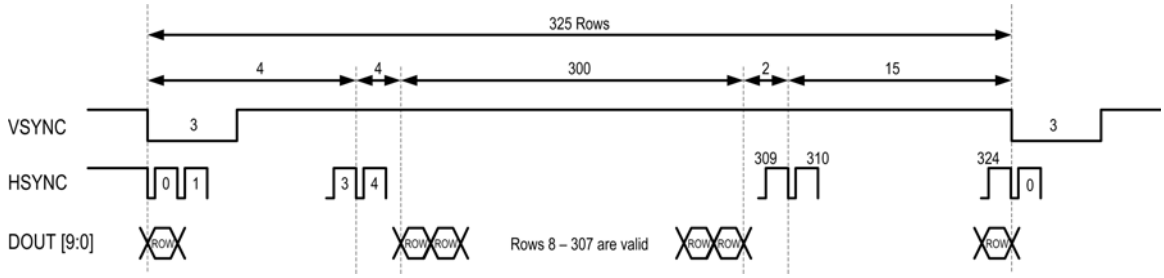

Figure 14. Default QSVGA Frame Timing - Set Registers 0x14/0x15 to 0x0010 (H)

Pixel Clock Duty Cycle

In the different frame rate modes (controlled by PART_CONTROL [6:4]), the duty cycle (high time / clock period) of the PCLK signal is described in the following table:

Table 6. Pixel Clock Duty Cycle

Frame Rate	Duty Cycle
30	50.0%
15	50.0%
10	50.0%
5	50.0%
4	53.3%
3	50.0%
2	50.0%
1	50.0%

Mechanical Information

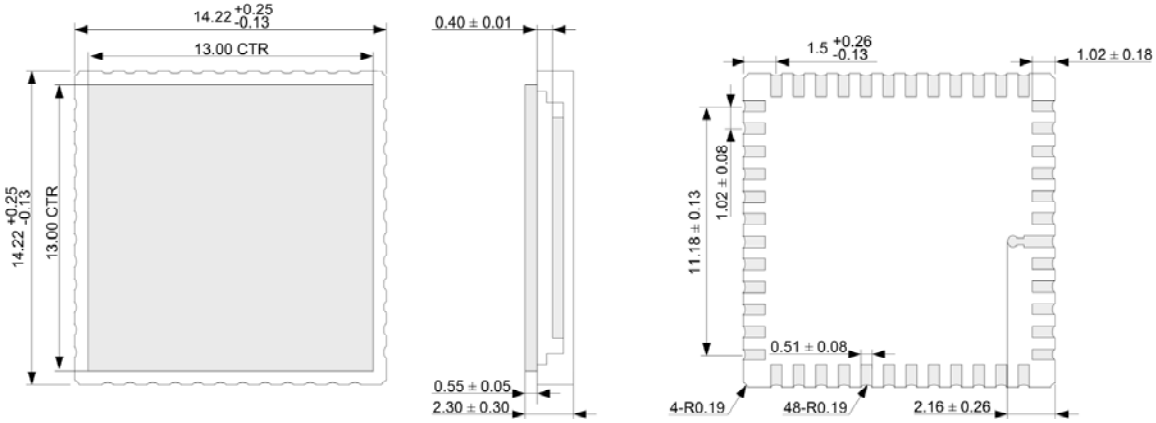

Figure 15. 48-Pin CLCC14.22 Mechanical Drawing

Ordering Information

Table 7. Ordering Information

Description	Part Order Number
Bare die in wafer form – no grinding, wafer thickness 725±25µm	ICM200ENAda
48-Pin CLCC14.22 package (for evaluation only)	ICM200Eca

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