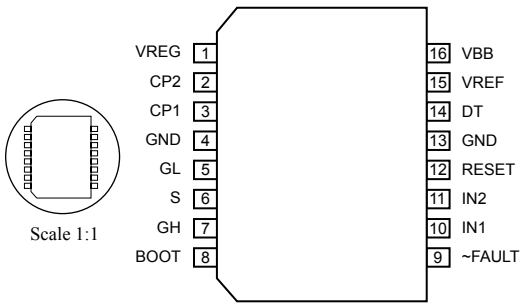
Preliminary Data Sheet
Subject to Change Without Notice
February 2, 2004

3946

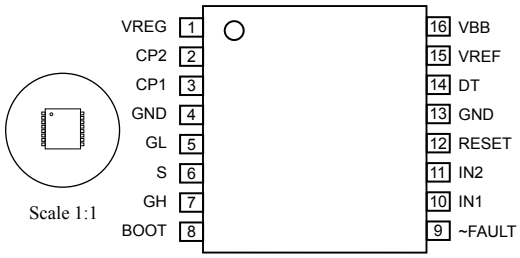
Data Sheet
29319.150f

Half-Bridge Power MOSFET Controller

A3946KLB SOIC



A3946KLP TSSOP with Exposed Thermal Pad



ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} ..... **60 V**
Logic Inputs .....**–0.3 V to 6.5 V**
Pin S……..... **–4 V to 60 V**
Pin GH .....**–4 V to 75 V**
Pin BOOT….. .....**–0.6 V to 75 V**
Pin DT ..... **V_{REF}**
Package Thermal Resistance, R_{JA}
A3946KLB..... **48°C/W**[1]
A3946KLB..... **38°C/W**[2]
A3946KLP ..... **44°C/W**[1]
A3946KLP ..... **34°C/W**[2]
Operating Temperature Range, T_A .. **–40°C to +135°C**
Junction Temperature, T_J.....**+150°C**
Storage Temperature Range, T_S....**-55°C to +150°C**

Notes:
1. Measured on a two-sided PCB with 3 in.^{2} of 2 oz. copper.
2. Measured on JEDEC standard High-K board.

The A3946 is designed specifically for applications that require high power unidirectional dc motors, three-phase brushless dc motors, or other inductive loads. The A3946 provides two high-current gate drive outputs that are capable of driving a wide range of power N-channel MOSFETs. The high-side gate driver switches an N-channel MOSFET that controls current to the load, while the low-side gate driver switches an N-channel MOSFET as a synchronous rectifier.

A bootstrap capacitor provides the above-battery supply voltage required for N-channel MOSFETs. An internal charge pump for the high side allows for dc (100% duty cycle) operation of the half-bridge.

The A3946 is available in a choice of two power packages: a 16-lead SOIC with copper batwing power tab (part number suffix *LB*), and a 16-lead TSSOP with exposed thermal pad (suffix *LP*).

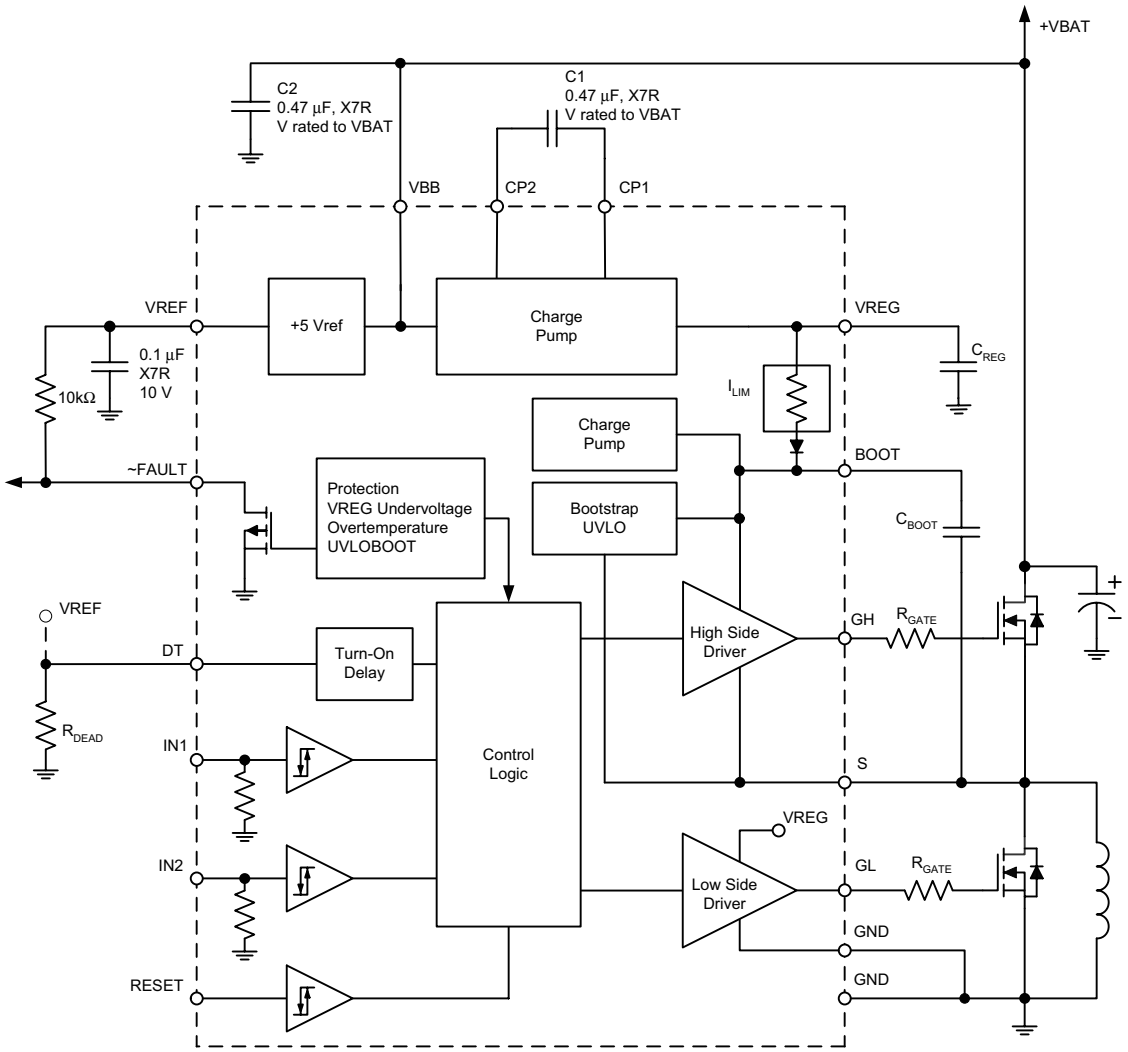
FEATURES

- On-chip charge pump for 7 V minimum input supply voltage
- High-current gate drive for driving a wide range of N-channel MOSFETs
- Bootstrapped gate drive with charge pump for 100% duty cycle
- Overtemperature protection
- Undervoltage protection
- –40ºC to 135ºC ambient operation

Always order by complete part number:

Part Number	Package
A3946KLB	16-Lead SOIC; Copper Batwing Power Tab
A3946KLP	16-Lead TSSOP; Exposed Thermal Pad

Functional Block Diagram



Control Logic Table

IN1	IN2	DT Pin	RESET	GH	GL	Function
X	X	X	0	Z	Z	Sleep mode
0	0	R_{DEAD} - GND	1	L	H	Low-side MOSFET ON following dead time
0	1	R_{DEAD} - GND	1	L	L	All OFF
1	0	R_{DEAD} - GND	1	L	L	All OFF
1	1	R_{DEAD} - GND	1	H	L	High-side MOSFET ON following dead time
0	0	VREF	1	L	L	All OFF
0	1	VREF	1	L	H	Low-side MOSFET ON
1	0	VREF	1	H	L	High-side MOSFET ON
1	1	VREF	1	H	H	High-side and low-side MOSFETs ON

ELECTRICAL CHARACTERISTICS at T_J = –40 to +150°C, V_{BB} = 7 to 60 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
V_{BB} Quiescent Current	I_{VBB}	RESET = High, Outputs Low	—	3	6	mA
		RESET = Low	—	—	10	µA
VREG Output Voltage	V_{REG}	V_{BB} > 7.75 V, I_{reg} = 0 mA to 15 mA	12.0	13	13.5	V
		V_{BB} = 7 V to 7.75 V, I_{reg} = 0 mA to 15 mA	11.0	—	13.5	V
Gate Output Drive						
Turn On Time	t_{rise}	C_{LOAD} = 3300 pF, 20% to 80%	—	60	100	ns
Turn Off Time	t_{fall}	C_{LOAD} = 3300 pF, 80% to 20%	—	40	80	ns
Pullup On Resistance	R_{DSUP}	T_j = 25°C	—	4	—	Ω
		T_j = 135°C	—	6	—	Ω
Pulldown On Resistance	R_{DSDOWN}	T_j = 25°C	—	2	—	Ω
		T_j = 135°C	—	3	—	Ω
Short Circuit Current – Source	—	t_{pw} < 10 µs	800	—	—	mA
Short Circuit Current – Sink	—	t_{pw} < 10 µs	1000	—	—	mA
GH Output Voltage	V_{GH}	t_{pw} < 10 µs, Bootstrap Capacitor fully charged	V_{REG} – 1.5	—	—	V
GL Output Voltage	V_{GL}	—	V_{REG} – 0.2	—	—	V
Timing						
Dead Time (Delay from Turn Off to Turn On)	t_{DT}	R_{dead} = 5 kΩ	200	350	500	ns
		R_{dead} = 100 kΩ	5	6	7	µs
Turn Off Propagation Delay	t_{OFF}	Input change to unloaded gate output change	—	90	150	ns
Turn On Propagation Delay	t_{ON}	Dead time disabled	—	90	150	ns

Allegro MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

ELECTRICAL CHARACTERISTICS at T_J = –40 to +150°C, V_{BB} = 7 to 60 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Protection						
VREG Undervoltage Turn On	V_{REGON}		8.75	9.25	9.75	V
VREG Undervoltage Turn Off	V_{REGOFF}		8.0	8.5	9.0	V
BOOT Undervoltage Turn On	V_{BSON}		8	8.75	9.5	V
BOOT Undervoltage Turn Off	V_{BSOFF}		7.25	8.0	8.75	V
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	—	170	—	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	—	15	—	°C
Logic						
Input Current	$I_{IN(1)}$	IN1 V_{IN} / IN2 V_{IN} = 2.0 V	—	40	100	µA
	$I_{IN(0)}$	IN1 V_{IN} / IN2 V_{IN} = 0.8 V	—	16	40	µA
		RESET pin only	—	—	1	µA
Logic Input Voltage	$V_{IN(1)}$	IN1 / IN2 logic high	2.0	—	—	V
		RESET logic high	2.2	—	—	V
	$V_{IN(0)}$	Logic low	—	—	0.8	V
Logic Input Hysteresis	—	All digital inputs	100	—	300	mV
Fault Output	V_{ol}	I = 1 mA, fault asserted	—	—	400	mV
	V_{oh}	V = 5 V	—	—	1	µA

Allegro MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

Functional Description

VREG. A 13 V output from the on-chip charge pump, used to power the low-side gate drive circuit directly, provides the current to charge the bootstrap capacitors for the high-side gate drive.

The VREG capacitor, C_{REG}, must supply the instantaneous current to the gate of the low-side MOSFET. A 10 µF, 25 V capacitor should be adequate. This capacitor can be either electrolytic or ceramic (X7R).

Diagnostics. A fault output, ~FAULT, is pulled low upon either an undervoltage condition on the VREG pin, an undervoltage on the BOOT pin, or when the junction temperature is greater than 170ºC.

An overtemperature event signals the ~FAULT pin, but does not disable any circuitry. It is up to the user to turn off the device, to prevent both overtemperature damage to the chip, and unpredictable device operation.

The VREG undervoltage fault and the overtemperature fault are latched. The method for clearing the faults is to pulse the RESET pin for a short period. A pulse of 1 to 10 µs clears the fault latch and releases the ~FAULT output flag. On the rising edge of the RESET pulse, ~FAULT returns to its proper state.

The BOOT pin undervoltage monitor fault is NOT latched. Under normal operating conditions, where both GH and GL are driven off, such as in a 3-phase application, the bootstrap capacitor is discharged and the ~FAULT pin is flagged. In this case, the bootstrap capacitor must be charged before a proper high-side turn-on event can occur.

Gate Protection. The voltage from the BOOT pin, relative to S, is monitored to ensure adequate gate drive for the high-side drive. The GH pin is held off whenever the voltage is below the threshold.

Proper gate drive for the low-side is ensured by the VREG monitor. If VREG is below the threshold, as in a power-up condition, both GH and GL are held off.

Charge Pump. The A3946 is designed to accommodate a wide range of power supply voltages. The charge pump output, VREG, is regulated to 13 V nominally.

Sleep Mode/Power Up. The sleep mode allows minimum draw from the VBB line. All of the internal circuitry is disabled. When coming out of sleep mode (RESET high), the protection logic ensures that the gate drive outputs are off until the charge pump reaches proper operating conditions. The charge pump should stabilize as indicated by the following formula:

$$t = C_{REG} (13\ V / 50\ mA) = 2.6\ ms$$

When coming out of RESET mode, wait this duration before starting the first bootstrap charge cycle.

Dead Time. The analog input pin DT sets the delay to turn on the high- or low-side gate outputs. When instructed to turn off, the gate outputs change after an short internal propagation delay (90 ns typical). The dead time controls the time between this turn-off and the turn-on of the appropriate gate. The duration can be adjusted within the range of 350 ns and 6000 ns using the following formula:

$$t_{DEAD} = (R_{DEAD} / 16.7\ e^{9}) + 50\ ns$$

If the DT pin is left open, it defaults to 12 µs.

Control Logic. Two different methods of control are possible with the A3946. When a resistor is connected from DT to ground, a single-pin PWM scheme is utilized by shorting IN1 with IN2. If a very slow turn-on is required (greater than 6 µs), the two input pins can be hooked-up individually to allow the dead times to be as long as needed.

The dead time circuit can be disabled by tying the DT pin to VREF. This disables the turn-on delay and allows direct control of each MOSFET gate via two control lines. This is shown in the Control Logic table, on page 2.

Top-Off Charge Pump. An internal charge pump allows 100% duty cycle operation of the high-side MOSFET. This is a low-current trickle charge pump, and is only operated after a high-side has been signaled to turn on. A small amount of bias current (< 200 µA) is drawn from the BOOT pin to operate the floating high-side circuit. The charge pump simply provides enough drive to ensure that the gate voltage does not droop due to this bias supply current. The charge required for initial turn-on of the high-side gate must be supplied by bootstrap capacitor charge cycles. This is described in the section Application Information.

VREF. Vref is used for the internal logic circuitry and is not intended as an external power supply. However, the VREF pin can source up to 4 mA of current. The 0.1 µF capacitor is needed for decoupling.

Allegro MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

Application Information

Bootstrap Capacitor Selection. C_{BOOT} must be correctly selected to ensure proper operation of the device. If too large, time is wasted charging the capacitor, with the result being a limit on the maximum duty cycle and PWM frequency. If the capacitor is too small, the voltage drop can be too large at the time the charge is transferred from the C_{BOOT} to the MOSFET gate.

To keep the voltage drop small:

$$Q_{BOOT} >> Q_{GATE}$$

where a factor in the range of 10 to 20 is reasonable. Using 20 as the factor:

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

and

$$C_{BOOT} = Q_{GATE} \times 20 / V_{BOOT}$$

The voltage drop on the BOOT pin, as the MOSFET is being turned on, can be approximated by:

$$Delta\_v = Q_{GATE} / C_{BOOT}$$

For example, given a gate charge, Q_{GATE}, of 160 nC, and the typical BOOT pin voltage of 12 V, the value of the Boot capacitor, C_{BOOT}, can be determined by:

$$C_{BOOT} = (160\ nC \times 20) / 12\ V \approx 0.266\ \mu F$$

Therefore, a 0.22 µF ceramic (X7R) capacitor can be chosen for the Boot capacitor.

In that case, the voltage drop on the BOOT pin, when the high-side MOSFET is turned on, is:

$$Delta\_v = 160\ nC / 0.22\ \mu F = 0.73\ V$$

Bootstrap Charging. It is good practice to ensure that the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested.

The time required to charge the capacitor can be approximated by:

$$t_{CHARGE} = C_{BOOT} (Delta\_v / 100\ mA)$$

At power-up and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, Delta_v can be considered to be the full high-side drive voltage, 12 V. Otherwise, Delta_v is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the S pin is pulled low, via a GL PWM cycle, and current flows from VREG through the internal bootstrap diode circuit to C_{BOOT}.

Power Dissipation. For high ambient temperature applications, there may be little margin for on-chip power consumption. Careful attention should be paid to ensure that the operating conditions allow the A3946 to remain in a safe range of junction temperature.

The power consumed by the A3946 can be estimated as:

$$P\_total = Pd\_bias + Pd\_cpump + Pd\_switching\_loss$$

where:

$Pd\_bias = V_{BB} \times I_{VBB}$, typically 3 mA,

and

$Pd\_cpump = (2V_{BB} - V_{REG})\ I_{AVE}$, for $V_{BB} < 15$ V, or

$Pd\_cpump = (V_{BB} - V_{REG})\ I_{AVE}$, for $V_{BB} > 15$ V,

in either case, where

$$I_{AVE} = Q_{GATE} \times 2 \times f_{PWM}$$

and

$Pd\_switching\_loss = Q_{GATE} \times V_{REG} \times 2 \times f_{PWM}$ Ratio,

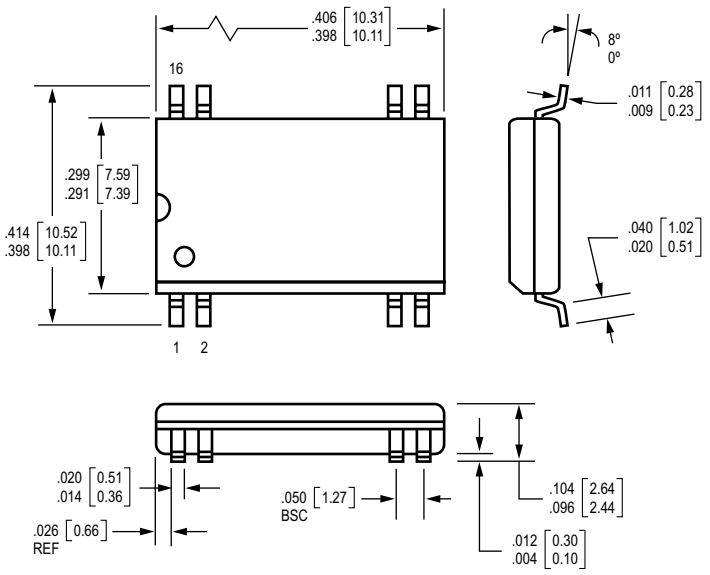
where

$$Ratio = 10\ \Omega / (R_{GATE} + 10\ \Omega).$$

Allegro MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

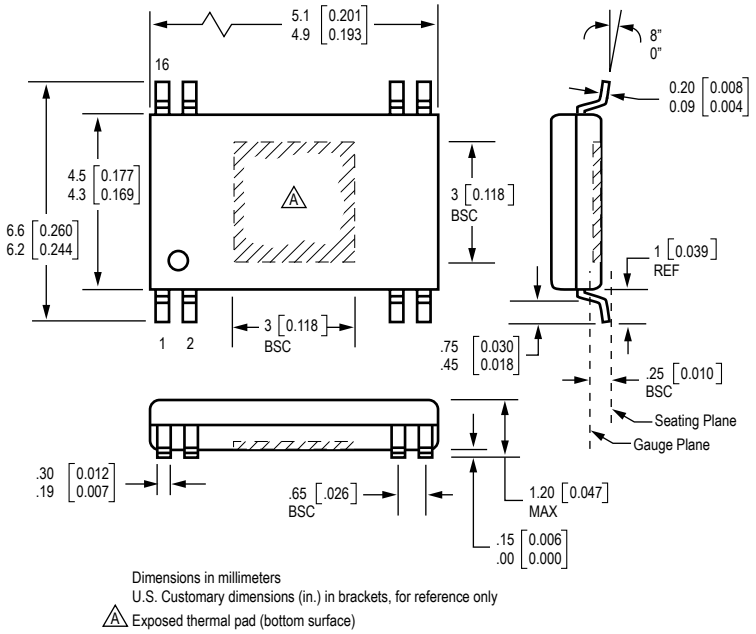
Pin Name	Pin Description	SOIC-16 (A3946KLB)	TSSOP-16 (A3946KLP)
VREG	Gate drive supply.	1	1
CP2	Charge pump capacitor, positive side. When not using the charge pump, leave this pin open.	2	2
CP1	Charge pump capacitor, negative side. When not using the charge pump, leave this pin open.	3	3
GND	External ground.	4	4
GL	Low-side gate drive output for external MOSFET driver. External series gate resistor can be used to control slew rate seen at the power driver gate, thereby controlling the di/dt and dv/dt of the S pin output.	5	5
S	Directly connected to the load terminal. The pin is also connected to the negative side of the bootstrap capacitor and negative supply connection for the floating high-side drive.	6	6
GH	High-side gate drive output for N-channel MOSFET driver. External series gate resistor can be used to control slew rate seen at the power driver gate, thereby controlling the di/dt and dv/dt of the S pin output.	7	7
BOOT	High-side connection for bootstrap capacitor, positive supply for the high-side gate drive.	8	8
~FAULT	Diagnostic output, open drain. Low during a fault condition.	9	9
IN1	Logic control.	10	10
IN2	Logic control.	11	11
RESET	Logic control input. When RESET = 0, the chip is in a very low power sleep mode.	12	12
GND	External ground.	13	13
DT	Dead Time. Connecting a resistor to GND sets the turn-on delay to prevent shoot-through. Forcing this input high disables the dead time circuit and changes the logic truth table.	14	14
VREF	5 V internal reference decoupling terminal.	15	15
VBB	Supply Input.	16	16

A3946KLB SOIC



Webbed lead frame. Leads 4 and 13 are joined together within the device package.

A3946KLP TSSOP with Exposed Thermal Pad



NOTES:
1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 49 devices or add "TR" to part number for tape and reel.

Allegro MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

3946
Half-Bridge Power MOSFET Controller

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro products are not authorized for use as critical components in life-support devices or systems without express written approval.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copyright©2003, 2004 AllegroMicrosystems, Inc.

Allegro® MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.