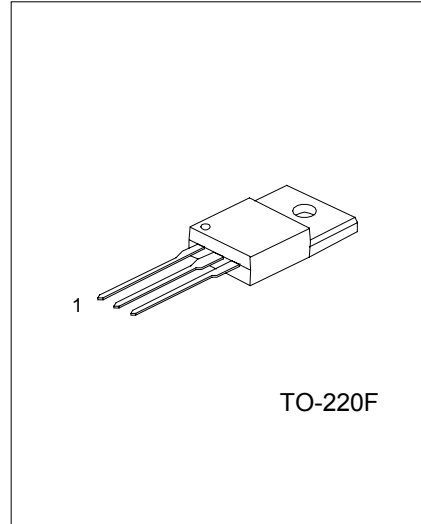
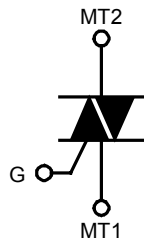


TRIACS

DESCRIPTION

Glass passivated , sensitive gate triacs in a full plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

SYMBOL



1:MT1 2:MT2 3:GATE

ABSOLUTE MAXIMUM RATINGS (Tj=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltages UT138FE-5 UT138FE-6 UT138FE-8	V _{DRM}	500* 600* 800	V
RMS On-state Current (Full sine wave; T _{hs} ≤ 56°C)	I _{T(RMS)}	12	A
Non-repetitive Peak. On-State Current (Full sine wave, T _j =125°C prior to surge, with reapplied V _{DRM(max)})	I _{TSM}	90 100	A
		t=20ms t=16.7ms	
I ² t For Fusing (t=10ms)	I ² t	40	A ² s
Repetitive Rate of Rise of On-state Current after Triggering (I _{TM} =20A, I _G =0.2A, dI _G /dt=0.2A/μs)	dI _T /dt	50 50 50 10	A/μs
		T2+ G+ T2+ G- T2- G- T2- G+	
Peak Gate Voltage	V _{GM}	5	V
Peak Gate Current	I _{GM}	2	A
Peak Gate Power	P _{GM}	5	W
Average Gate Power (over any 20 ms period)	P _{G(AV)}	0.5	W
Operating Junction Temperature	T _j	125	°C
Storage Temperature	T _{stg}	-40~150	°C

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15A/μs.

ISOLATION LIMITING VALUE & CHARACTERISTIC (T_{HS}=25°C, unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Repetitive peak voltage from all three terminals to external heatsink (R.H. ≤ 65%, clean and dustfree)	V _{isol}			1500	V
Capacitance from MT2 to external heatsink (f=1MHz)	C _{isol}		12		pF

THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance, Junction to heatsink (full or half cycle) with heatsink compound without heatsink compound	R _{thj-hs}			4.0 5.5	K/W
Thermal Resistance, Junction to Ambient In free air	R _{thj-a}		55		K/W

STATIC CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gate Trigger Current	I _{GT}	V _D =12V, I _T =0.1A T2+ G+ T2+ G- T2- G- T2- G+		2.5 4.0 5.0 11	10 10 10 25	mA
Latching Current	I _L	V _D =12V, I _{GT} =0.1A T2+ G+ T2+ G- T2- G- T2- G+		3.2 16 4.0 5.5	30 40 30 40	mA
Holding Current	I _H	V _D =12V, I _{GT} =0.1A		4.0	30	mA
On-State Voltage	V _T	I _T =15A		1.4	1.65	V
Gate Trigger Voltage	V _{GT}	V _D =12V, I _T =0.1A V _D =400V, I _T =0.1A, T _J =125°C	0.25	0.7	1.5	V
Off-state Leakage Current	I _D	V _D =V _{DRM(max)} , T _J =125°C		0.1	0.5	mA

DYNAMIC CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Critical Rate Of Rise Of Off-State Voltage	dV _D /dt	V _{DM} =67% V _{DRM(max)} , T _J =125°C Exponential waveform, Gate open circuit		50		V/μs
Gate Controlled Turn-on Time	t _{gt}	I _{TM} =16A, V _D =V _{DRM(max)} , I _G =0.1A, dI _G /dt=5A/μs		2		μs

TYPICAL CHARACTERISTICS

Figure 1. Maximum on-state Dissipation, P_{tot} vs rms On-state Current, $I_T(RMS)$, Where α = conduction Angle.

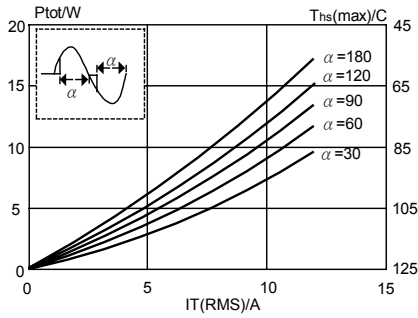


Figure 4. Maximum Permissible RMS Current $I_T(RMS)$ vs heatsink Temperature T_{hs}

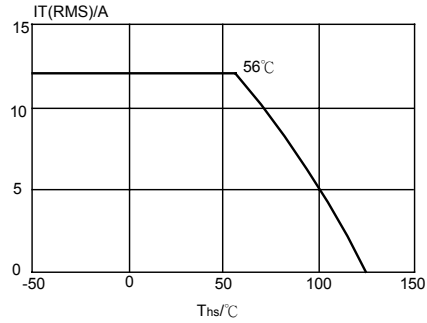


Figure 2. Maximum Permissible Non-repetitive Peak On-state Current I_{TSM} , vs Pulse Width t_p , for Sinusoidal Currents, $t_p \leq 20ms$

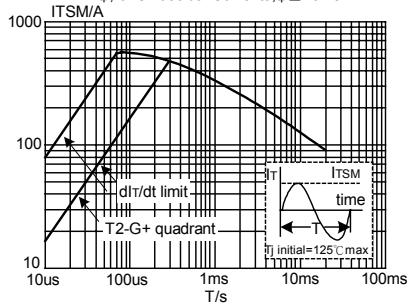


Figure 5. Maximum Permissible Repetitive rms on-state Current $I_T(RMS)$, vs Surge Duration, for Sinusoidal Currents, $f=50Hz; T_{hs} \leq 56^\circ C$

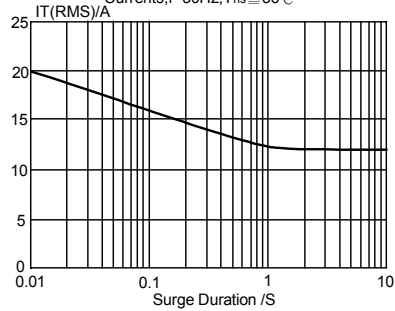


Figure 3. Maximum Permissible Non-Repetitive peak on-state Current I_{TSM} , vs Number of Cycles, for Sinusoidal Currents, $f=50Hz$

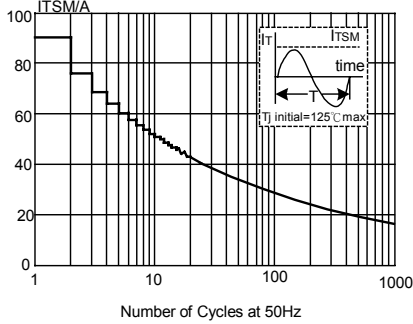
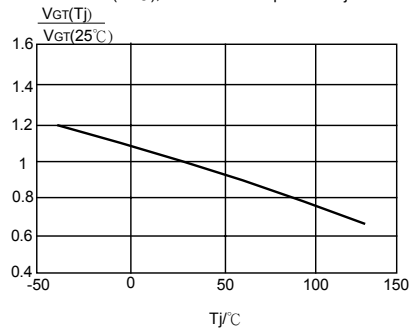
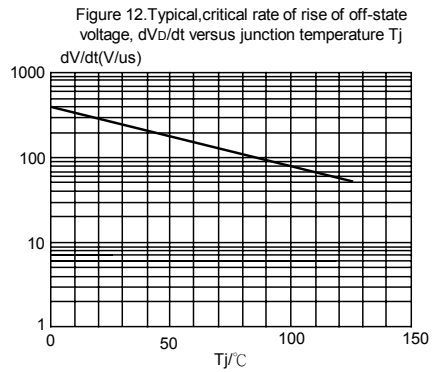
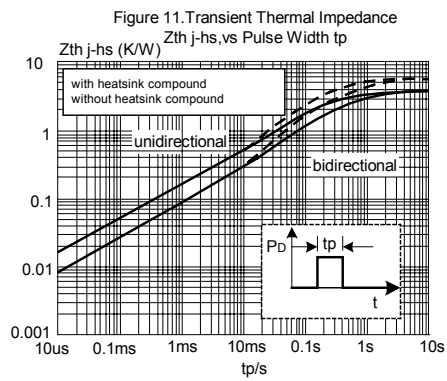
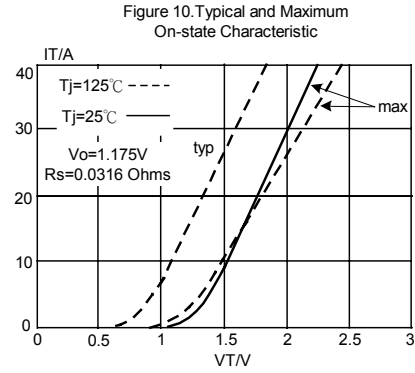
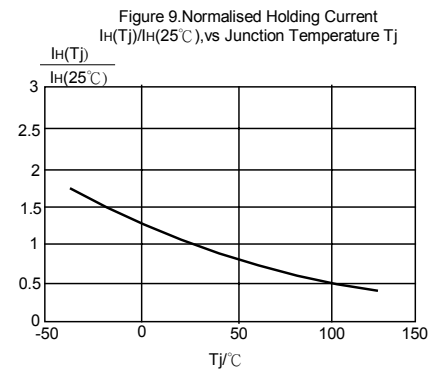
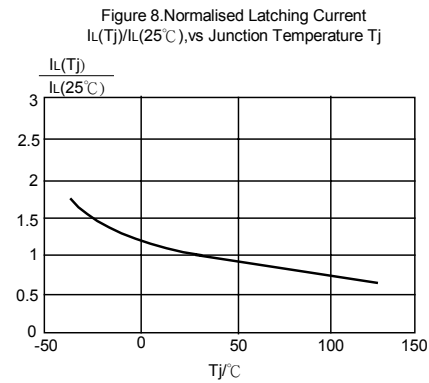
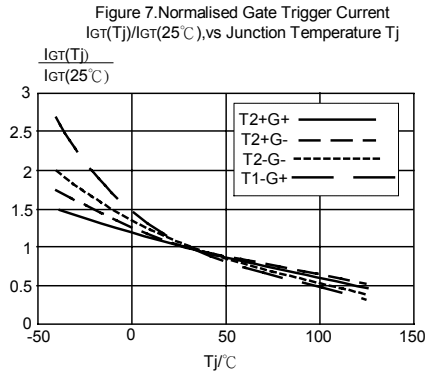


Figure 6. Normalised Gate Trigger Voltage $V_{GT}(T_j)/V_{GT}(25^\circ C)$, vs Junction Temperature T_j





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