

MC10H186

Hex D Master-Slave Flip-Flop with Reset

Description

The MC10H186 is a hex D type flip-flop with common reset and clock lines. This MECL 10H™ part is a functional/pinout duplication of the standard MECL 10K™ family part, with 100% improvement in clock toggle frequency and propagation delay and no increase in power-supply current.

Features

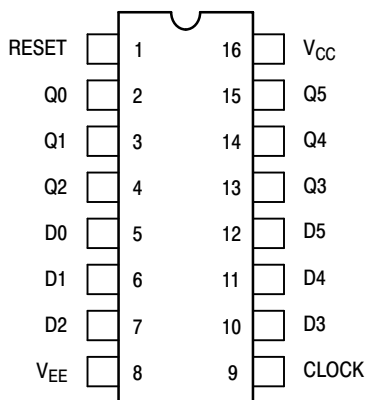
- Propagation Delay, 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K Compatible
- Pb-Free Packages are Available*

CLOCKED TRUTH TABLE

R	C	D	Q _{n+1}
L	L	X	Q _n
L	H*	L	L
L	H*	H	H
H	L	X	L

* A clock H is a clock transition from a low to a high state.

DIP PIN ASSIGNMENT



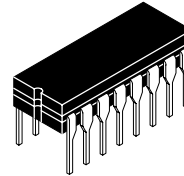
Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



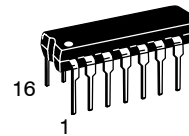
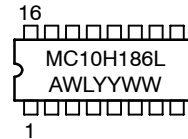
ON Semiconductor®

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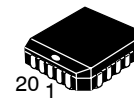
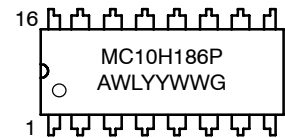
MARKING DIAGRAMS*



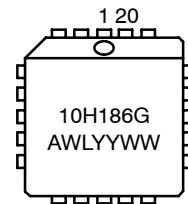
**CDIP-16
L SUFFIX
CASE 620A**



**PDIP-16
P SUFFIX
CASE 648**



**PLCC-20
FN SUFFIX
CASE 775**



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MC10H186

Table 1. MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V _{EE}	Power Supply (V _{CC} = 0)	-8.0 to 0	Vdc
V _I	Input Voltage (V _{CC} = 0)	0 to V _{EE}	Vdc
I _{out}	Output Current – Continuous – Surge	50 100	mA
T _A	Operating Temperature Range	0 to +75	°C
T _{stg}	Storage Temperature Range – Plastic – Ceramic	-55 to +150 -55 to +165	°C °C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Table 2. ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note 1.)

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
I _E	Power Supply Current	-	121	-	110	-	121	mA
I _{inH}	Input Current High Pins 5,6,7,10,11,12 Pin 9 Pin 1	-	430 670 1250	-	265 420 765	-	265 420 765	μA
I _{inL}	Input Current Low	0.5	-	0.5	-	0.3	-	μA
V _{OH}	High Output Voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V _{OL}	Low Output Voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V _{IH}	High Input Voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V _{IL}	Low Input Voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

Table 3. AC PARAMETERS

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
t _{pd}	Propagation Delay	0.7	3.0	0.7	3.0	0.7	3.0	ns
t _{set}	Set-up Time	1.5	-	1.5	-	1.5	-	ns
t _{hold}	Hold Time	1.0	-	1.0	-	1.0	-	ns
t _r	Rise Time	0.7	2.6	0.7	2.6	0.7	2.6	ns
t _f	Fall Time	0.7	2.6	0.7	2.6	0.7	2.6	ns
f _{tog}	Toggle Frequency	250	-	250	-	250	-	MHz
t _{rr}	Reset Recovery Time (t ₁₋₉₊)	3.0	-	3.0	-	3.0	-	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

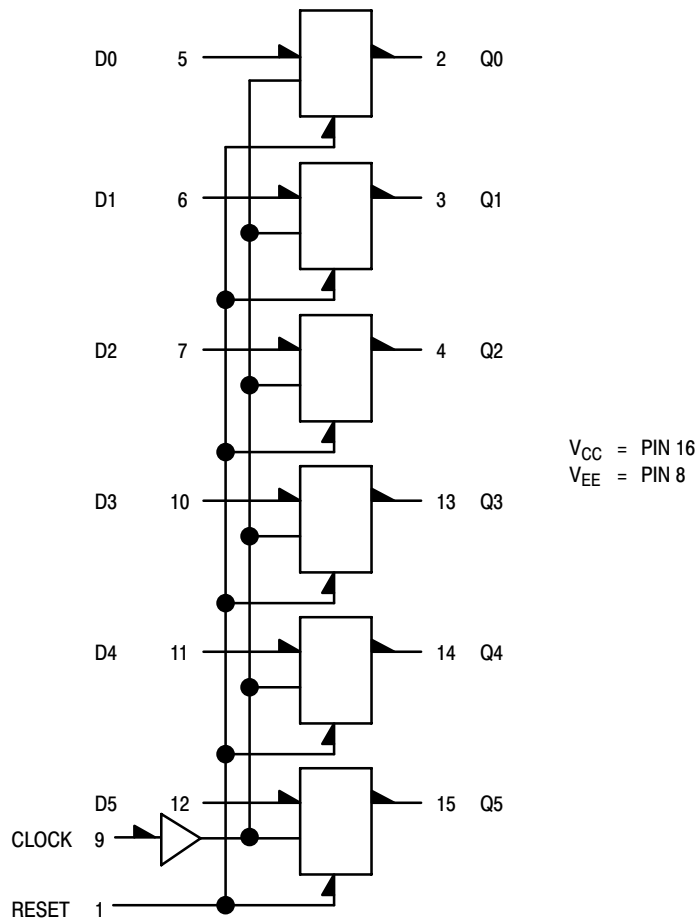
MC10H186

APPLICATION INFORMATION

The MC10H186 contains six high-speed, master slave type “D” flip-flops. Data is entered into the master when the clock is low. Master-to-slave data transfer takes place on the positive-going Clock transition. Thus outputs may change only on a positive-going Clock transition. A change

in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. A common Reset is included in this circuit. **THE RESET ONLY FUNCTIONS WHEN THE CLOCK IS LOW.**

LOGIC DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping [†]
MC10H186FN	PLLC-20	46 Units / Rail
MC10H186FNG	PLLC-20 (Pb-Free)	46 Units / Rail
MC10H186FNR2	PLLC-20	500 / Tape & Reel
MC10H186FNR2G	PLLC-20 (Pb-Free)	500 / Tape & Reel
MC10H186L	CDIP-16	25 Unit / Rail
MC10H186P	PDIP-16	25 Unit / Rail
MC10H186PG	PDIP-16 (Pb-Free)	25 Unit / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC10H186

PACKAGE DIMENSIONS

20 LEAD PLLC
CASE 775-02
ISSUE E



NOTES:

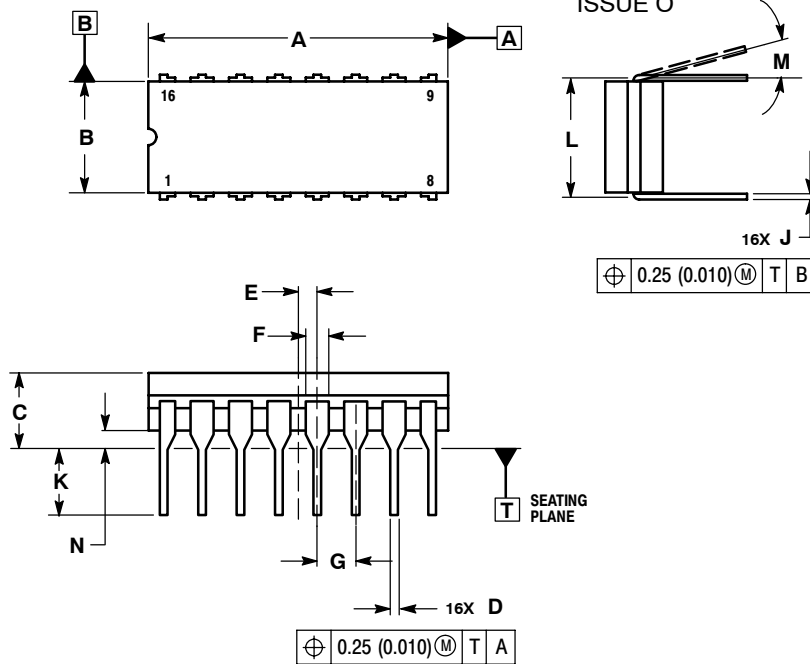
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSIONS IN INCHES.
3. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
4. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
5. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
6. DIMENSIONS IN THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°		10°	
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

MC10H186

PACKAGE DIMENSIONS

CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620A-01 ISSUE O

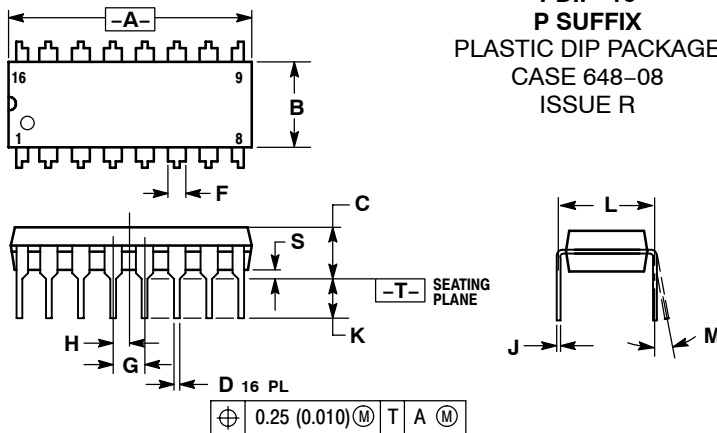


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. THIS DRAWING REPLACES OBSOLETE CASE OUTLINE 620-10.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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