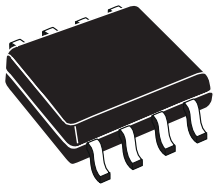
STS01DTP06

Dual NPN-PNP complementary Bipolar transistor

General features

$V_{CE(sat)}$	h_{FE}	I_C
0.35V	>100	1A

- High gain
- Low $V_{CE(sat)}$
- Simplified circuit design
- Reduced component count

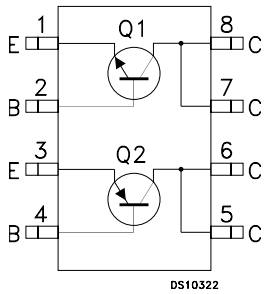


SO-8

Applications

- Push-Pull or Totem-Pole configuration
- MOSFET and IGBT gate driving
- Motor, relay and solenoid driving

Internal schematic diagram



Description

The STS01DTP06 is a Hybrid dual NPN-PNP complementary power bipolar transistor manufactured by using the latest low voltage planar techlogy. The STS01DTP06 is housed in dual island SO-8 package with separated terminals for higher assembly flexibility, specifically recommended to be used in Push-Pull or Totem Pole configuration as post IGBTs and MOSFETs driver.

Order codes

Part Number	Marking	Package	Packing
STS01DTP06	S01DTP06	SO-8	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		NPN	PNP	
V_{CBO}	Collector-base voltage (I_E = 0)	60	-60	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	30	-30	V
V_{EBO}	Emitter-base voltage (I_C = 0)	5	-5	V
I_C	Collector current	3	-3	A
I_{CM}	Collector peak current (t_P < 5ms)	6	-6	A
I_B	Base current	1	-1	A
I_{BM}	Base peak current (t_P < 1ms)	2	-2	A
P_{tot}	Total dissipation at T_c = 25°C single	2		W
P_{tot}	Total dissipation at T_c = 25°C couple	1.6		W
T_{stg}	Storage temperature	-65 to 150		°C
T_J	Max. operating junction temperature	150		°C

Table 2. Thermal data

Symbol	Parameter		Value	Unit
$R_{thj\text{-}amb}$ 1	Thermal resistance junction-ambient (Single operation)	Max	62.5	°C/W
$R_{thj\text{-}amb}$ 1	Thermal resistance junction-ambient (Dual operation)	Max	78	°C/W

1 *When mounted on 1 inch square pad of 2 oz. copper, t ≤10 sec.*

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified)

Table 3. Q1-NPN transistor electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cut-off current (I_E = 0)	V_{CB} = 60V			0.1	µA
I_{CEO}	Collector cut-off current (I_B = 0)	V_{CE} = 30V			1	µA
I_{EBO}	Emitter cut-off current (I_C = 0)	V_{EB} = 5V			1	µA
$V_{(BR)CEO}$ (1)	Collector-emitter breakdown voltage (I_B = 0)	I_C = 10mA	30			V
$V_{CE(sat)}$ (1)	Collector-emitter saturation voltage	I_C = 1A I_B = 10mA I_C = 2A I_B = 100mA		0.35	1 0.7	V V
$V_{BE(sat)}$ (1)	Base-emitter saturation voltage	I_C = 1A I_B = 10mA		0.85	1.1	V
h_{FE} (1)	DC current gain	I_C = 1A V_{CE} = 2V I_C = 3A V_{CE} = 2V	100 30			

1. Pulsed: Pulse duration = 300 ms, duty cycle ≤ 1.5 %

(T_{case} = 25°C unless otherwise specified)

Table 4. Q2-PNP transistor electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cut-off current (I_E = 0)	V_{CB} = -60V			-0.1	µA
I_{CEO}	Collector cut-off current (I_B = 0)	V_{CE} = -30V			-1	µA
I_{EBO}	Emitter cut-off current (I_C = 0)	V_{EB} = -5V			-1	µA
$V_{(BR)CEO}$ (1)	Collector-emitter breakdown voltage (I_B = 0)	I_C = -10mA	-30			V
$V_{CE(sat)}$ (1)	Collector-emitter saturation voltage	I_C = -1A I_B = -10mA I_C = -2A I_B = -100mA		-0.35	-1 -0.7	V V

Table 4. Q2-PNP transistor electrical characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{BE(sat)}$ (1)	Base-emitter saturation voltage	I_C = -1A	I_B = -10mA		-0.85	-1.1	V
h_{FE} (1)	DC current gain	I_C = -1A I_C = -3A	V_{CE} = -2V V_{CE} = -2V	100 30			

1. Pulsed: Pulse duration = 300 ms, duty cycle ≤ 1.5 %

2.1 Electrical characteristics (curve)

Figure 1. Reverse biased area Q1 NPN transistor

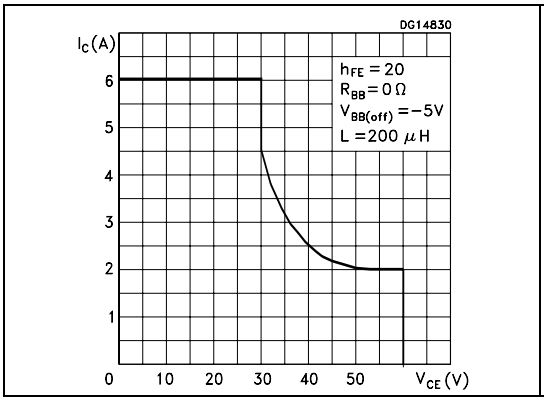


Figure 2. DC current gain Q1 NPN transistor

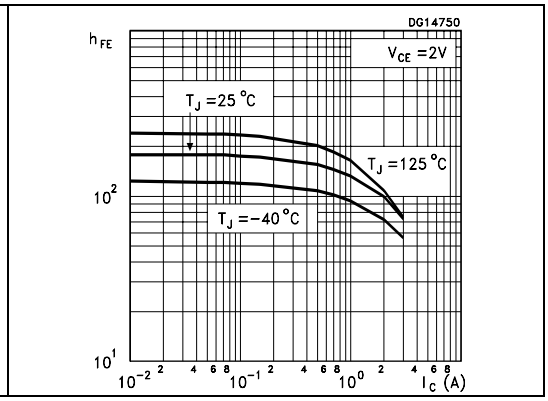


Figure 3. DC current gain Q1 NPN transistor

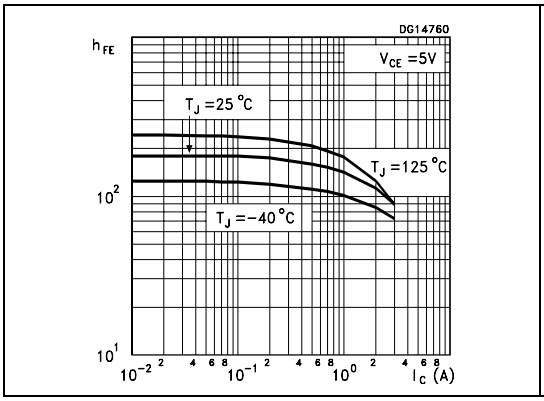


Figure 4. Collector-emitter saturation voltage Q1 NPN transistor

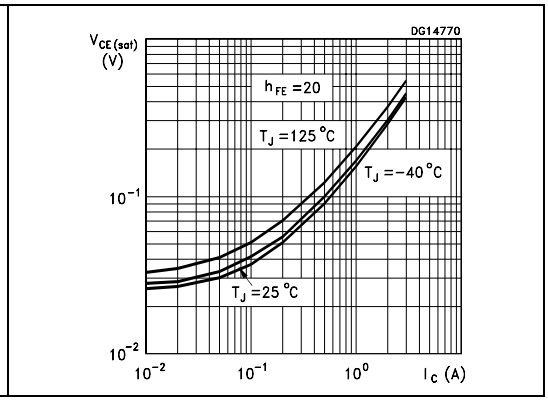


Figure 5. Base-emitter saturation voltage Q1 NPN transistor

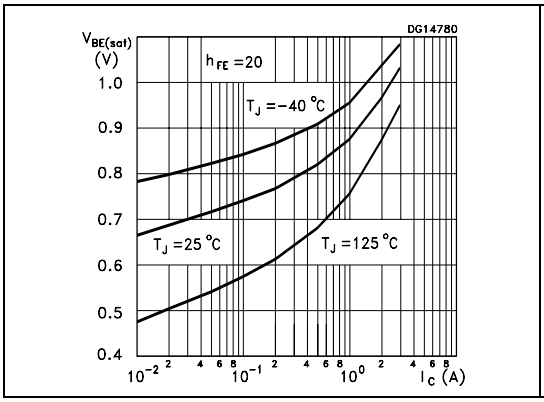


Figure 6. Reverse biased area Q2 PNP transistor

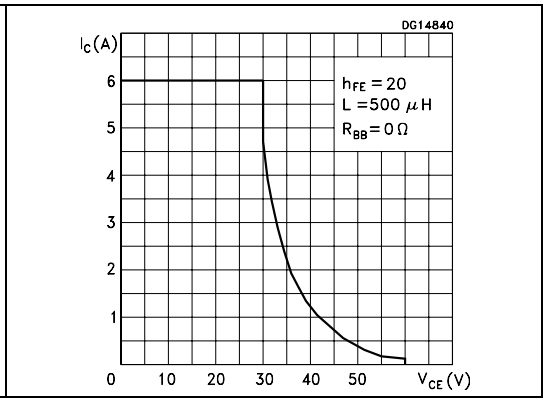


Figure 7. DC current gain Q2 PNP transistor

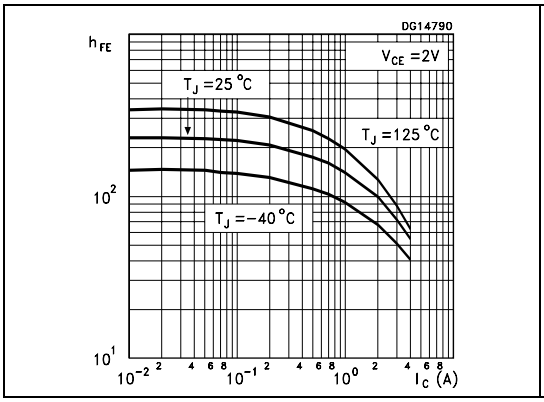


Figure 8. DC current gain Q2 PNP transistor

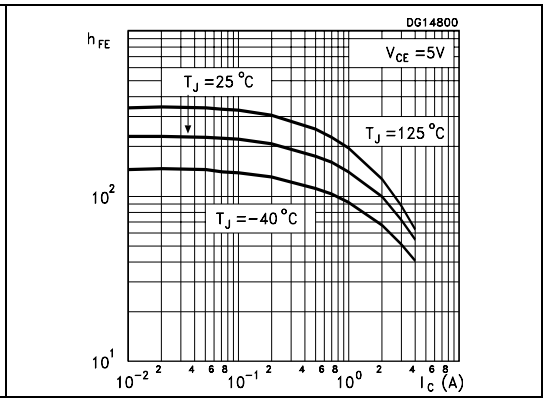


Figure 9. Collector-emitter saturation voltage Q2 PNP transistor

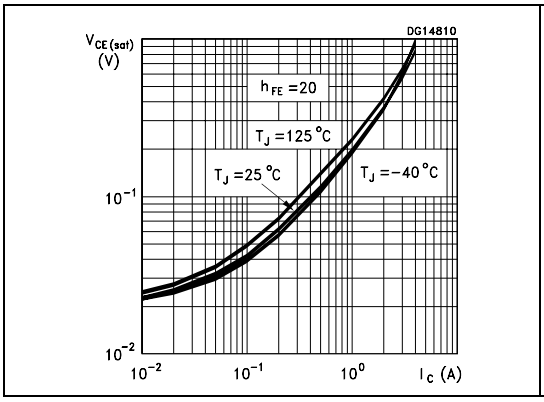
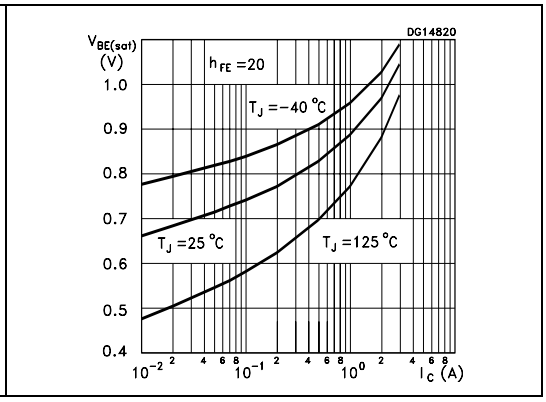
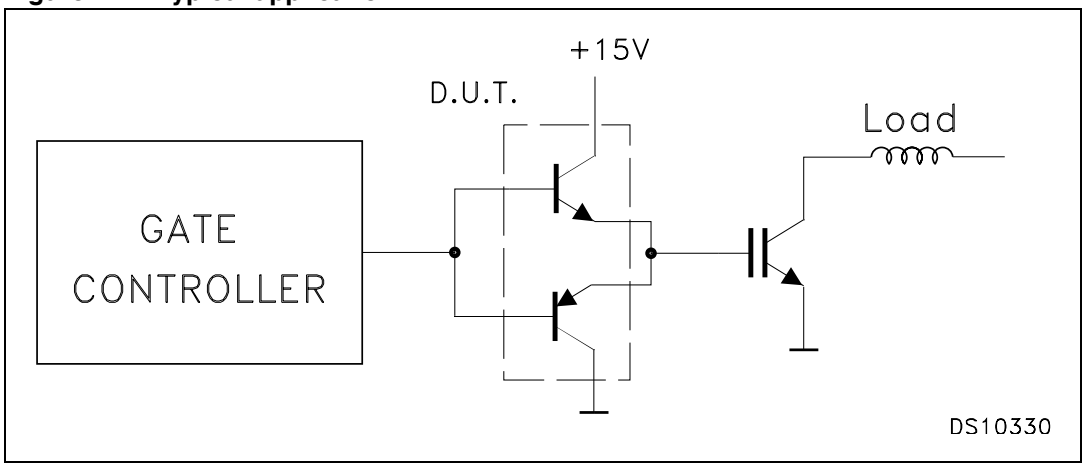


Figure 10. Base-emitter saturation voltage Q2 PNP transistor



2.2 Test circuits

Figure 11. Typical application

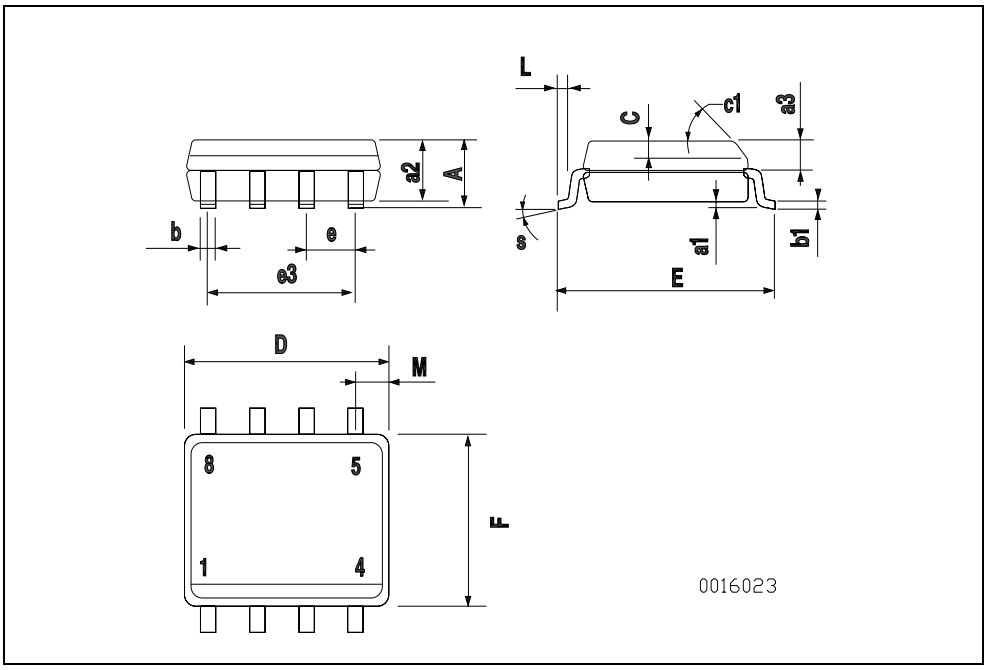


3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



4 Revision history

Table 5. Revision history

Date	Revision	Changes
22-Apr-2005	1	Initial release.
22-Mar-2006	2	New template
30-Mar-2006	3	The limit of current in figure number six has been modified from 6.5A to 6A.

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