

N- and P-Channel Quad Power MOSFET Arrays

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)} (max)$ Q1 + Q2 or Q3 + Q4	$V_{GS(th)} (max)$		Order Number / Package
		N-Channel	P-Channel	
40V	3.0Ω	2.0V	-3.0V	VQ3001N6
20V	3.0Ω	2.0V	-3.0V	VQ7254N6

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices
- ☐ Low threshold version available

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

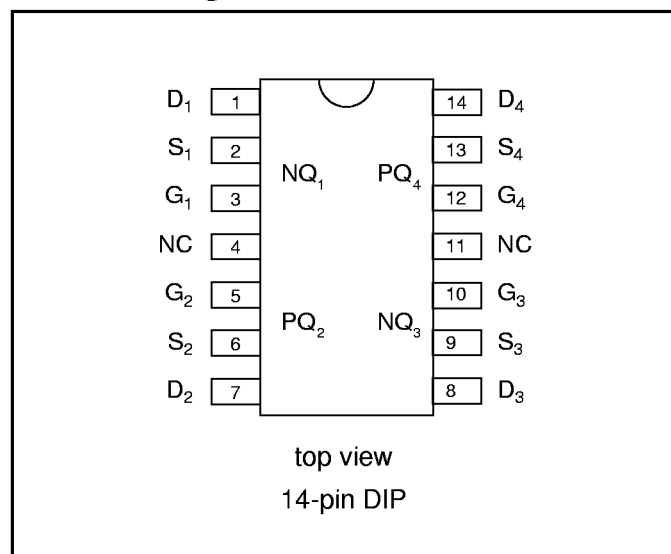
- ☐ Telecom switches
- ☐ Photo voltaic drives
- ☐ Logic level interfaces
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Motor controls

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 30V$
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Pin Configuration



Thermal Characteristics

Package	I _D (continuous) [†]		I _D (pulsed) [†]		Power Dissipation* @ T _C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I _{DR}		I _{DRM} [†]	
	N	P	N	P				N	P	N	P
Plastic Dip	1.4A	-0.65A	3.0A	-3.0A	1.5W	83.3	41.6	1.4A	-0.65A	3.0A	-3.0A

* Total for 4 die.

† Each die.

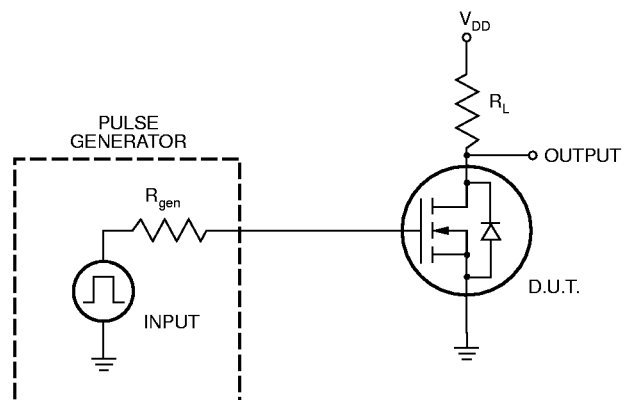
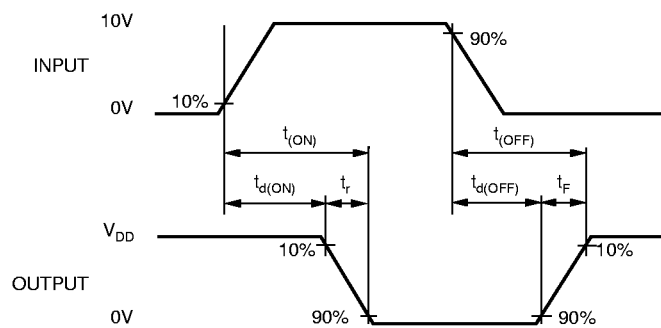
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		N-Channel		P-Channel		Unit	Test Conditions
			Min	Max	Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	VQ3001	40		-40		V	V _{GS} = 0V, I _D = 10μA
		VQ7254	20		-20			
V _{GS(th)}	Gate Threshold Voltage	VQ3001	0.8	2.5	-0.8	-4.5	V	V _{GS} = V _{DS} , I _D = 1mA T _A = 25°C
		VQ7254						
		VQ7254	0.65		-0.65		V	V _{GS} = V _{DS} , I _D = 1mA T _A = 85°C
I _{GSS}	Gate Body Leakage			100		-100	nA	V _{GS} = ±20V, V _{DS} = 0V
I _{DSS}	Zero Gate Voltage Drain Current			10		-10	μA	V _{GS} = 0V, V _{DS} = 0.8 Min. Rating
				500		-500	μA	V _{GS} = 0V, V _{DS} = 0.8 Min. Rating, T _A = 125°C
V _{DS(ON)}	Total Static Drain-to-Source ON-State Voltage	VQ3001		1.0		-2.0	V	V _{GS} = 11.4V, I _D = 1A
		TQ3001						
		VQ7254		1.0		-2.0		
R _{DS(ON)}	Total Static Drain-to-Source ON-State Resistance	VQ3001					Ω	V _{GS} = 11.4V, I _D = 1A
		TQ3001		1.0		2.0		
		VQ7254		1.0		2.0		
G _{FS}	Forward Transconductance		200		200		mS	V _{DS} = 10V, I _D = 0.5A
C _{ISS}	Input Capacitance			190		195	pF	V _{GS} = 0V, V _{DS} = 20V f = 1Mz
C _{OSS}	Output Capacitance			110		120		
C _{RSS}	Reverse Transfer Capacitance			50		60		
t _(ON)	Turn-ON Time			30		30	ns	V _{DD} = 15V, I _D = 0.65A, R _{GEN} = 25Ω
t _(OFF)	Turn-OFF Time			30		30	ns	
V _{SD}	Forward ON Voltage	VQ7254		1.8		-2.0	V	V _{GS} = 0V, I _F = 1.5A
		VQ3001		1.8		-2.0		V _{GS} = 0V, I _F = 1.5A

Notes:

1. All D.C. parameters 100% tested (pulse test: 300μs pulse, 2% duty cycle).
2. All A.C. parameters sample tested.
3. Refer to device types TN06L and TP06L for characteristic curves.

Switching Waveforms and Test Circuit



FET polarity in test circuit is N-channel only.