DATA SHEET

PHC2300
Complementary enhancement mode MOS transistors

Product specification
Supersedes data of 1997 Jun 19
File under Discrete Semiconductors, SC13b

1997 Oct 24

Philips Semiconductors

PHILIPS

Complementary enhancement mode MOS transistors

PHC2300

FEATURES

- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Universal line interface in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

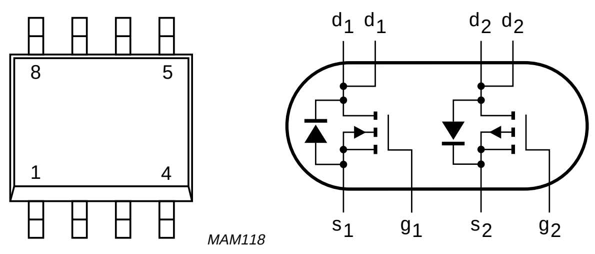


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	300	V
	P-channel		–	–300	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage				V
	N-channel	$V_{DS} = V_{GS}$; I_D = 1 mA	0.8	2	V
	P-channel	$V_{DS} = V_{GS}$; I_D = –1 mA	–0.8	–2	V
I_D	drain current (DC)	T_s = 80 °C			
	N-channel		–	340	mA
	P-channel		–	–235	mA
R_{DSon}	drain-source on-state resistance				
	N-channel	V_{GS} = 10 V; I_D = 170 mA	–	8	Ω
	P-channel	V_{GS} = –10 V; I_D = –115 mA	–	17	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	1.6	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	300	V
	P-channel		–	–300	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1			
	N-channel		–	340	mA
	P-channel		–	–235	mA
I_{DM}	peak drain current	note 2			
	N-channel		–	1.4	A
	P-channel		–	–0.9	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	1.6	W
		T_{amb} = 25 °C; note 4	–	1.8	W
		T_{amb} = 25 °C; note 5	–	0.9	W
		T_{amb} = 25 °C; note 6	–	1.2	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C

Notes

1. T_s is the temperature at the soldering point of the drain leads.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. (So both devices may be loaded up to 1.6 W at the same time).
4. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

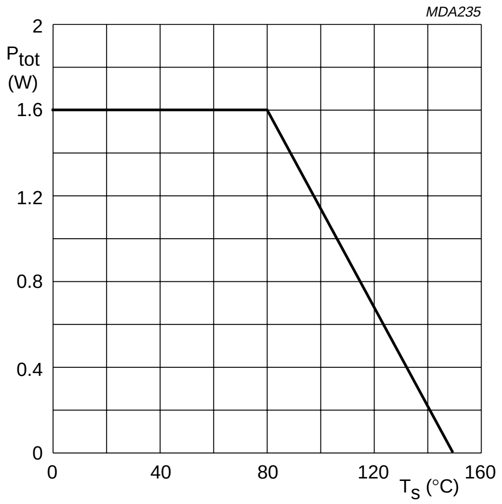
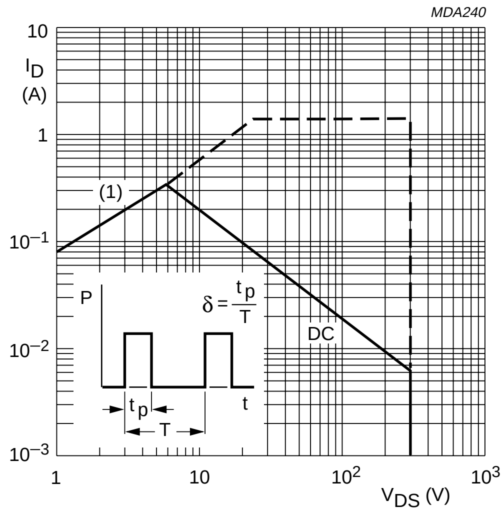


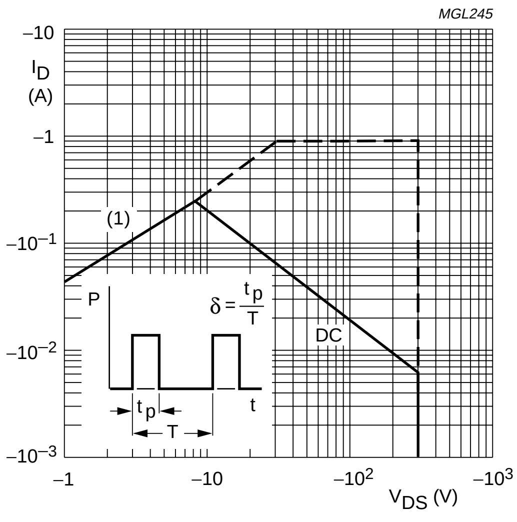
Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 80$ °C.

(1) R_{DSon} limitation.

Fig.3 SOAR; N-channel.



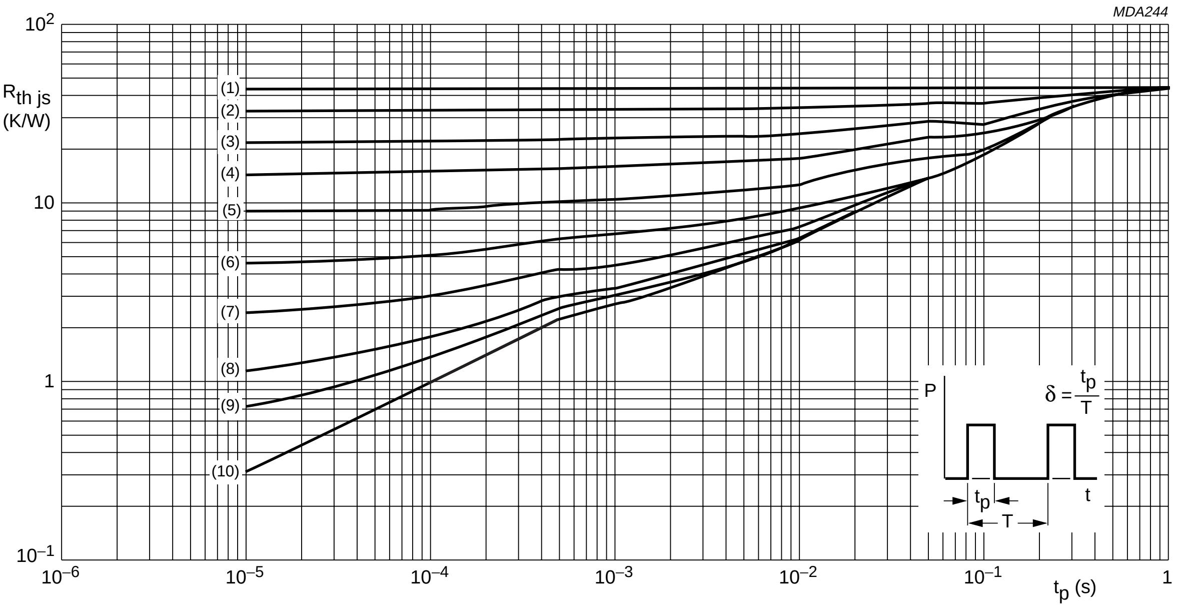
$\delta = 0.01$; $T_s = 80$ °C.

(1) R_{DSon} limitation.

Fig.4 SOAR; P-channel.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	43	K/W



(1) δ = 1.00. (2) δ = 0.75. (3) δ = 0.5. (4) δ = 0.33. (5) δ = 0.2.

(6) δ = 0.1. (7) δ = 0.05. (8) δ = 0.02. (9) δ = 0.01. (10) δ = 0.

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time for N- and P-channels; typical values.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per FET						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	V_{GS} = 0; I_D = 10 μA	300	–	–	V
	P-channel	V_{GS} = 0; I_D = –10 μA	–300	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	V_{GS} = V_{DS}; I_D = 1 mA	0.8	–	2	V
	P-channel	V_{GS} = V_{DS}; I_D = –1 mA	–0.8	–	–2	V
I_{DSS}	drain-source leakage current					
	N-channel	V_{GS} = 0; V_{DS} = 240 V	–	–	100	nA
	P-channel	V_{GS} = 0; V_{DS} = –240 V	–	–	–100	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0				
	N-channel		–	–	±100	nA
	P-channel		–	–	±100	nA
R_{DSon}	drain-source on-state resistance					
	N-channel	V_{GS} = 10 V; I_D = 170 mA	–	–	8	Ω
	P-channel	V_{GS} = –10 V; I_D = – 115 mA	–	–	17	Ω
C_{iss}	input capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	57	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –50 V; f = 1 MHz	–	45	–	pF
C_{oss}	output capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	15	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –50 V; f = 1 MHz	–	15	–	pF
C_{rss}	reverse transfer capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	2.6	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –50 V; f = 1 MHz	–	3	–	pF
Q_G	total gate charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 170 mA	–	2097	–	pC
	P-channel	V_{GS} = –10 V; V_{DS} = –50 V; I_D = –115 mA	–	2137	–	pC
Q_{GS}	gate-source charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 170 mA	–	75	–	pC
	P-channel	V_{GS} = –10 V; V_{DS} = –50 V; I_D = –115 mA	–	68	–	pC
Q_{GD}	gate-drain charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 170 mA	–	527	–	pC
	P-channel	V_{GS} = –10 V; V_{DS} = –50 V; I_D = –115 mA	–	674	–	pC
Switching times						
t_{on}	turn-on time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 170 mA	–	2.5	10	ns
	P-channel	V_{GS} = 0 to –10 V; V_{DD} = –50 V; I_D = –115 mA	–	4	10	ns
t_{off}	turn-off time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 50 V; I_D = 170 mA	–	17	30	ns
	P-channel	V_{GS} = –10 to 0 V; V_{DD} = –50 V; I_D = –115 mA	–	25	35	ns

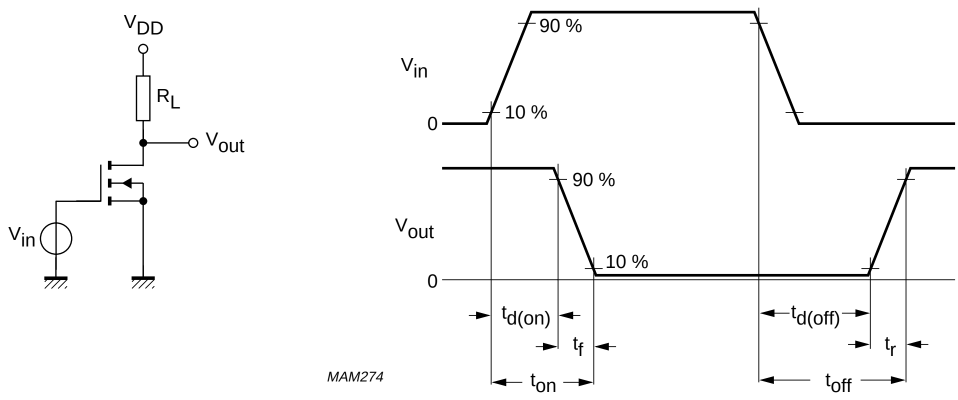


Fig.6 Switching times test circuit with input and output waveforms; N-channel.

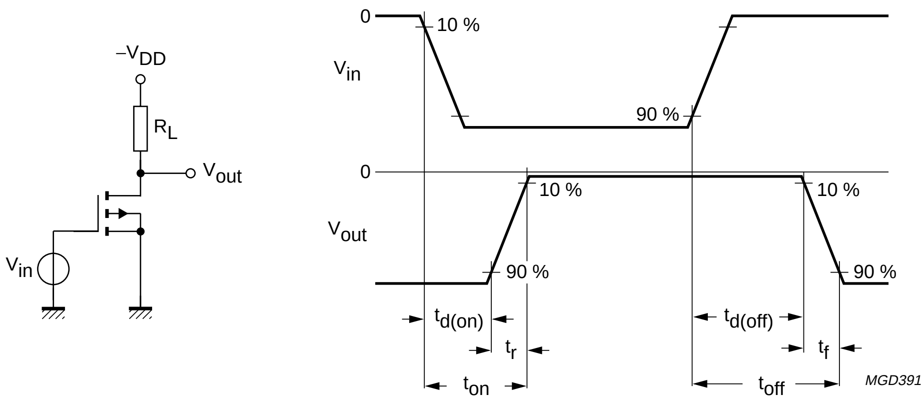
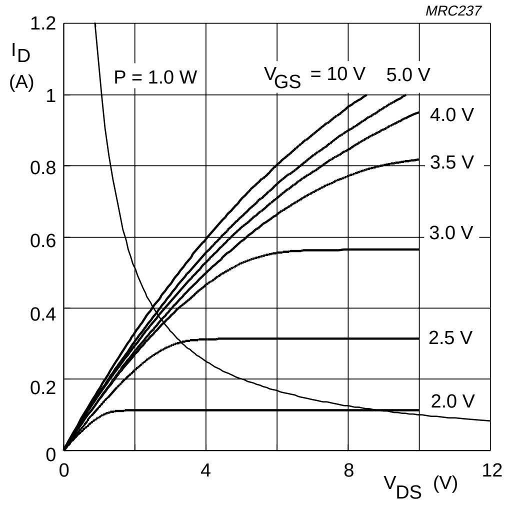
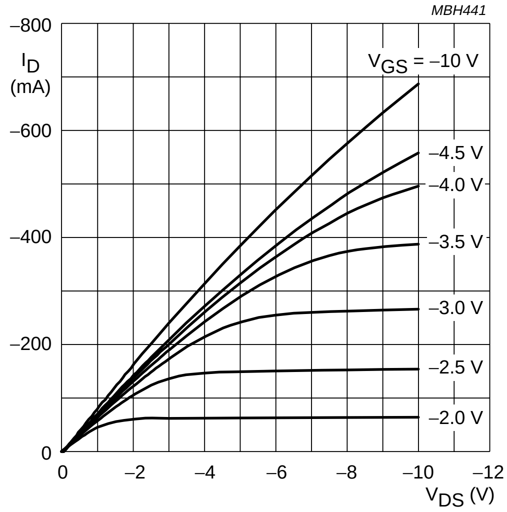


Fig.7 Switching times test circuit with input and output waveforms; P-channel.



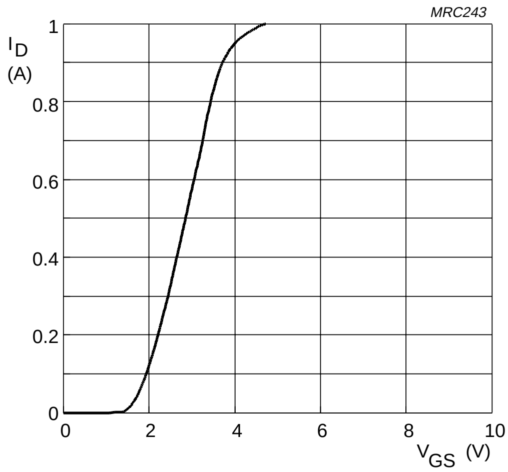
T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Output characteristics; N-channel typical values.



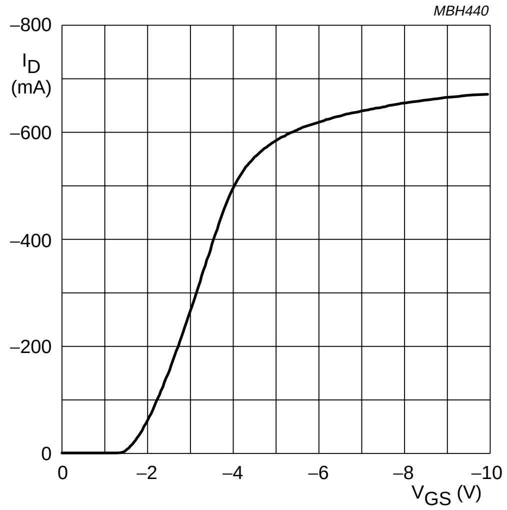
T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.9 Output characteristics; P-channel typical values.



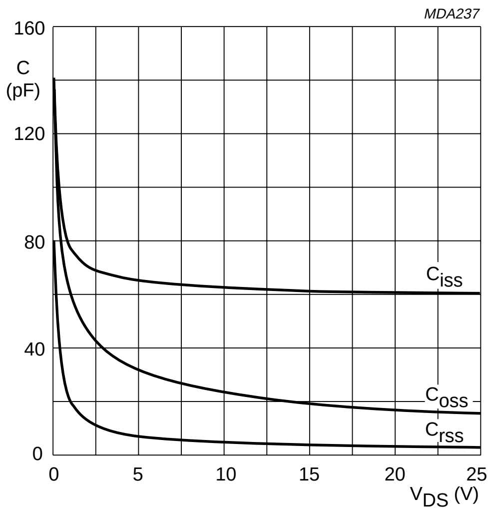
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.10 Transfer characteristic; N-channel typical values.



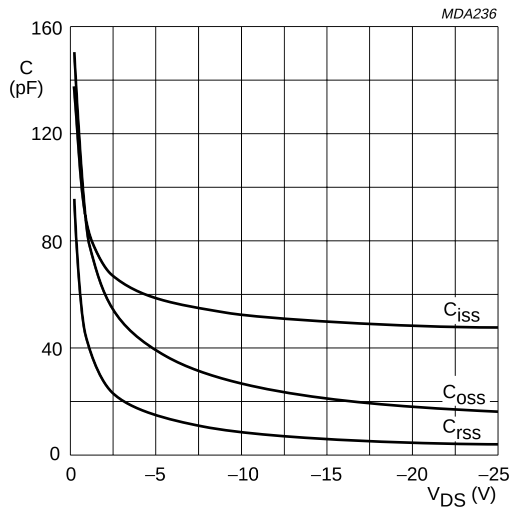
V_{DS} = −10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.11 Transfer characteristic; P-channel typical values.



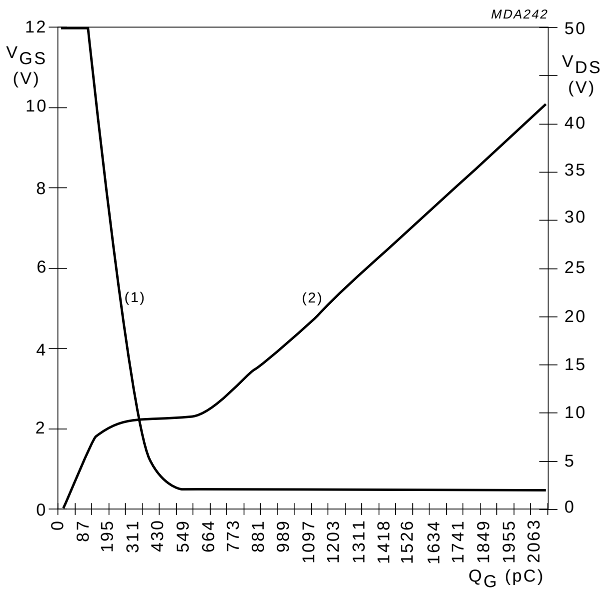
f = 1 MHz; T_{amb} = 25 °C.

Fig.12 Capacitance as a function of drain-source voltage; N-channel typical values.



f = 1 MHz; T_{amb} = 25 °C.

Fig.13 Capacitance as a function of drain-source voltage; P-channel typical values.

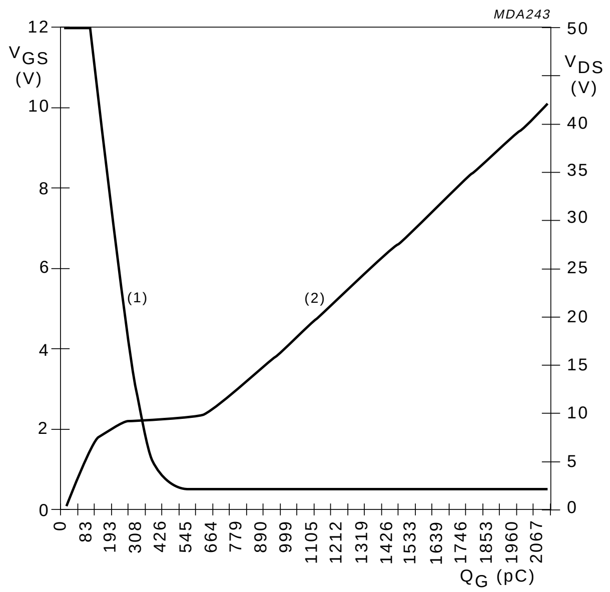


V_{DD} = 50 V; I_D = 170 mA; T_{amb} = 25 °C.

(1) V_{DS}.

(2) V_{GS}.

Fig.14 Gate-source voltage and drain-source voltage as a function of total gate charge; N-channel typical values.

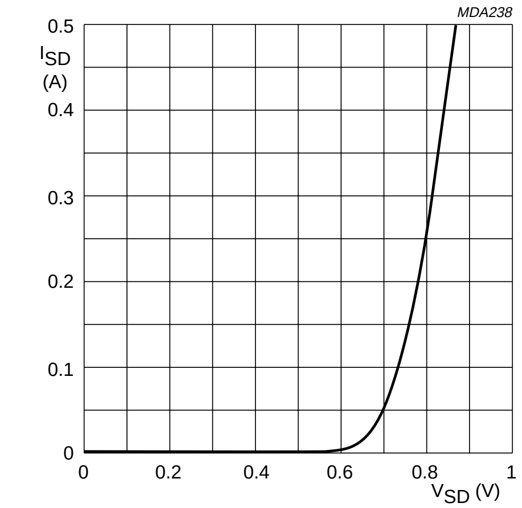


V_{DD} = –50 V; I_D = –115 mA; T_{amb} = 25 °C.

(1) V_{DS}.

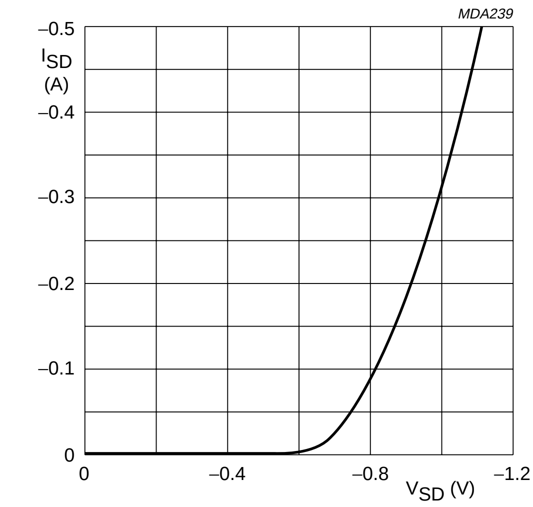
(2) V_{GS}.

Fig.15 Gate-source voltage and drain-source voltage as a function of total gate charge; P-channel typical values.



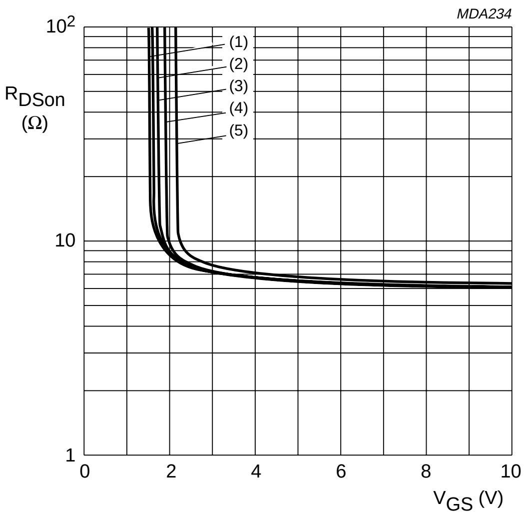
$V_{GD} = 0$.

Fig.16 Source-drain current as a function of source-drain diode forward voltage; N-channel typical values.



$V_{GD} = 0$.

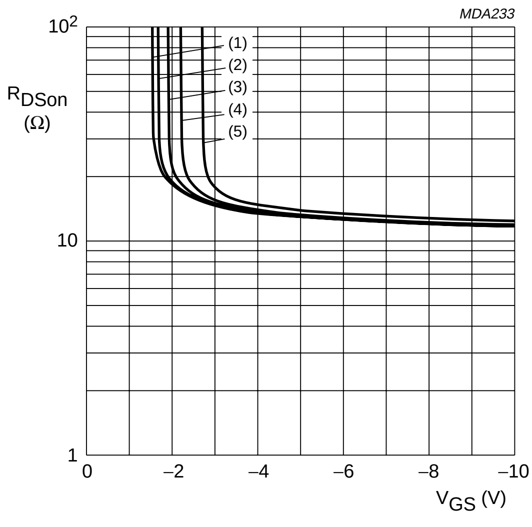
Fig.17 Source-drain current as a function of source-drain diode forward voltage; P-channel typical values.



$V_{DS} \geq I_D \times R_{DSon}$; $T_{amb} = 25$ °C;
$t_p = 300$ µs; $\delta = 0$.

(1) $I_D = 10$ mA.
(2) $I_D = 20$ mA.
(3) $I_D = 50$ mA.
(4) $I_D = 100$ mA.
(5) $I_D = 200$ mA.

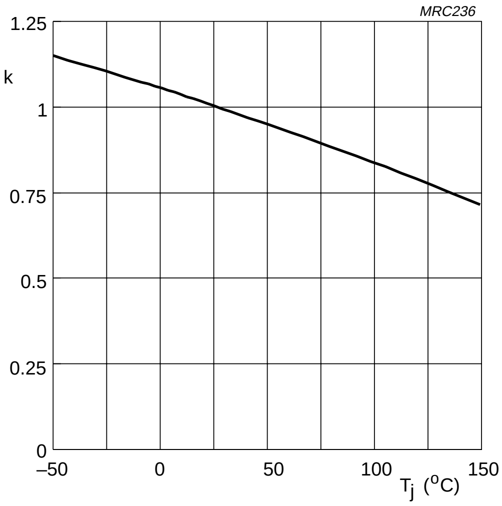
Fig.18 Drain-source on-state resistance as a function of gate-source voltage; N-channel typical values.



$V_{DS} \geq I_D \times R_{DSon}$; $T_{amb} = 25$ °C;
$t_p = 300$ µs; $\delta = 0$.

(1) $I_D = -10$ mA.
(2) $I_D = -20$ mA.
(3) $I_D = -50$ mA.
(4) $I_D = -100$ mA.
(5) $I_D = -200$ mA.

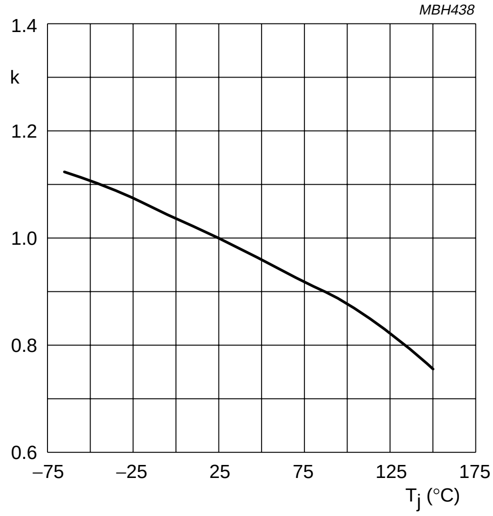
Fig.19 Drain-source on-state resistance as a function of gate-source voltage; P-channel typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

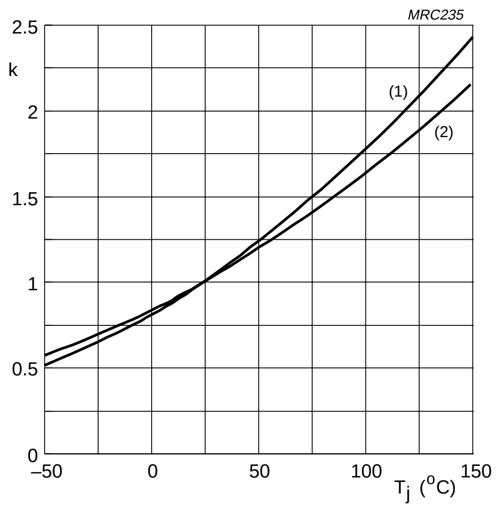
Fig.20 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; N-channel, typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = –1 mA.

Fig.21 Temperature coefficient of gate-source threshold voltage as function of junction temperature; P-channel typical values.

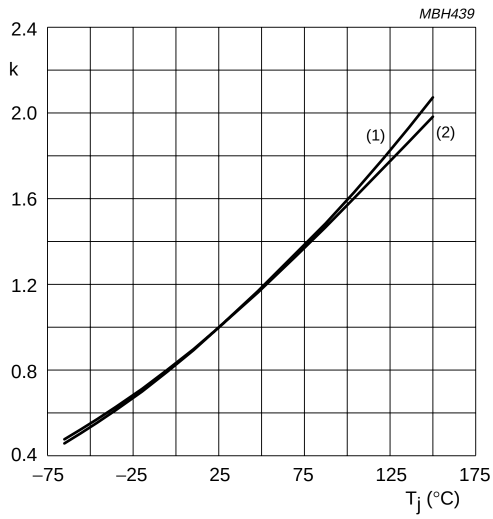


$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at V_{GS} = 10 V; I_D = 250 mA.

(2) R_{DSon} at V_{GS} = 2.4 V; I_D = 20 mA.

Fig.22 Temperature coefficient of drain-source on-resistance as a function of junction temperature; N-channel typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

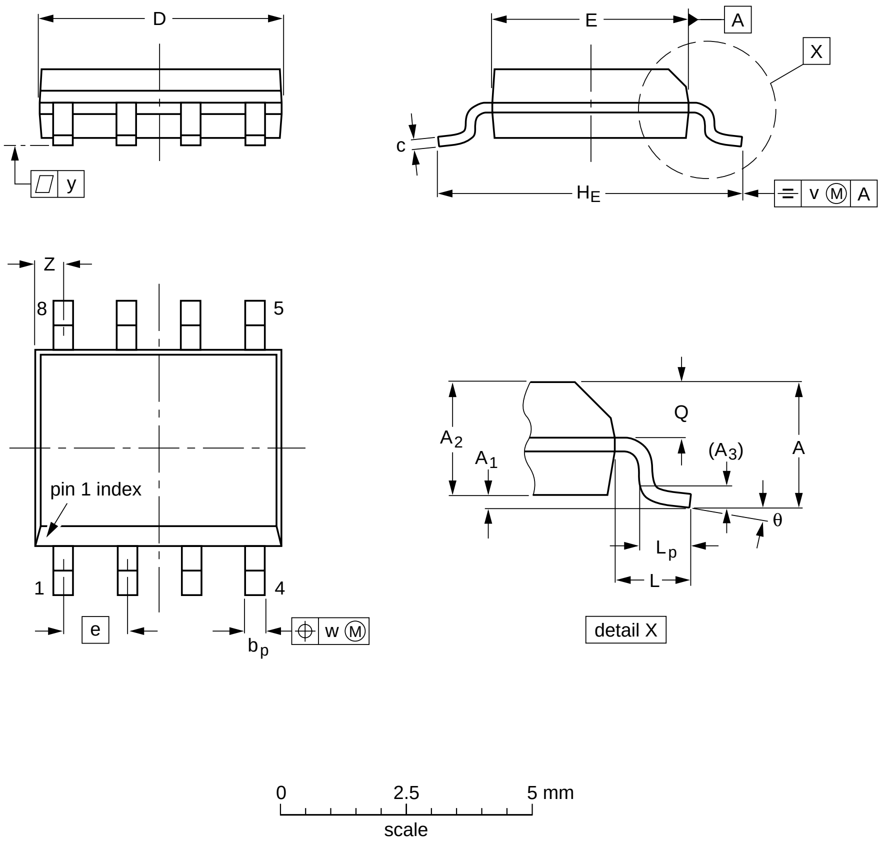
(1) R_{DSon} at V_{GS} = -4.5 V; I_D = –80 mA.

(2) R_{DSon} at V_{GS} = -2.8 V; I_D = –50 mA.

Fig.23 Temperature coefficient of drain-source on-resistance as a function of junction temperature; P-channel typical values.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Printed in The Netherlands 137107/1200/02/pp16 Date of release: 1997 Oct 24 Document order number: 9397 750 02783

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