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NEC Electronics Inc.

μPD3570
2560-BIT CCD
LINEAR IMAGE SENSOR

PRELIMINARY

Description

The μPD3570 is a CCD (charge-coupled device) linear image sensor that changes optical images to electrical signals. It has 2560 photo-elements, 64 optical-black elements, two lines of CCD charge transfer registers, a drive unit, a sample-and-hold circuit, and an output amplifier. The drive unit simplifies the external circuit and reduces total drive power, and the sample-and-hold circuit substantially reduces output signal noise.

The photo-elements have excellent response characteristics because of their PN junction construction. They are 7 x 5 μm, separated by 2 μm channel stoppers.

The charge transfer registers feature extremely high transfer efficiencies, above 99.996%.

Features

☐ Clock generator and drive unit on-chip allows direct drive by +5 V logic system
☐ Excellent photo-electrical characteristics
☐ Optical-black clamp circuit controls dark-level DC voltage
☐ Sensor reset function controls storage charges
☐ High resolution
☐ Similar response characteristics to those of the human eye

Ordering Information

Part No.	Package
μPD3570D	20-pin ceramic shrink-DIP

Pin Configuration

20-Pin Ceramic Shrink DIP (300 mil)


```
AGND  □ 1       20 □ AGND
 OUT  □ 2       19 □ V+
 AV+  □ 3       18 □ CH
  V+  □ 4       17 □ VCL
 SUB  □ 5       16 □ tREF
  T1  □ 6       15 □ T2
  T3  □ 7       14 □ T4
  SR  □ 8       13 □ TG
DGND  □ 9       12 □ CLK
  VL  □ 10      11 □ DGND
```

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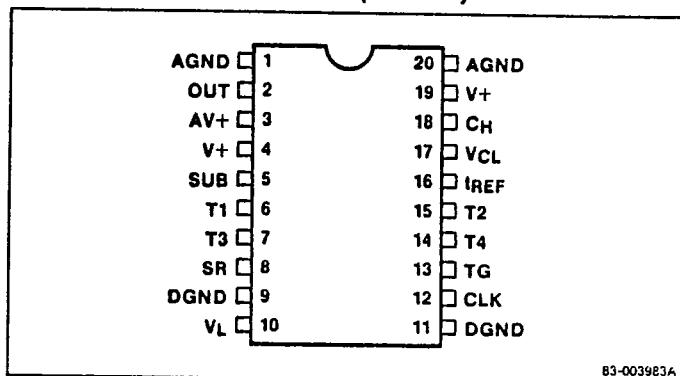
Pin Identification

Symbol	Function
AGND	Analog ground
OUT	Output
AV+	+12 V analog supply voltage
V+	+12 V driver supply voltage
SUB	Substrate
T1-T4 (Note 1)	Test 1 through 4
SR	Sensor reset
DGND	Digital ground
V_L	+5 V logic supply voltage
CLK	Master clock
TG	Transfer gate clock
t_{REF}	Reference timing output
V_{CL}	Clamp voltage
C_H	Hold capacitance

Note:

During normal operation, T1 and T2 should be tied to DGND, and T3 and T4 to +12 V.

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Block Diagram
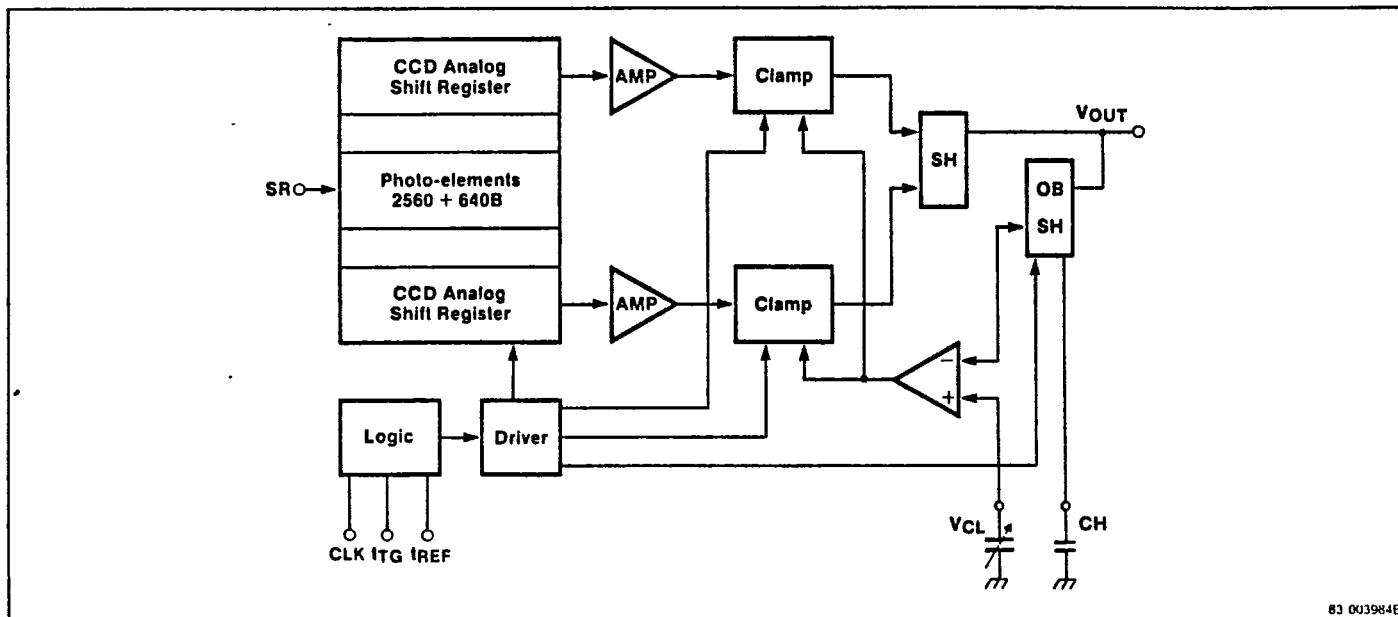
Absolute Maximum Ratings

$T_A = 25°C$

Driver supply voltage, AV+ or V+	−0.3 to +15 V
Logic supply voltage, V_L	−0.3 to +7 V
Input voltage, pins 6, 7, 8, 14, 15, 17	−0.3 to +15 V
Input voltage, pins 5, 12, 13	−0.3 to +7 V
Operating temperature range	−25 to +55°C
Storage temperature range	−40 to +100°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Photo-Element Construction
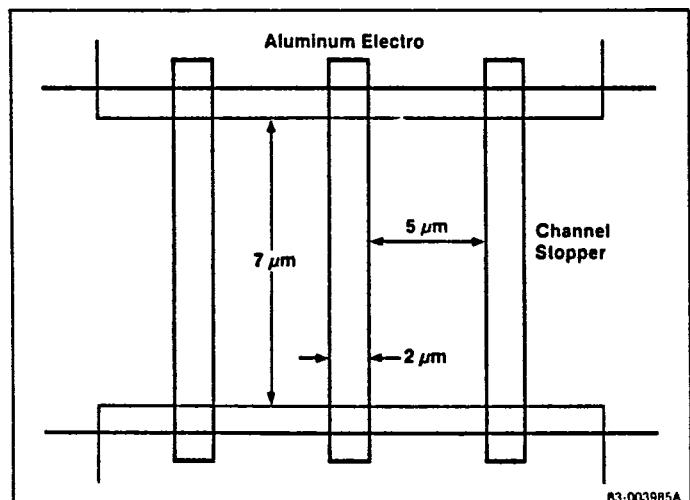
Recommended Operating Conditions

$T_A = −25$ to $+55°C$

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Driver supply voltage	V+, AV+	11.4	12.0	12.6	V
Logic supply voltage	V_L	4.75	5.0	5.25	V
Substrate voltage	V_{SUB}	4.75	5.0	5.25	V
Sensor reset ON voltage	V_{SR} (on)	11	12		V
Sensor reset OFF voltage	V_{SR} (off)	1.5	2.5	3.5	V
Input voltage, high	V_{INH}	2.4			V
Input voltage, low	V_{INL}			0.5	V
Master clock frequency	CLK	0.2	1.0	3.0	MHz
TG clock	t_{TG}	2t (Note 1)		10	μs
Clamp voltage	V_{CL}	3.0	3.5	4.0	V
Hold capacitance	C_H	2.2	4.7	10	μF

Note:

(1) t = 1/CLK
Test pin voltage T1 = T2 = 0 V
Test pin voltage T3 = T4 = +12 V

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DC Characteristics

$T_A = 25°C$; $V+ = AV+ = 12 V$; $V_L = +5 V$; $V_{SR} = 1 V$; $V_{CL} = 3 V$; $C_H = 4.7 μF$; $f_{CLK} = 1 MHz$; $t_{TG} = 4 μs$; $t_{STO} = 5 ms$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Clock input capacitance	C_{CLK}		10		pF	
Clock input leakage current	I_{LCLK}		1	10	μA	$V_{IN} = 5 V$
Output voltage, high	V_{OH}	3.5	4.5	5.0	V	$R_L = 5 k$; OUT—GND
Output voltage, low	V_{OL}		0.2	0.8	V	$R_L = 5 k$; OUT—VDG
Sensor reset capacitance	C_{SR}		100		pF	
Sensor reset current	I_{SR}			100	μA	No transients
Test leakage current	I_{LTEST}		1	10	μA	Pins 7, 14
Clamp leakage current	I_{LCLAMP}		1	10	μA	
Substrate current	I_{SUB}		10	100	μA	$V_{SUB} = 5 V$
Analog supply current	$AI+$	5	8	12	mA	Pin 3
Driver supply current	$I+$	5	8	12	mA	Pins 4, 19 total
Logic supply current	I_L	20	35	60	mA	
Output signal impedance	Z_O		0.5	1.5	kΩ	
Clamp offset voltage	$V_{CL(os)}$	−70	0	+80	mV	$V_{OB} — V_{CL}$ at $V_{CL} = 3 V$
Output saturation voltage	$V_{O(sat)}$	2.5	3.5	4.5	V	
Saturation exposure SE			0.83		lx.s	2856 K tungsten lamp
			2.50		lx.s	White fluorescent
Photo-response non-uniformity			±5	±10	%	$V_{OUT} = 2 V$, 3200 K
Average dark signal			2	10	mV	See timing chart
Dark signal non-uniformity			2	15	mV	
Sensitivity		3.0	4.2	5.4	V/lx.s	2856 K tungsten lamp
		0.98	1.4	1.82	V/lx.s	White fluorescent

Sensor Reset

Sensor reset is a function that controls the signal charge generated by the photo-electric conversion of the photo-transistors. The following timing diagram shows the relationship between SR and the transfer gate timing signal (t_{TG}).

Note that when SR is held low, the storage time is determined strictly by t_{TG}, and is defined to be the time between falling edges of successive t_{TG} pulses (shown in the drawing as t_{STO1}).

With SR high, the storage time is defined as the time between the falling edge of the SR pulse and the falling edge of the t_{TG} pulse. Thus, storage time is controlled by the width of the SR pulse.

Using the SR function, the output signal can be held at a fixed level, even if the input varies.
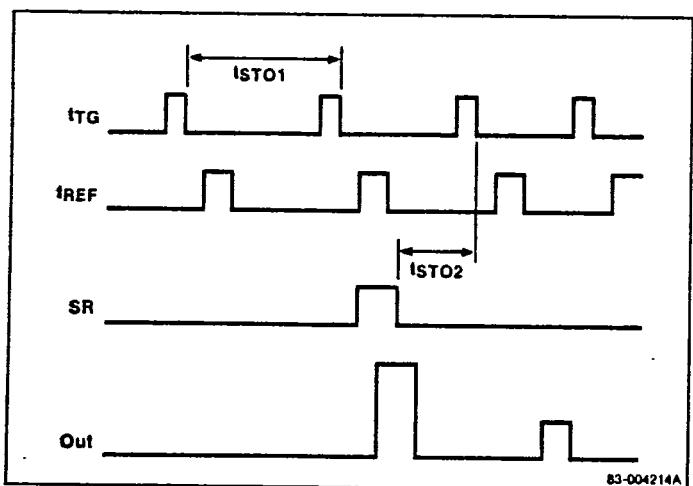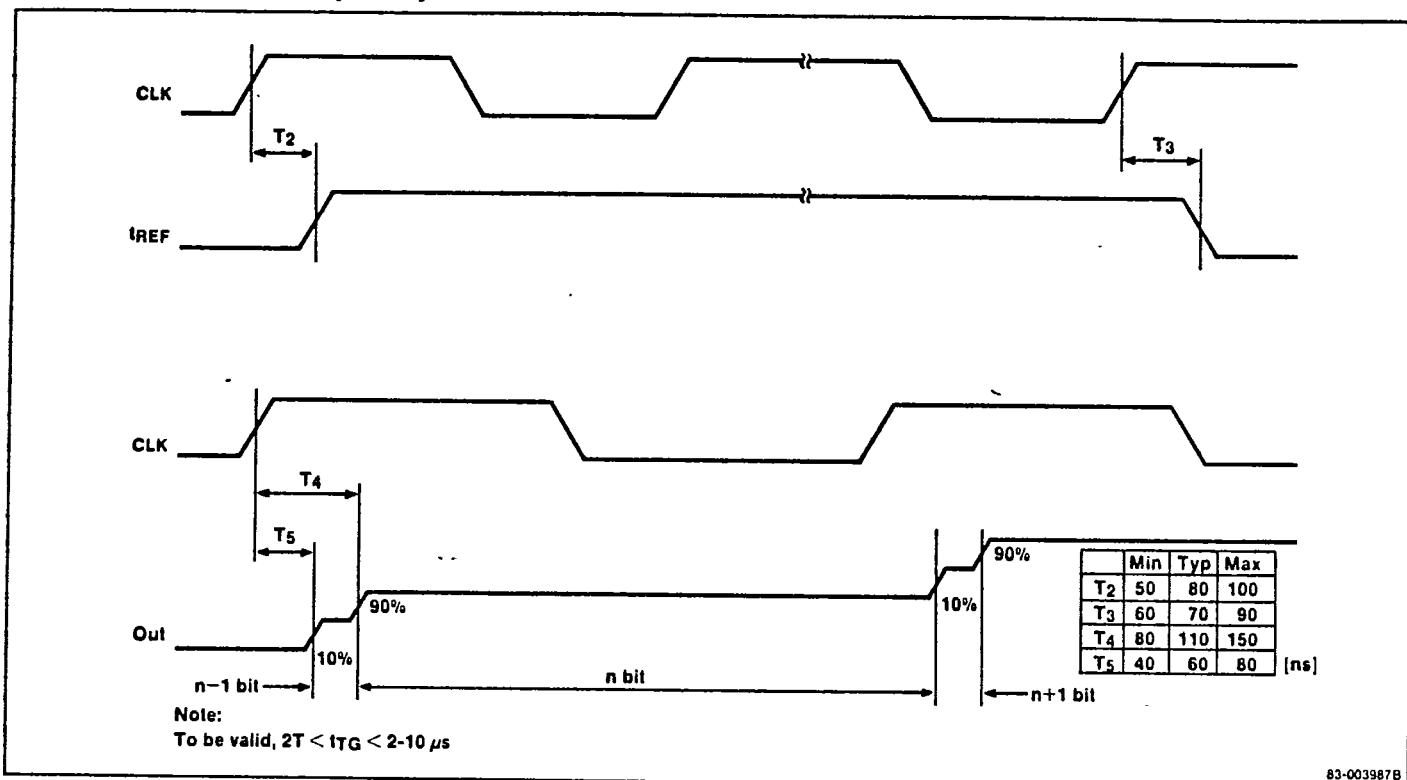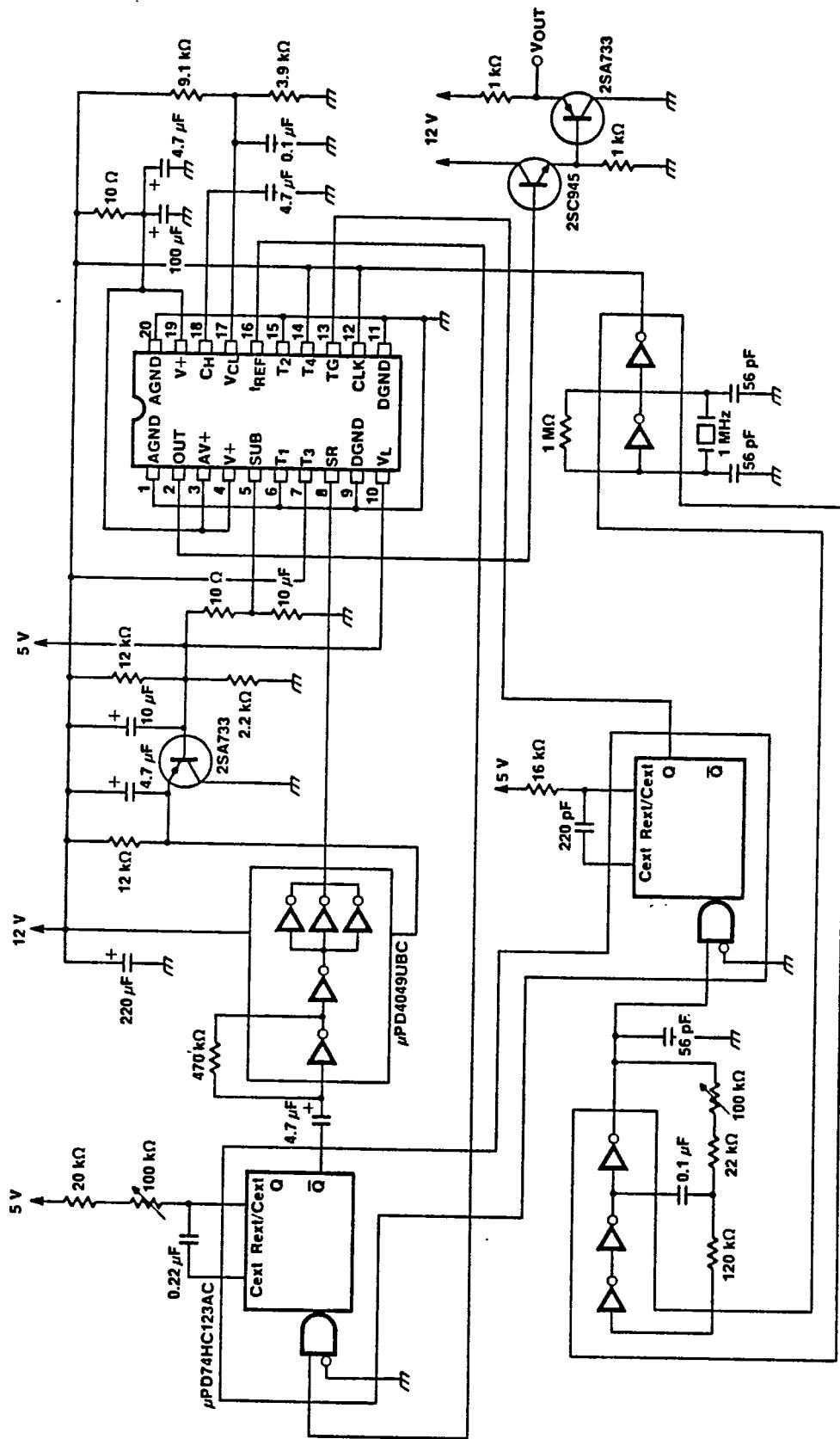
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Timing Waveform

[N-1]N
0 1 2
CLK
5
10
20
65
70
75
80
85
90
2640
2645
2650
2655

tTG

4T Note 1
12T

tREF

2T
50T
16T

64T
12T
4T

Optical Black 64-bit

4-bit

Valid Photo
2 560-bit

2 560T

Invalid Dummy
Photo cell   4-bit
4-bit
4T
4T

DSNU

Out
T₁

Out

Out
Note:
T₁ = tTG + 2T

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Timing Waveforms (cont)

	Min	Typ	Max	
T_2	50	80	100	
T_3	60	70	90	
T_4	80	110	150	
T_5	40	60	80	[ns]

Note:
To be valid, $2T < t_{TG} < 2 \text{-} 10 \ \mu s$

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Typical Applications

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Operating Characteristics

$T_A = 25°C$

Dark Signal
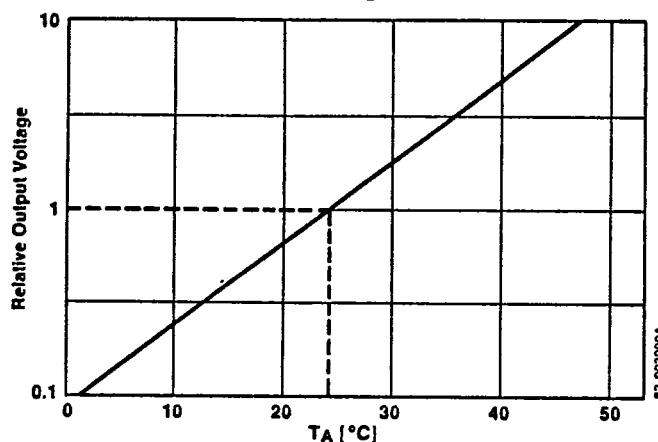
Signal Output
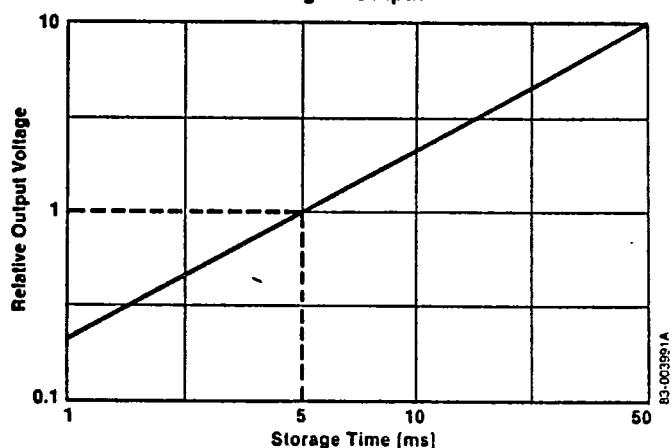
Ambient Temperature [°C]
Relative Spectrum Response $T_A = 25°C$

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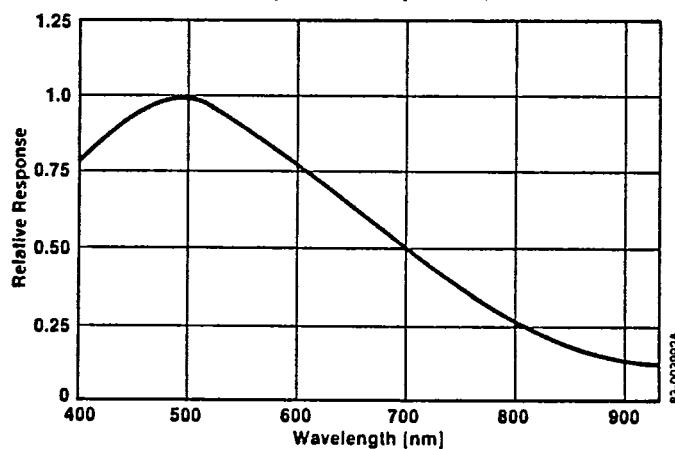
Application Notes

Electrostatic Damage

Normal precautions for MOS devices should be taken.

Surge Voltages

The power supply pins (pins 3, 4, 14) can be easily damaged by surge voltages. Use normal current limiting and bypass techniques.

Sensor Reset

Voltage applied to this pin must not be allowed to fall below 1.5 V. Serious damage to the device could result. Drive signal must be pulsed. Driving the SR pin by anything other than a pulse will change the characteristics of the device. Drive pulse to the SR pin should be applied after the leading edge of the t_{TG} pulse.

Window Glass

If some dust gets on the glass it is possible that the resultant output signal may be misinterpreted as a black level signal. So the surface of the glass must always be kept clean. Avoid abrasives and strong chemicals; if glass needs to be cleaned, use soap and water and wipe with a soft cloth.

Ambient Temperature

The dark current of the device is very temperature sensitive, so care must be taken to ensure a constant ambient temperature.

Substrate Pin

+5 power should be applied prior to the application of +12 V.