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**REVISION HISTORY**

07/04—Revision PrB July 27 2004

09/04 - Revision PrC Sept 30 2004: spec changes

11/04 – Revision PrD: RSSI added in

## ELECTRICAL SPECIFICATIONS

Table 1.

Parameter	Conditions <sup>1</sup>	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
Bandwidth (BW) <sup>2</sup>	-3 dB	3.3	3.8		GHz
Total Input RMS Noise ( $I_{RMS}$ ) <sup>2</sup>	DC to 4.0 GHz		520	TBD	nA
Small Signal Transimpedance ( $Z_T$ )	100MHz	2800	3800	4800	V/A
Low Frequency Cutoff	$I_{IN} = 10\mu A$		15		kHz
	$I_{IN} = 500\mu A$		TBD		kHz
Output Return Loss	DC to 4.25GHz, differential		-20	-12	dB
Input Overload Current <sup>3</sup>	Pavg	TBD	3.25		dBm
Maximum Output Swing	pk-pk diff, $I_{IN,PK-PK} = 2.0$ mA	180	250	350	mV
Output Data Transition Time	20% to 80% rise/fall time $I_{IN,PK-PK} = 2.5$ mA		40		ps
PSRR	<10 MHz		-40		dB
Group Delay Variation	50 MHz to 1.0 GHz		TBD		ps
Transimpedance Ripple	50 MHz to 1.0 GHz		TBD		dB
Total Jitter	$10\mu A < I_{IN,PK-PK} \leq 100\mu A$		TBD	TBD	ps
	$100\mu A < I_{IN,PK-PK} \leq 2.0\mu A$		TBD	TBD	ps
Deterministic Jitter	$10\mu A < I_{IN,PK-PK} \leq 100\mu A$		2		ps
	$100\mu A < I_{IN,PK-PK} \leq 2.0\mu A$		4		Ps
Linear Output Range	Pk-pk, < 1dB compression		TBD		mV
<b>DC PERFORMANCE</b>					
Power Dissipation	$I_{IN,AVE} = 0$	50	75	120	mW
Input Voltage			0.85		V
Output Common Mode Voltage	DC terminated to VCC		$V_{CC} - 0.12$		V
Output Impedance	Single-ended		50		$\Omega$
PD FILTER Resistance	$R_F$		200		$\Omega$
PD FILTER Capacitance	$C_F$		20		pF
RSSI Sensitivity	$I_{IN,AVE} = 0$ uA to 1 mA		0.8		V/mA
RSSI Offset	$I_{IN,AVE} = 0$ uA		TBD		mV

<sup>1</sup> Min/Max VCC = +3.3 V  $\pm$  0.3 V, T<sub>a</sub> = -40°C to +95°C; Typ VCC = 3.3 V, T<sub>a</sub> = +25°C.<sup>2</sup> Photodiode capacitance C<sub>D</sub> = 0.5pF  $\pm$  0.15pF, photodiode resistance = 5  $\Omega$ . Load impedance = 50 $\Omega$  (each output, ac-coupled).<sup>3</sup> 10<sup>-10</sup> BER, 10 dB ER,

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage ( $V_{CC}$ to GND)	5 V
Maximum Input Current	10 mA
Storage Temperature Range	-65°C to +125°C
Operating Ambient Temperature Range	-40°C to +95°C
Maximum Junction Temperature	165°C
Die Attach Temperature (<60 seconds)	450°C

Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PAD DESCRIPTION

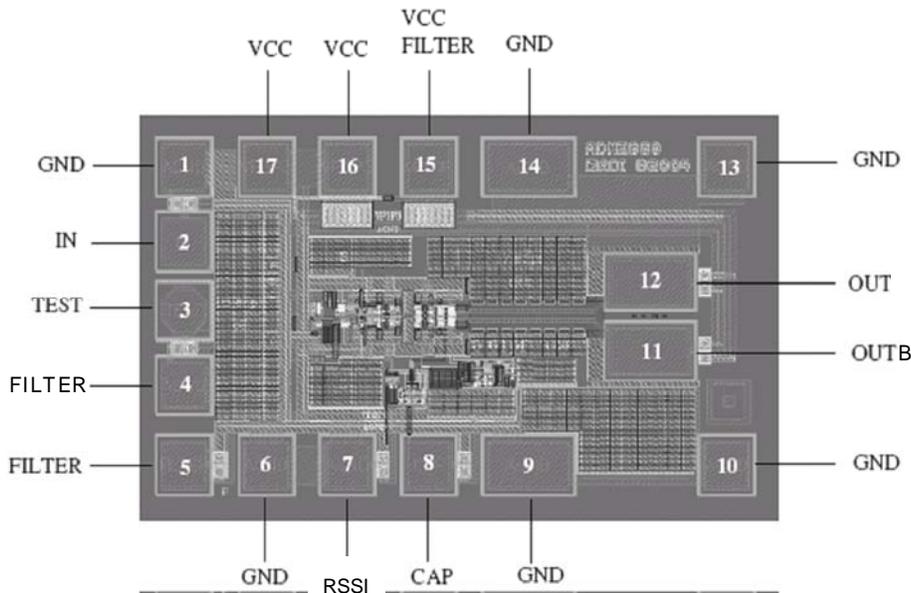


Table 3.

Pad No.	Pad Name	Function
1	GND	Ground (input return).
2	IN	Current input. Bond directly to PD anode.
3	TEST	Test probe Pad. Leave floating.
4	FILTER	Filter Output
5	FILTER	Filter Output
6	GND	Ground.
7	RSSI	Voltage Output (provides average input current reading)
8	CAP	Low Frequency setpoint. Connect with 1 nF capacitance to GND for < 15 kHz.
9	GND	Ground.
10	GND	Ground (output return).
11	OUTB	Negative Output. Drives 50 $\Omega$ termination (ac or dc termination).
12	OUT	Positive Output. Drives 50 $\Omega$ termination (ac or dc termination).
13	GND	Ground (output return).
14	GND	Ground.
15	VCCFILTER	Filter Supply. Connect to V <sub>CC</sub> to enable on-chip 200 $\Omega$ , 20 pF Filter.
16	VCC	3.3 V positive Supply. Recommended bypass to GND is 200 pF RF capacitor.
17	VCC	3.3 V positive Supply. Recommended bypass to GND is 200 pF RF capacitor.

## PAD LAYOUT

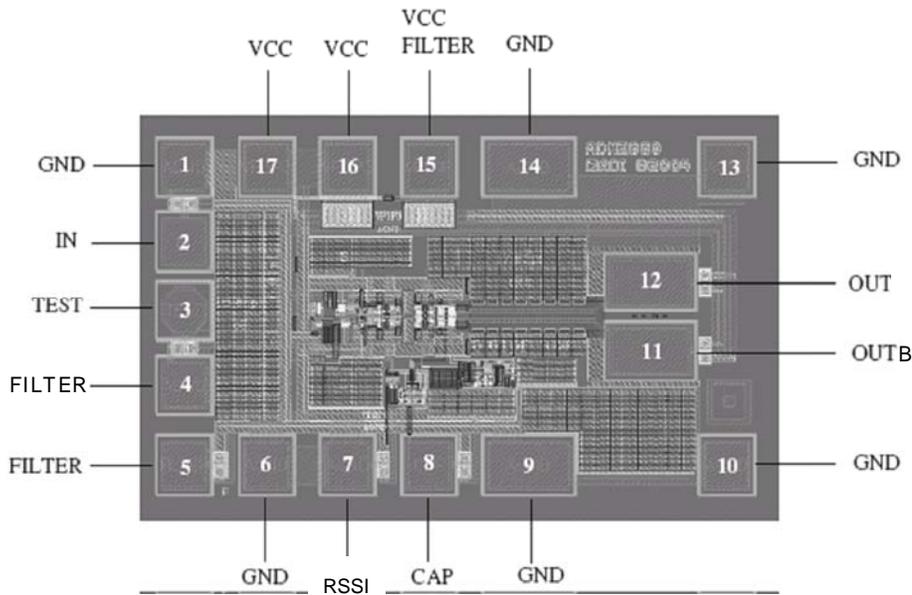


Figure 2.. Pad Layout

## PAD COORDINATES

Table 4.

PAD #	PAD	X (um)	Y (um)
1	GND	-500	260
2	IN	-500	130
3	TEST	-500	10
4	FILTER	-500	-120
5	FILTER	-500	-260
6	GND	-350	-260
7	RSSI	-200	-260
8	CAP	-50	-260
9	GND	130	-260
10	GND	500	-260
11	OUTB	350	-60
12	OUT	350	60
13	GND	500	260
14	GND	130	260
15	VCCFILTER	-50	260
16	VCC	-200	260
17	VCC	-350	260

## DIE INFORMATION

**Die Size**

0.7mm × 1.2mm

(edge-edge including 1mil scribe)

**Die Thickness**

10mils = 0.25mm

**Passivation Openings**

0.075 mm × 0.075 mm

(pads 1-8, 9, 10, 13, 15, 16, 17)

0.144mm × 0.075mm

(pads 9, 11, 12, 14)

**Passivation Composition**5000Å Si<sub>3</sub>N<sub>4</sub> (top)+5000 Å SiO<sub>2</sub> (bot)**Pad Composition**

Al/1%Cu

**Backside Contact**

## ASSEMBLY RECOMMENDATIONS

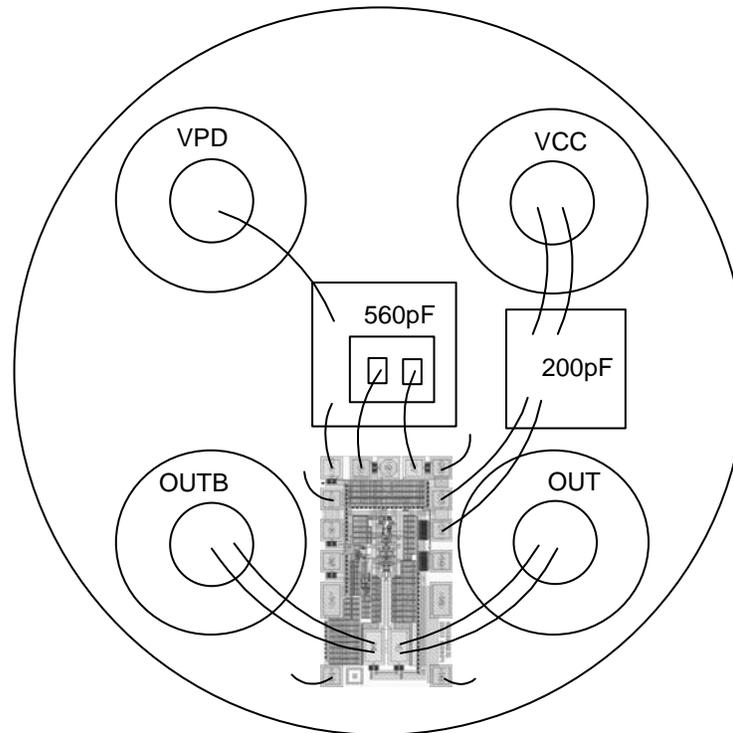


Figure 3. 5-Pin TO-46 with External Photodiode Supply  $V_{PD}$

1× Vendor-Specific (0.3 mm × 0.3 mm) 4.25 Gbps Photo Diode

1× ADN2882 (0.7 mm × 1.2 mm) Analog Devices SiGe 4.25 Gbps Transimpedance Amplifier

1× 200 pF RF single-layer capacitor

1× 560pF RF Single-layer capacitor

### Notes

Minimize all GND bond wire lengths

Minimize IN, OUT and OUTB bond wire lengths

Maintain symmetry between IN and OUT/OUTB bond wires

## ASSEMBLY RECOMMENDATIONS

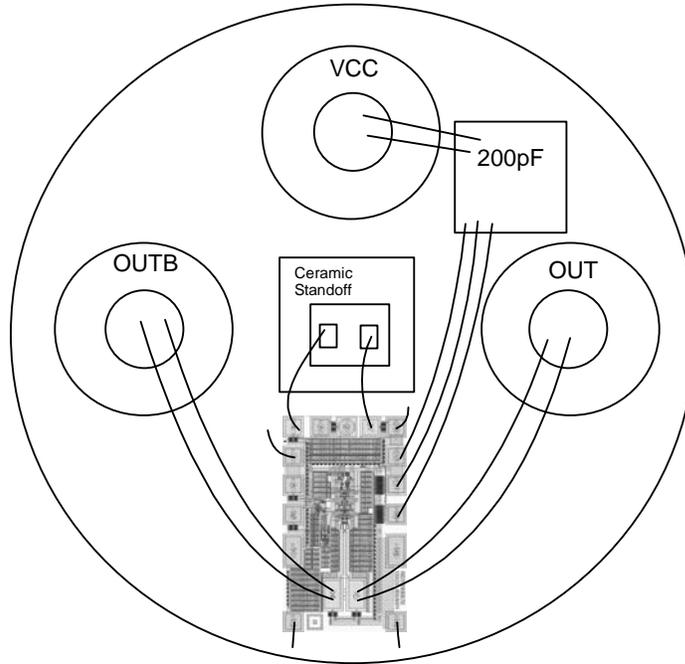


Figure 4. Recommended Layout for 4 pin TO-46

1× Vendor-Specific (0.3 mm × 0.3 mm) 4.25 Gbps Photo Diode

1× ADN2882 (0.7 mm × 1.2 mm) Analog Devices SiGe 4.25 Gbps Transimpedance Amplifier

1× 200 pF RF single-layer capacitor

1× ceramic standoff

### Notes

Minimize all GND bond wire lengths

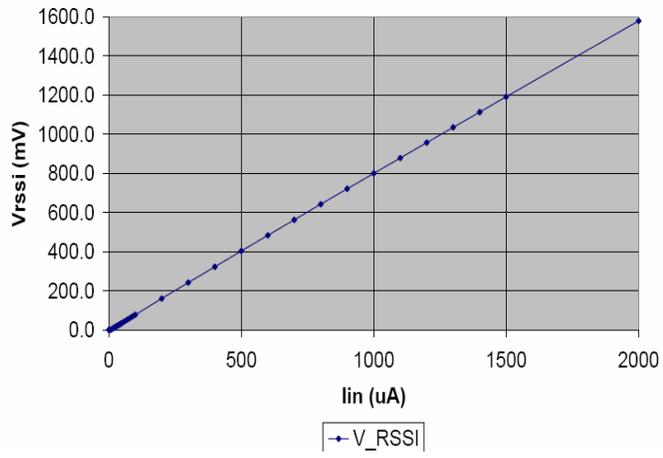
Minimize IN, OUT and OUTB bond wire lengths

Maintain symmetry between IN and OUT/OUTB bond wires



### TYPICAL SIGNAL PERFORMANCE

Mean Vrssi Vs. lin



**ORDERING GUIDE**

<b>Model</b>	<b>Temperature</b>	<b>Package Description</b>	<b>Package Option</b>
ADN2882XCHIPS-WP	-40°C to 95°C	NA	Tested Die