24-Bit, 156 kSPS,112dB ΣΔ ADC, With On-Chip Buffers, Serial Interface

Preliminary Technical Data

AD7765

FEATURES

High performance 24-bit Sigma-Delta ADC
112dB SNR at 78kHz output data rate
109dB SNR at 156 kHz output data rate
156 kHz maximum fully filtered output word rate
Pin-selectable over-sampling rate (128x & 256x)
Flexible SPI serial interface
Fully differential modulator input
On-chip differential amplifier for signal buffering
On-chip Reference Buffer
Low pass FIR filter
Over-range alert pin
Digital gain correction registers
Power down mode
Synchronization of multiple devices via $\overline{\text{SYNC}}$ pin
Daisy Chaining

APPLICATIONS

Data acquisition systems
Vibration analysis
Instrumentation

FUNCTIONAL BLOCK DIAGRAM

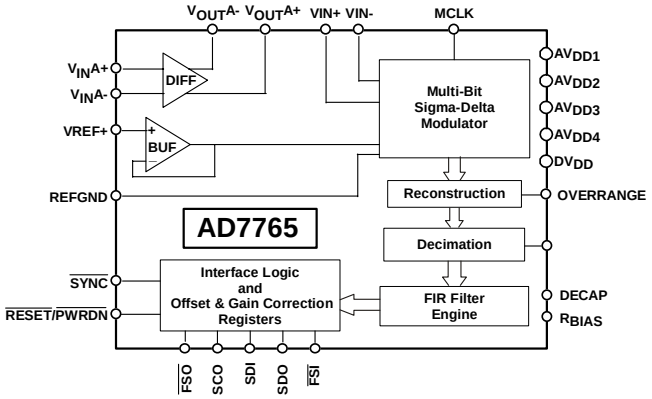

Figure 1.

PRODUCT OVERVIEW

The AD7765 high performance, 24-bit, sigma delta analog to digital converter combines wide input bandwidth, high speed and performance of 112dB at a 156Khz output data rate with the benefits of sigma delta conversion, while, also offering excellent DC specifications which make the converter ideal for high speed data acquisition of AC signals where DC data is also a requirement.

A wide dynamic range combined with significantly reduced anti-aliasing requirements simplifies the design process. The AD7765 offers pin-selectable decimation rates of 128x and 256x. Other features include an integrated buffer to drive the reference, a differential amplifier for signal buffering and level shifting.

The addition of an internal gain register, an over-range alert pin, and a low-pass digital FIR filter make the AD7765 a compact highly integrated data acquisition device requiring minimal peripheral component selection. The AD7765 is ideally suited to applications demanding high SNR without necessitating design of complex front end signal processing.

The differential input is sampled at up to 40MS/s by an analog modulator. The modulator output is processed by a series of low-pass filters. The sample rate, filter corner frequencies and output word rate are determined by the external clock frequency supplied to the AD7765.

The reference voltage supplied to the AD7765 determines the analog input range. With a 4V reference, the analog input range is ±3.2V differential biased around a common mode of 2V. This common mode biasing can be achieved using the on-chip differential amplifiers, further reducing the external signal conditioning requirements.

The AD7765 is available in a 28-lead TSSOP package and is specified over the industrial temperature range from -40°C to +85°C

RELATED DEVICES

Part no.	Description
AD7760	24-bit, 2.5MSPS, 100dB ΣΔ, parallel interface
AD7762	24-bit, 625ksps, 109dB ΣΔ, parallel interface
AD7763	24-bit, 625ksps, 109dB ΣΔ, serial interface
AD7764	24-bit, 312kSPS, 109dB ΣΔ, serial interface

Rev. PrC

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

SPECIFICATIONS

V_{DD1} = 2.5 V, V_{DD2} = 5 V, V_{REF} = 4.096 V, T_A = +25°C, Using the on-chip amplifier with components as shown in Table 7, unless otherwise noted.[1]

Table 1.

Parameter	Test Conditions/Comments	Specifcation	Unit
DYNAMIC PERFORMANCE			
Decimate by 256	MCLK = 40MHz, ODR = 78.125kHz, FIN = 1kHz Sine Wave		
Dynamic Range	Modulator inputs shorted	TBD	dB min
		115	dB typ
Signal to Noise Ratio (SNR)[2]		112	dB typ
Spurious Free Dynamic Range (SFDR)		TBD	dBFS typ
Total Harmonic Distortion (THD)	Input Amplitude = -0.5dB	-105	dB typ
	Input Amplitude = -6dB	TBD	dB max
			dB typ
	Input Amplitude = -60dB		dB typ
Decimate by 128	MCLK = 40MHz, ODR = 156.25kHz, FIN =100kHz Sine Wave		
Dynamic Range	Modulator inputs shorted	TBD	dB min
		112	dB typ
Signal to Noise Ratio (SNR)[2]		109	dB typ
Spurious Free Dynamic Range (SFDR)	Non-harmonic		dBFS typ
Total Harmonic Distortion (THD)	Input Amplitude = -0.5dB		dB typ
	Input Amplitude = -6dB	TBD	dB max
			dB typ
Intermodulation Distortion (IMD)	Input Amplitude = -6dB, FINA= TBD KHz, FINB=TBD KHz	TBD	dB typ
DC ACCURACY			
Resolution	Guaranteed monotonic to 24 bits	24	Bits
Integral Nonlinearity		0.00076	LSB typ
Zero Error		0.014	% typ
		0.02	% max
Gain Error		0.018	% typ
Zero Error Drift		0.00001	%FS/°C typ
Gain Error Drift		0.0002	%FS/°C typ
DIGITAL FILTER RESPONSE			
Decimate by 256			
Group Delay	MCLK = 40MHz	358	µS typ
Decimate by 128			
Group Delay	MCLK = 40MHz	177	µS typ
ANALOG INPUT			
Differential Input Voltage	Vin(+) – Vin(-), V_{REF} = 2.5V	±2	V pk-pk
	Vin(+) – Vin(-), V_{REF} = 4.096V	±3.25	V pk-pk
Input Capacitance	At internal buffer inputs	5	pF typ
	At modulator inputs	55	pF typ
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage	V_{DD3} = 5V ± 5%	+4.096	Volts
V_{REF} Input DC Leakage Current		±1	µA max
V_{REF} Input Capacitance		5	pF max

Parameter	Test Conditions/Comments	Specifcation	Unit
POWER DISSIPATION			
Total Power Dissipation		TBD	mW max
POWER REQUIREMENTS			
AV_{DD1} (Modulator Supply)	±5%	+2.5	Volts
AV_{DD2} (General Supply)	±5%	+5	Volts
AV_{DD3} (Diff-Amp Supply)		+3.15/+5.25	V min/max
AV_{DD4} (Ref Buffer Supply)		+3.15/+5.25	V min/max
DV_{DD}	±5%	+2.5	Volts
AI_{DD1} (Modulator)		TBD	mA typ
AI_{DD2} (General)		TBD	mA typ
AI_{DD4} (Reference Buffer)	AV_{DD4} = +5V	10	mA typ
AI_{DD3} (Diff Amp)	AV_{DD3} = 5V	10	mA typ
D_{IDD}	Clock Stopped	TBD	mA typ
DIGITAL I/O			
MCLK Input Amplitude[3]		5	V typ
Input Capacitance		7.3	pF typ
Input Leakage Current		±1	µA/pin max
Three-State Leakage Current (SDO)		±1	µA max
V_{INH}		TBD	V min
V_{INL}		TBD	V max
V_{OH}[4]		1.5	V min
V_{OL}		0.1	V max

[1] See Terminology section
[2] SNR specifications in dBs are referred to a full-scale input, FS. Tested with an input signal at 0.5dB below full scale, unless otherwise specified.
[3] While the AD7764 can function with an MCLK amplitude of less than 5 V, this is the recommended amplitude to achieve the performance as stated.
[4] Tested with a 400µA load current.

TIMING SPECIFICATIONS

Table 2. AV_{DD1} = DV_{DD} = 2.5 V, AV_{DD2} = AV_{DD3} = AV_{DD4} = 5 V, V_{REF} = 4.096 V, T_A = +25°C, C_{LOAD} = 25pF.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{MCLK}	500	KHz min	Applied Master Clock Frequency
	40	MHz max	
f_{ICLK}	250	kHz min	Internal Modulator Clock Derived from MCLK.
	20	MHz max	
t_1	$1 \times t_{ICLK}$	typ	SCO High Period
t_2	$1 \times t_{ICLK}$	typ	SCO Low Period
t_3	TBD	typ	SCO rising edge to FSO falling edge
t_4	TBD	typ	Data Access time, $\overline{FSO}$ falling edge to data active
t_5	TBD	ns max	Initial Data Access Time, SDO active to SDO valid
t_6	TBD	ns min	SDO valid to SCO Rising Edge
t_7	TBD	ns max	SCO rising edge to SDO valid
t_8	TBD	typ	SCO rising edge to $\overline{FSO}$ rising edge
t_9	TBD	typ	$\overline{FSO}$ rising edge to SDO invalid
t_{10}	TBD × t_{SCO}	max	$\overline{FSO}$ Low Period
t_{11}	TBD	min	$\overline{FSI}$ Low Period
t_{12}[1]	TBD	max	$\overline{FSI}$ Low Period
t_{13}	TBD	min	SCO rising edge to SDI valid
t_{14}	TBD	min	SDI valid to SCO rising edge
t_{15}	TBD	max	SCO rising edge to SDI valid
t_{16}	TBD	min	$\overline{FSI}$ rising edge to SDI three-state

[1] This is the max time $\overline{FSI}$ can be held low when writing to an individual (non-daisy chained) AD7764 device.

TIMING DIAGRAMS

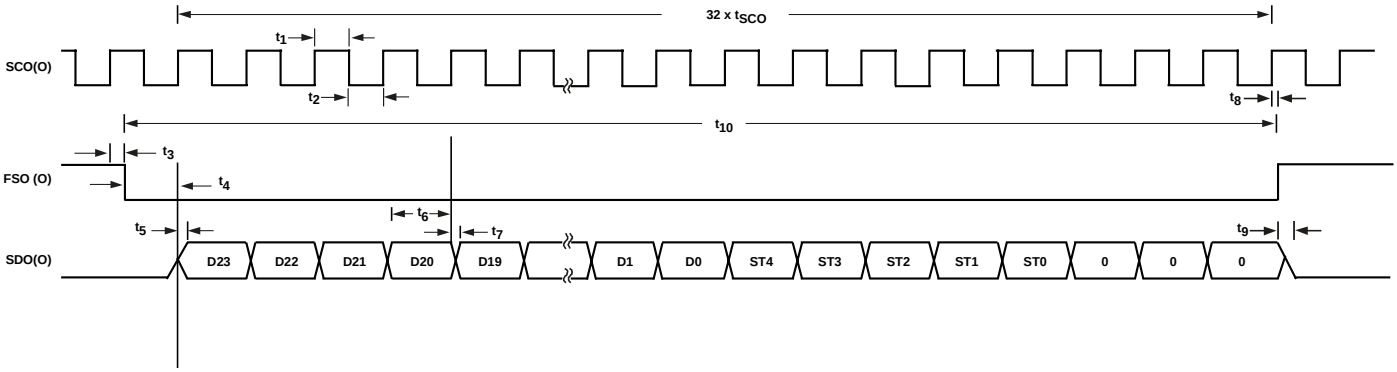

Figure 2. Serial Read Timing Diagram

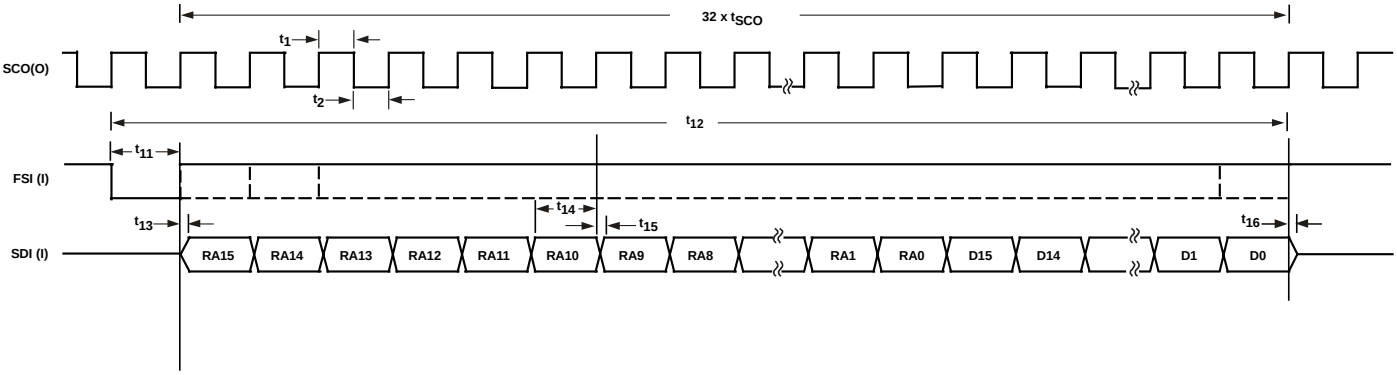

Figure 3. AD7765 Register Write

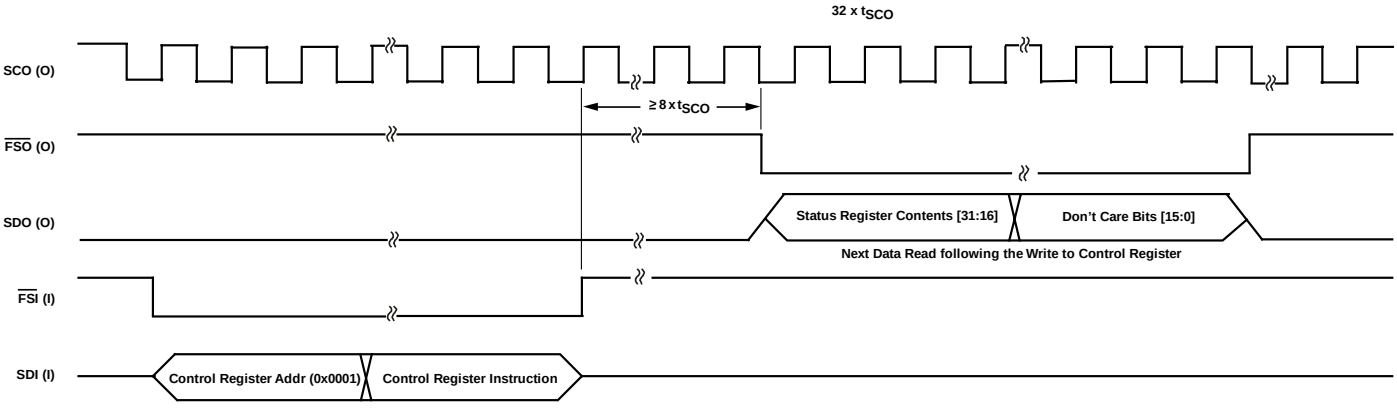

Figure 4.AD7765 Register read cycle

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 3

Parameters	Rating
AV_{DD1} to GND	−0.3 V to +2.8 V
(AV_{DD2}, AV_{DD3}, AV_{DD4}) to GND	−0.3 V to +6 V
DV_{DD} to GND	−0.3 V to +2.8 V
$V_{IN}A_+$, $V_{IN}A_-$ to GND[1]	−0.3 V to +6 V
V_{IN+}, V_{IN-} to GND[1]	−0.3 V to +6 V
Digital input voltage to GND[2]	−0.3 V to +2.8 V
V_{REF} to GND[3]	−0.3 V to +6 V
AGND to DGND	−0.3 V to +0.3 V
Input current to any pin except supplies[4]	TBD
Operating temperature range	
Commercial	−40°C to +85°C
Storage temperature range	−65°C to +150°C
Junction temperature	150°C
TSSOP Package	
θ_{JA} thermal impedance	143°C/W
θ_{JC} thermal impedance	45°C/W
Lead temperature, soldering	
Vapor phase (60 secs)	215°C
Infrared (15 secs)	220°C
ESD	TBD kV

[1] Absolute maximum voltage for V_{IN-}, V_{IN+} and V_{INA-}, V_{INA+} is 6.0V or AV_{DD3}+0.3V, whichever is lower.

[2] Absolute maximum voltage on digital inputs is 3.0V or DV_{DD}+ 0.3V, whichever is lower.

[3] Absolute maximum voltage on V_{REF} input is 6.0V or AV_{DD4} + 0.3V, whichever is lower.

[4] Transient currents of up to TBD mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

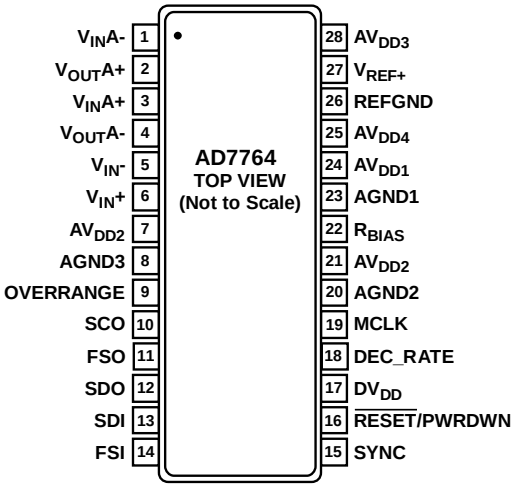

Figure 5. 28-Lead TSSOP Pin Configuration

Table 4. Pin Function Descriptions

Pin Number	Pin Mnemonic	Description
24	AV_{DD1}	+2.5V power supply to the modulator. This pin should be decoupled to pin TBD with a TBDnF capacitor.
7, 21	AV_{DD2}	+5V power supply. Pin 7 should be decoupled to AGND3(pin 8) with a TBD nF capacitor. Pin 21 should be decoupled to AGND1 (pin 23) with a TBD nF capacitor.
28	AV_{DD3}	+3.3V to +5V power supply for on-board differential ampifier. This pin should be decoupled to AGND1 (pin TBD) with a TBDnF capacitor.
25	AV_{DD4}	+3.3V to +5V power supply for on-board reference buffer. This pin should be decoupled to REFGND (pin TBD) with a TBDnF capacitor.
17	DV_{DD}	+2.5V power supply for digital circuitry and FIR filter. This pin should be decoupled to the ground plane with a TBDnF capacitor.
22	R_{BIAS}	Bias Current setting pin. A resistor must be inserted between this pin and AGND. For more details on this, see the Bias Resistor Section.
23	AGND1	Power Supply ground for analog circuitry.
20	AGND2	Power Supply ground for analog circuitry.
8	AGND3	Power Supply ground for analog circuitry.
26	REFGND	Reference Ground. Ground connection for the reference voltage.
27	V_{REF+}	Reference Input. The input range of this pin is determined by the reference buffer supply voltage (AV_{DD4}). See Reference Section for more details.
1	$V_{IN}A-$	Negative Input to Differential Amplifier.
2	$V_{OUT}A+$	Positive Output from Differential Amplifier.
3	$V_{IN}A+$	Positive Input to Differential Amplifier.
4	$V_{OUT}A-$	Negative Output from Differential Amplifier.
5	$V_{IN}-$	Negative Input to the Modulator.
6	$V_{IN}+$	Positive Input to the Modulator.
9	OVERRANGE	When this pin outputs a logic high it indicates that the analog input is out of range . This occurs when the magnitude of the differential input is greater than V_{REF}
10	SCO	Serial Clock Out. This clock signal is derived from the internal ICLK signal. The frequency of this clock is equal to ICLK. See the AD7765 Interface section for further details.
11	$\overline{FSO}$	Frame Sync Out. This signal frames the serial data output and is 32 SCO periods wide.

Pin Number	Pin Mnemonic	Description
12	SDO	Serial Data Out. Address, Status and Data bits are clocked out on this line during each serial transfer. Each bit is clocked out on an SCO rising edge and valid on the falling edge. See the AD7765 Interface section for further details.
13	SDI	Serial Data In. The first data bit (MSB) must be valid on the next SCO falling edge after the $\overline{FSI}$ event has been latched. 32 bits are required for each write; the first 16-bit word contains the device and register address and the second word contains the data. See the AD7765 Interface section for further details.
14	$\overline{FSI}$	Frame Sync In. The status of this pin is checked on the falling edge of SCO. If this pin is low then the first data bit is latched in on the next SCO falling edge. See the AD7765 Interface section for further details.
15	$\overline{SYNC}$	Synchronization Input. A falling edge on this pin resets the internal filter. This can be used to synchronize multiple devices in a system. See the AD7765 Interface section for further details.
16	$\overline{RESET}$/$\overline{PWDN}$	When a logic low is sensed on this pin, the part is powered down and all internal circuitry is reset.
19	MCLK	Master Clock Input. A low jitter digital clock must be applied to this pin. The output data rate will depend on the frequency of this clock. See Clocking the AD7765 Section for more details.
18	DEC_RATE	This pin selects which of the two decimation modes the AD7765 operates. When logic high is applied to this pin, decimate by 128 mode is selected. Decimate by 256 is selected when by applying logic low to the pin.

TERMINOLOGY

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7763, it is defined as

$$THD(\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Nonharmonic Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component, excluding harmonics.

Dynamic Range
The ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7765 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used.

In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dB.

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero Error
The zero error is the difference between the ideal midscale input voltage (when both inputs are shorted together) and the actual voltage producing the midscale output code.

Zero Error Drift
The change in the actual zero error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

Gain Error
The first transition (from 100…000 to 100…001) should occur for an analog voltage 1/2 LSB above the nominal negative full scale. The last transition (from 011…110 to 011…111) should occur for an analog voltage 1 1/2 LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition, from the difference between the ideal levels.

Gain Error Drift
The change in the actual gain error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

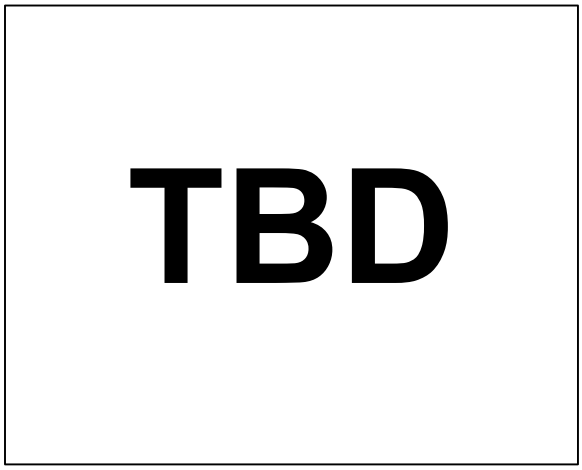

Figure 6

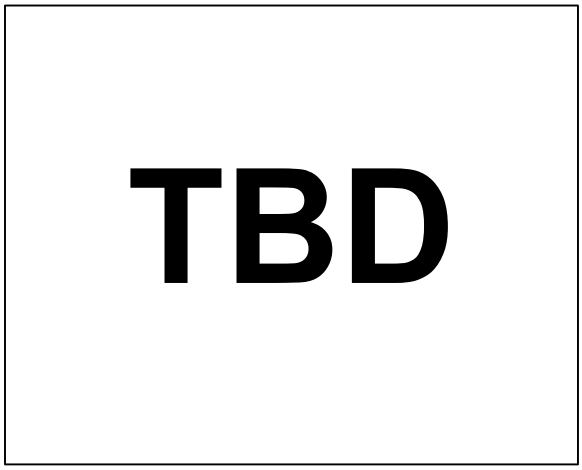

Figure 9

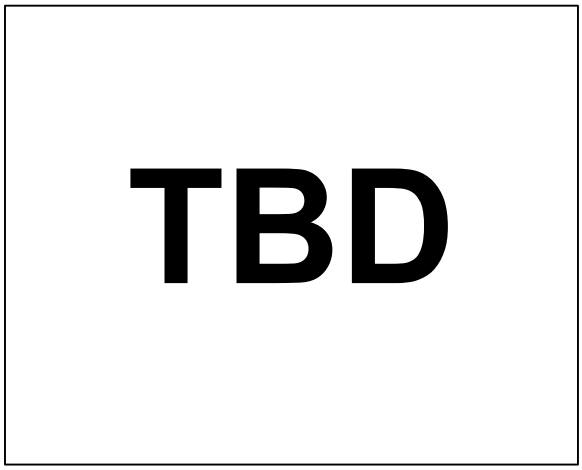

Figure 7

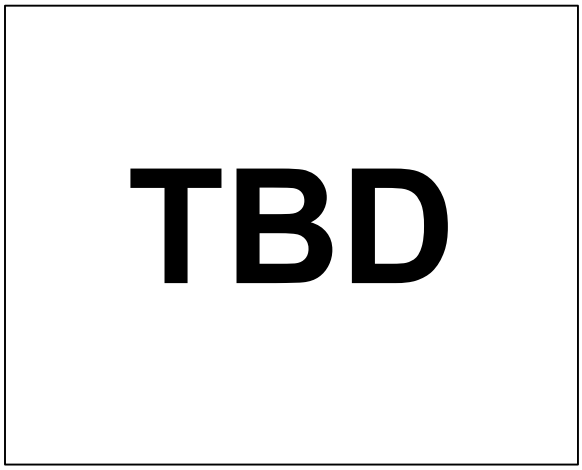

Figure 10

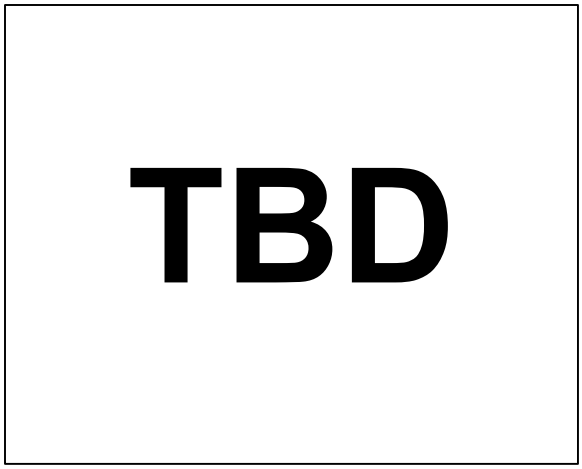

Figure 8

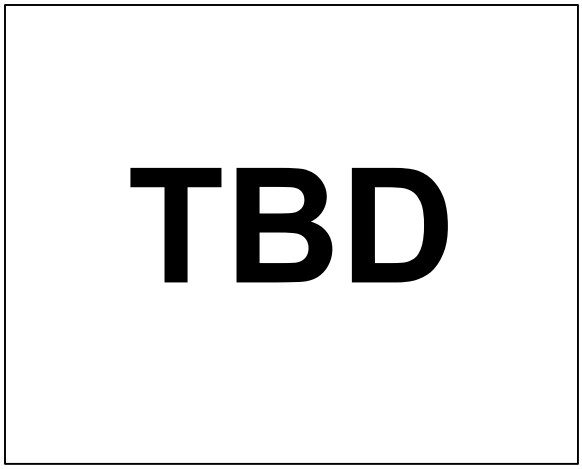

Figure 11

THEORY OF OPERATION

The AD7765 employs a sigma-delta conversion technique to convert the analog input into an equivalent digital word. The modulator samples the input waveform and outputs an equivalent digital word to the digital filter at a rate equal to I_{CLK}.

Due to the high over-sampling rate, which spreads the quantization noise from 0 to f_{ICLK}, the noise energy contained in the band of interest is reduced (Figure 12). To further reduce the quantization noise, a high order modulator is employed to shape the noise spectrum; so that most of the noise energy is shifted out of the band of interest (Figure 13).

The digital filtering which follows the modulator removes the large out-of-band quantization noise (Figure 14) while also reducing the data rate from f_{ICLK} at the input of the filter to $f_{ICLK}/128$ or $f_{ICLK}256$ at the output of the filter, depending on the decimation rate used.

Digital filtering has certain advantages over analog filtering. It does not introduce significant noise or distortion and can be made perfectly linear phase.

The AD7765 employs three Finite Impulse Response (FIR) filters in series. By using different combinations of decimation ratios, data can be obtained from the AD7765 at two data rates. The first filter receives data from the modulator at ICLK MHz where it is decimated by four to output data at (ICLK/4) MHz.

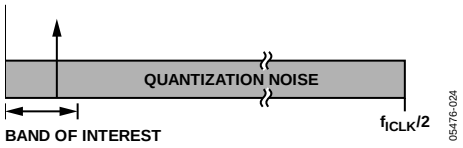

Figure 12. Σ-Δ ADC, Quantization Noise

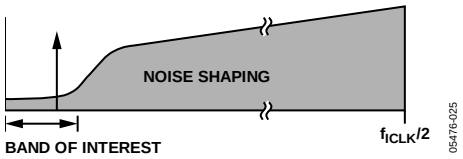

Figure 13. Σ-Δ ADC, Noise Shaping

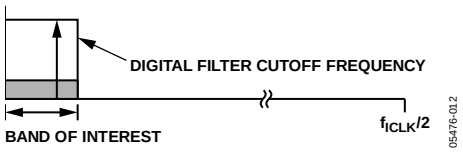

Figure 14 Σ-Δ ADC, Digital Filter Cutoff Frequency

The second filter allows the decimation rate to be chosen from either 16x or 32x. The third filter has a fixed decimation rate of 2x. Table 5 below shows some characteristics of the digital filtering (See Clocking the AD7765 for details on ICLK).The group delay of the filter is defined to be the delay to the centre of the impulse response and is equal to the computation + filter delays. The delay until valid data is available (the DVALID status bit is set) is equal to 2x the filter delay + the computation delay.

Table 5. Configuration With Default Filter

ICLK Frequency	Decimation Rate	Data State	Computation Delay	Filter Delay	Passband Bandwidth	Output Data Rate (ODR)
20 MHz	128x	Fully Filtered	3.1µS	174µS	62.5 kHz	156.25 kHz
20 MHz	256x	Fully Filtered	4.65µS	346.8µS	31.25 kHz	78.125 kHz
12.288MHz	128x	Fully Filtered	5.05µS	283.2µS	38.4 kHz	96 kHz
12.288MHz	256x	Fully Filtered	7.57µS	564.5µS	19.2 kHz	48 kHz

AD7765 INTERFACE

READING DATA

The AD7765 uses an SPI compatible serial interface. The timing diagram in Figure 2 shows how the AD7765 transmits its conversion results.

The data being read from the AD7765 is clocked out using the serial clock output, SCO. The SCO frequency is half that of the MCLK input to the AD7765.

The conversion result output on the serial data output (SDO) line is framed by the frame synchronization output, $\overline{FSO}$, which is sent logic low for 32 SCO cycles. Each bit of the new conversion result is clocked onto the SDO line on the rising SCO edge and is valid on the falling SCO edge. The 32-bit result consists of the 24 data bits which, are followed by 5 status bits followed by a further 3 zeros. The five status bits are :

D7				D3
DVALID	OVR	LPWR	Dec_Rate 1	Dec_Rate 0

WRITING TO THE AD7765

The AD7765 write operation is shown in Figure 3. The serial writing operation is synchronous to the SCO signal. The status of the frame sync input,$\overline{FSI}$, is checked on the falling edge of the SCO signal. If the $\overline{FSI}$ line is low then the first data bit on the serial data in (SDI) line is latched in on the next SCO falling edge.

The active edge of the $\overline{FSI}$ signal should be set to occur at a position when the SCO signal is high or low, which allows set-up and hold time from the SCO falling edge to be met. The width of the $\overline{FSI}$ signal may be set to between 1 and 32 SCO periods wide. A second or subsequent $\overline{FSI}$ falling edge which occurs before 32 SCO periods have elapsed will be ignored.

Figure 3 details the format for the serial data being written to the AD7765, through the SDI pin. 32 bits are required for a write operation. The first 16 bits are used to select the register address that the data being read is intended for. The second 16 bits contain the data for the selected register.

Writing to AD7765 should be allowed at any time even while reading a conversion result. It should be noted that after writing to the devices, valid data will not be output until after the settling time for the filter has elapsed. The DVALID status bit is asserted at this point to indicate that the filter has settled and that valid data is available at the output.

READING STATUS AND OTHER REGISTERS

The AD7765 features a programmable control registers and a read-only status register. To read back the contents of these registers, the user must first write to the control register of the device, setting a bit corresponding to the register to be read. The next read operation then outputs the contents of the selected register instead of a conversion result.

To ensure that the next read cycle contains the contents of the register that has been written to, the write operation to the register in question must be completed a minimum of $8 \times t_{SCO}$ before the falling edge of $\overline{FSO}$, which indicates the start of the next read cycle. See Figure 4 for details.

Information on the relevant bits that must be set in the control register are provided in the AD7765 Registers section.

SYNCHRONISATION

The $\overline{SYNC}$ input to the AD7765 provides a synchronization function that allows the user to begin gathering samples of the analog front-end input from a known point in time.

The $\overline{SYNC}$ function allows multiple AD7765s, operated from the same master clock and using the same $\overline{SYNC}$ signal, to be synchronized so that each ADC simultaneously updates its output register.

Using a common $\overline{SYNC}$ signal to all AD7765 devices in a system allows synchronization to occur. On the falling edge of the $\overline{SYNC}$ signal the digital filter sequencer is reset to 0. The filter is held in reset state until a rising edge of the SCO senses $\overline{SYNC}$ high. Thus, to perform a synchronization of devices, a $\overline{SYNC}$ pulse of a minimum of 2.5 ICLK cycles in length can be applied, synchronous to the falling edge of SCO. On the first rising edge of SCO after $\overline{SYNC}$ goes logic high, the filter is taken out of reset, and the multiple parts gather input samples synchronously.

Following a $\overline{SYNC}$, the digital filter needs time to settle before valid data can be read from the AD7765. The user knows there is valid data on the SDO line by checking the DVALID status bit (see D7 in the status bits listing) that is output with each conversion result. The time from the rising edge of SYNC until the DVALID bit is asserted is dependent on the filter configuration used. See the Theory of Operation section and the figures listed in Table 5 for details on calculating the time until DVALID is asserted.

DAISY CHAINING

Daisy chaining devices allows numerous devices to use the same digital interface lines. This feature is especially useful for reducing component count and wiring connections, e.g. in isolated multi-converter applications or for systems with a limited interfacing capacity. Data read-back is analogous to clocking a shift register.

The block diagram in Figure 15 shows the way in which devices must be connected in order to achieve daisy chain functionality. Figure 15 shows four AD7765 devices daisy chained together with a common MCLK signal applied, will work for both decimate by 128 or 256 modes.

Reading Data in Daisychain Mode

The SDO line of AD7765 (A) provides the output data from the chain of AD7765 converters. The last device in the chain (AD7765(D) in Figure 15) will have its Serial Data In (SDI) pin connected to ground. All the devices in the chain must use common MCLK and SYNC signals.

To enable the daisy chain conversion process, apply a common $\overline{\text{SYNC}}$ pulse to all devices (see synchronization of devices).

After applying a $\overline{\text{SYNC}}$ pulse to all the devices there is a delay of TBD SCO periods before valid conversion data appears at the output of the chain of devices. As shown in Figure 16 the first conversion result is output from the device labeled AD7765(A). This 32-bit conversion result is then followed by the conversion results from the devices B,C and D respectively with all conversion results output in an MSB first sequence. The signals output from the daisy chain are the stream of conversion results from the SDO pin of AD7765(A) and the FSO signal also output by the first device in the chain (AD7765(A)).

The falling edge of FSO signals the MSB of the first conversion output in the chain. FSO stays logic low throughout the 32 SCO clock periods needed to output the AD7765(A) result and thereafter goes logic high during the output of the conversion results from the devices B,C, and D.

The maximum number of devices that can be daisy chained is dependent on the decimation rate the user selects. The max number of devices that can be daisy chained can be calculated simply by dividing the chosen decimation rate by 32(the number of bits that must be clocked out for each conversion). Table 6 shows give the maximum number of chained devices for each decimation rate.

Table 6 Maximum length of device chain for all decimation rates

Decimation Rate	Maximum length of chain
x256	8
x128	4

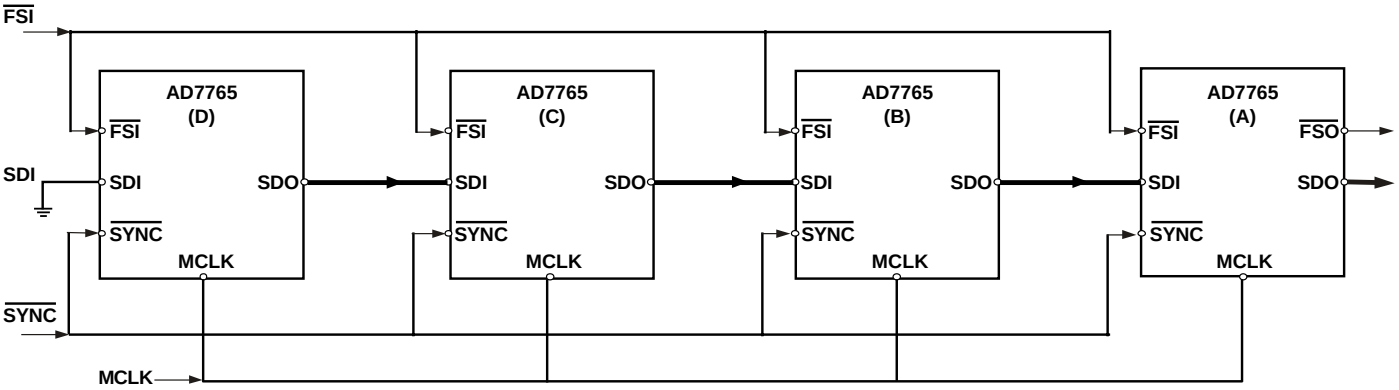

Figure 15. Daisy Chaining 4xAD7765 devices in decimate by 128 mode using a 40Mhz MCLK signal.

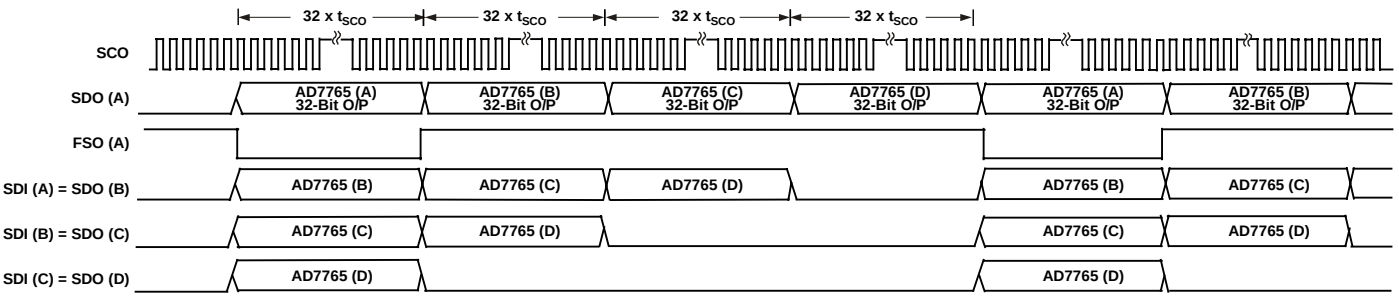

Figure 16. Daisychain mode, Data read timing diagram (for daisychain configuration shown in Figure 15).

Writing Data in Daisychain Mode

Writing to AD7765 devices in daisy chain mode is similar to writing to a single device. The serial writing operation is synchronous to the SCO signal. The status of the frame sync input,$\overline{FSI}$, is checked on the falling edge of the SCO signal. If the $\overline{FSI}$ line is low then the first data bit on the serial data in (SDI) line is latched in on the next SCO falling edge.

Writing data to the AD7765 in Daisy Chain mode operates with the same timing structure as per writing to a single device as shown in Figure 3. The difference between writing to a single device and a number of daisychained devices is in the implementation of the $\overline{FSI}$ signal. The number of devices that are in the daisy chain determines the period for which the $\overline{FSI}$ signal must remain logic low. If the user wishes to write to n number of devices in the daisy chain, the period between the falling edge of $\overline{FSI}$ and the rising edge of $\overline{FSI}$ must be be between 32 x (n-1) to 32 x n, SCLK periods. For example, if three AD7765 devices are being written to in Daisychain mode $\overline{FSI}$ is logic low for between 32 x(3-1) to 32 x 3 SCLK pulses. i.e. the rising edge of FSI must occur between the 64th and 96th SCO period.

The AD7765 devices may be written to at any time. The falling edge of $\overline{FSI}$ overrides all attempts to read data from the SDO pin. In the case of a daisy chain the $\overline{FSI}$ signal remaining logic low for more than 32 SCO periods will indicate to the AD7765 device that there are more devices further on in the chain. This means the AD7765 in question will direct data that is input on the SDI pin to its SDO pin. This ensures that data is passed to the next device in the chain. Synchronise all the AD7765 devices in the chain after the write is completed.

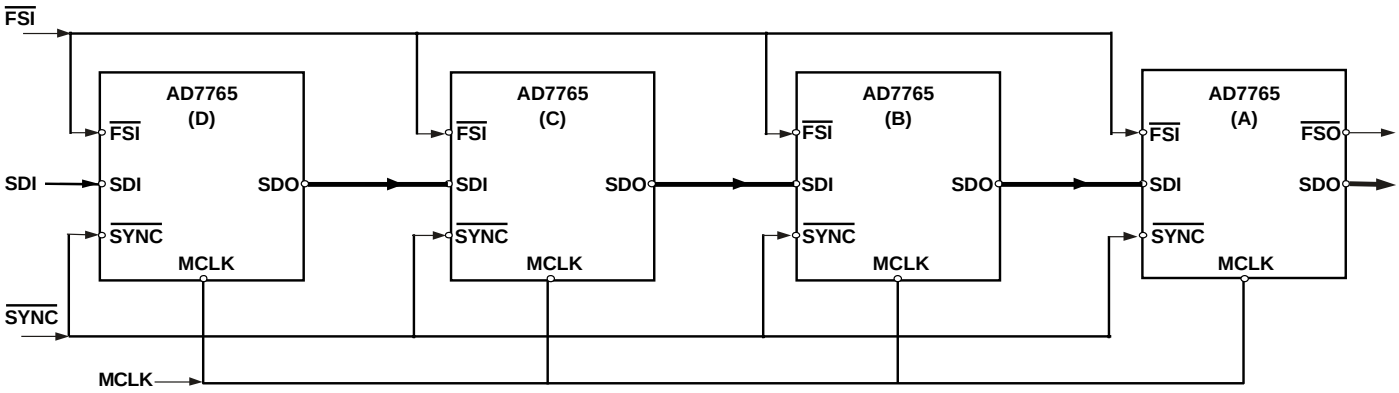

Figure 17.Writing to AD7765 Daisy chain configuration

CLOCKING THE AD7765

The AD7765 requires an external low jitter clock source. This signal is applied to the MCLK pin. An internal clock signal (ICLK) is derived from the MCLK input signal. This ICLK controls all the internal operation of the AD7765. The maximum ICLK frequency is 20MHz. The ICLK is generated as follows:

ICLK = MCLK/2

If the user wishes to get output data rates equal to those used in audio systems, a 12.288 MHz ICLK frequency can be used. As shown in Table 5, output data rates of 96kHz and 48kHz are achievable with this ICLK frequency.

The MCLK jitter requirements depend on a number of factors and are given by the following equation:

$$t_{j(RMS)} = \frac{\sqrt{OSR}}{2 \times \pi \times f_{IN} \times 10^{\frac{SNR(dB)}{20}}}$$

Where:

OSR = Over-sampling ratio = $\frac{f_{ICLK}}{ODR}$

f_{IN} = Maximum Input Frequency

SNR(dB) = Target SNR.

EXAMPLE 1

This example can be taken from Table 5, where:

ODR = 156.25 kHz
f_{ICLK} = 20MHz
f_{IN} (max) = 78.125 kHz
SNR = 109dB

$$t_{j(RMS)} = \frac{\sqrt{128}}{2 \times \pi \times 78.125 \times 10^3 \times 10^{5.45}} = 81.77\,ps$$

This is the maximum allowable clock jitter for a full-scale 78.125kHz input tone with the given ICLK and Output Data Rate.

EXAMPLE 2

Taking a second example from Table 5, where:

ODR = 48kHz
f_{ICLK} = 12.288MHz
f_{IN} (max) = 19.2kHz
SNR = 112dB

$$t_{j(RMS)} = \frac{\sqrt{256}}{2 \times \pi \times 19.2 \times 10^3 \times 10^{5.75}} = 333\,ps$$

The input amplitude also has an effect on these jitter figures. If, for example, the input level was 3dB down from full-scale , the allowable jitter would be increased by a factor of √2 increasing the figure calculated in the first example from 81.77ps to 115.64ps RMS. This is because the maximum slew rate is reduced by a reduction in amplitude. Figure 18 and Figure 19 illustrate this point showing the maximum slew rate of a sine wave of the same frequency but with different amplitudes.

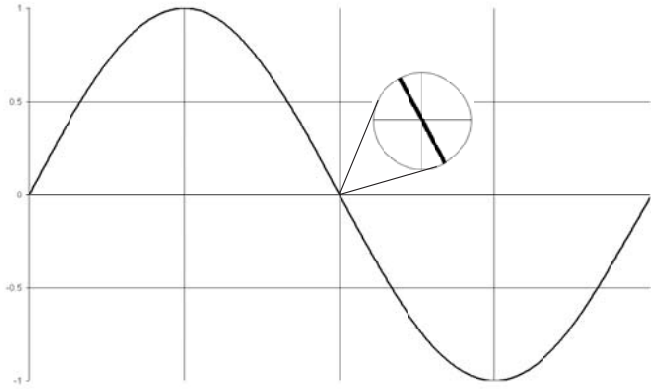

Figure 18. Maximum Slew Rate of Sine Wave with Amplitude of 2V Pk-Pk

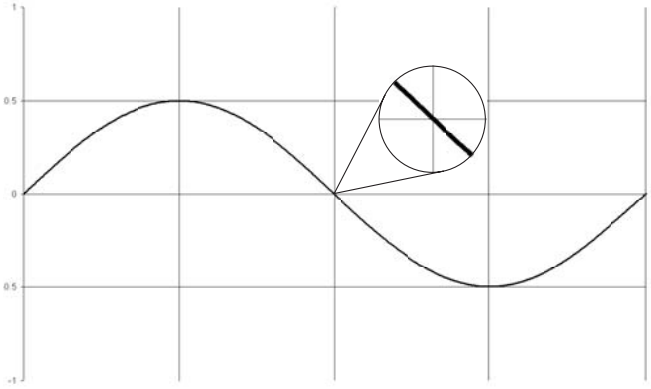

Figure 19. Maximum Slew Rate of Same Frequency Sine Wave with Amplitude of 1V Pk-Pk

DRIVING THE AD7765

The AD7765 has an on-chip differential amplifier. This amplifier will operate with a supply voltage (AV_{DD3}) from 3V to 5.5V. For a 4.096V reference, the supply voltage must be 5V.

To achieve the specified performance in normal power mode, the differential amplifier should be configured as a first order anti-alias filter as shown in Figure 20. Any additional filtering should be carried out in previous stages using low noise, high-performance op-amps such as the AD8021.

Suitable component values for the first order filter are listed in Table 7. Using the first row as an example would yield a 10dB attenuation at the first alias point of 19MHz.

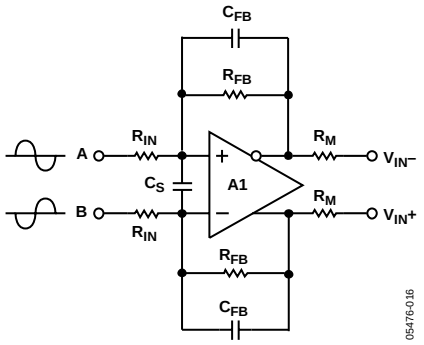

Figure 20. Differential Amplifier Configuration

Table 7.First-Order Filter Component Values

V_{REF}	R_{IN}	R_{FB}	R_M	C_S	C_{FB}
4.096v	4.75kΩ	3.01kΩ	43Ω	1.2pF	33pF

Figure 21 shows the signal conditioning that occurs using the circuit in Figure 20 with a ±2.5V input signal biased around ground using the component values and conditions in Table 7.

The differential amplifier will always bias the output signal to sit on the optimum common mode of $V_{REF}/2$, in this case 2.048V. The signal is also scaled to give the maximum allowable voltage swing with this reference value. This is calculated as 80% of V_{REF}, i.e. $0.8 \times 4.096V \approx 3.275V$ peak to peak on each input.

To obtain maximum performance from the AD7765, it is advisable to drive the ADC with differential signals. Figure 22 shows how a bipolar, single-ended signal biased around ground can drive the AD7765 with the use of an external op amp, such as the AD8021

With a 4.096 V reference, a 5 V supply must be provided to the reference buffer (AV_{DD4}).

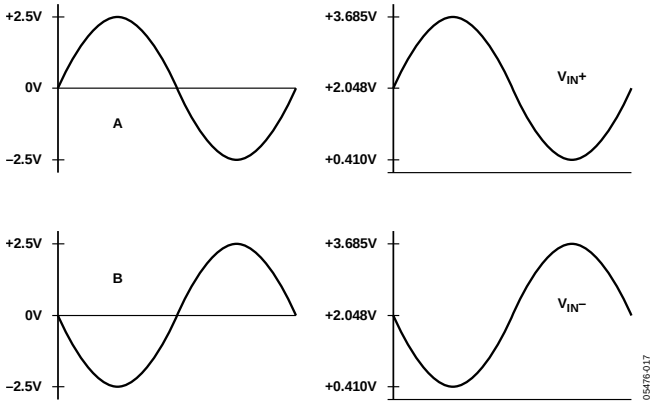

Figure 21. Differential Amplifier Signal Conditioning.

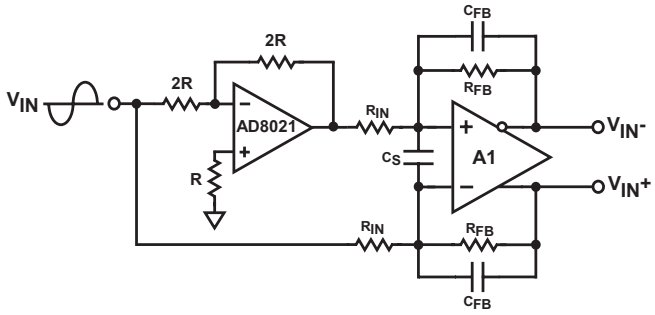

Figure 22. Single Ended to Differential Conversion

The AD7765 employs a double sampling front end,as shown in Figure Figure 23. For simplicity, only the equivalent input circuitry for V_{IN+} is shown. The equivalent circuitry for V_{IN-} is the same.

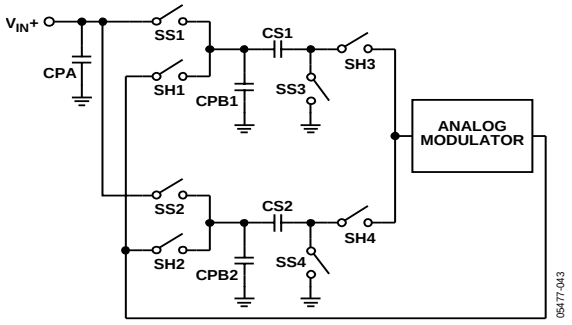

Figure 23. Equivalent Input Circuit

The sampling switches SS1 and SS3 are driven by ICLK, whereas, the sampling switches SS2 and SS4 are driven by $\overline{\text{ICLK}}$. When ICLK is high, the analog input voltage is connected to CS1. on the falling edge of ICLK , the SS1 and SS3 switches open and the analog input is sampled on CS1. Similarly, when ICLK is low, the analog input voltage is connected to CS2. On the rising edge of ICLK, the SS2 and SS4 switches open, and the analog input is sampled on CS2.

Capacitors CPA, CPB1 and CPB2 represent parasitic capacitances which include the junction capacitances associated with the MOS switches.

Table 8 Equivalent Component Values

CS1	CS2	CPA	CPB1/2
13pF	13pF	13pF	5pF

USING THE AD7765

The following is the recommended sequence for powering up and using the AD7765.

1. Apply Power
2. Start clock oscillator, applying MCLK
3. Take $\overline{\text{RESET}}$ low for a minimum of 1 MCLK cycle
4. Wait a minimum of 2 MCLK cycles after $\overline{\text{RESET}}$ has been released.
5. In circumstances where multiple parts are being synchronized, a $\overline{\text{SYNC}}$ pulse must be applied to the parts, otherwise no $\overline{\text{SYNC}}$ pulse is required.

Conditions for applying the $\overline{\text{SYNC}}$ pulse:

(a) The issue of a $\overline{\text{SYNC}}$ pulse to the part must not coincide with a write to the part.

(b) Ensure that the $\overline{\text{SYNC}}$ pulse is taken low for a minimum of 2.5 ICLK cycles.

Data can now be read from the part using the default gain and over range threshold values. The conversion data read will not be valid however until the settling time of the filter has passed. When this has occurred, the DVALID status bit read will be set indicating that the data is indeed valid.

Values for gain and over range threshold registers can be written or read at this stage.

BIAS RESISTOR SELECTION

The AD7765 requires a resistor to be connected between the R_{BIAS} pin and AGND. The value for this resistor is dependant on the reference voltage being applied to the device. The resistor value should be selected to give a current of 25μA through the resistor to ground. For a 4.096V reference voltage, the correct resistor value is 160kΩ.

AD7765 REGISTERS

The AD7765 has a number of user-programmable registers. The control register is used to set the functionality of the on-chip buffer and differential amplifier. and also provides the user the option to power down the AD7765. There are also digital gain and over-range threshold registers. Writing to these registers involves writing the register address first, then a 16-bit data word. Register Addresses, details of individual bits and default values are given here:

Table 9 Control Register (Address 0x0001, Default Value 0x001A)

MSB															LSB
0	RD Ovr	RD Gain	0	RD Stat	0	SYNC	0	Bypass Ref	0	0	0	Pwr Down	0	Ref Buf Off	Amp Off

Bit	Mnemonic	Comment
14	RD Ovr[8,9]	Read Overrange. If this bit has been set, the next read operation will output the contents of the Overrange Threshold Register instead of a conversion result.
13	RD Gain[8,9]	Read Gain. If this bit has been set, the next read operation will output the contents of the digital Gain Register.
11	RD Stat[8,9]	Read Status. If this bit has been set, the next read operation will output the contents of the Status Register.
9	SYNC[8]	Synchronize. Setting this bit will initiate in internal synchronisation routine. Setting this bit simultaneously on multiple devices will synchronize all filters.
7	By-Pass Ref	By-passes reference buffer if the buffer is off.
3	Pwr Down	A logic high powers the part down, however, no reset is done. Writing a 0 to this bit powers the part back up.
2	0	Set this bit to logic zero.
1	Ref Buf Off	Asserting this bit powers down the reference buffer.
0	Amp Off	Switches the differential amplifier off.

Table 10. Status Register (Read Only)

MSB															LSB
PART 1	1	DIE 2	DIE 1	DIE 0	DVALID	LPWR	OVR	0	1	0	Ref Buf On	Amp On	0	DEC 1	DEC 0

Bit	Mnemonic	Comment
15,14	PART1:0	Part Number. These bits will be constant for the AD7765.
13 to 11	DIE2:0	Die Number. These bits will reflect the current AD7765 die number for identification purposes within a system.
10	DVALID	Data Valid. This bit corresponds to the DVALID bit in the status word output in the second 16-bit read operation.
9	0	This bit is set to logic zero.
8	OVR	If the current analog input exceeds the current overrange threshold, this bit will be set.
4	Ref Buf On	This bit is set when the reference buffer is in use.
3	Amp On	This bit is set when the input amplifier is in use.
1 to 0	DEC1:0	Decimation Rate. These bits correspond to decimation rate that is in use.

[8] Bits 14 to 11 & bit 9 are self clearing bits.
[9] Only one of the bits may be set in any write operation as they all determine the contents of the next operation.

NON BIT-MAPPED REGISTERS

Gain Register (Address 0x0004, Default Value 0xA000)

The Gain Register is scaled such that 0x8000 corresponds to a gain of 1.0. The default value of this register is 1.25 (0xA000). This gives a full scale digital output when the input is at 80% of V_{REF}. This ties in with the maximum analog input range of ±80% of V_{REF} Pk-Pk.

Over Range Register (Address 0x0005, Default Value 0xCCCC)

The Over Range register value is compared with the output of the first decimation filter to obtain an overload indication with minimum propagation delay. This is prior to any gain scaling or offset adjustment. The default value is 0xCCCC which corresponds to 80% of V_{REF} (the maximum permitted analog input voltage) Assuming V_{REF} = 4.096V, the bit will then be set when the input voltage exceeds approximately 6.55v pk-pk differential. Note that the over-range bit is also set immediately if the analog input voltage exceeds 100% of V_{REF} for more than 4 consecutive samples at the modulator rate.

OUTLINE DIMENSIONS

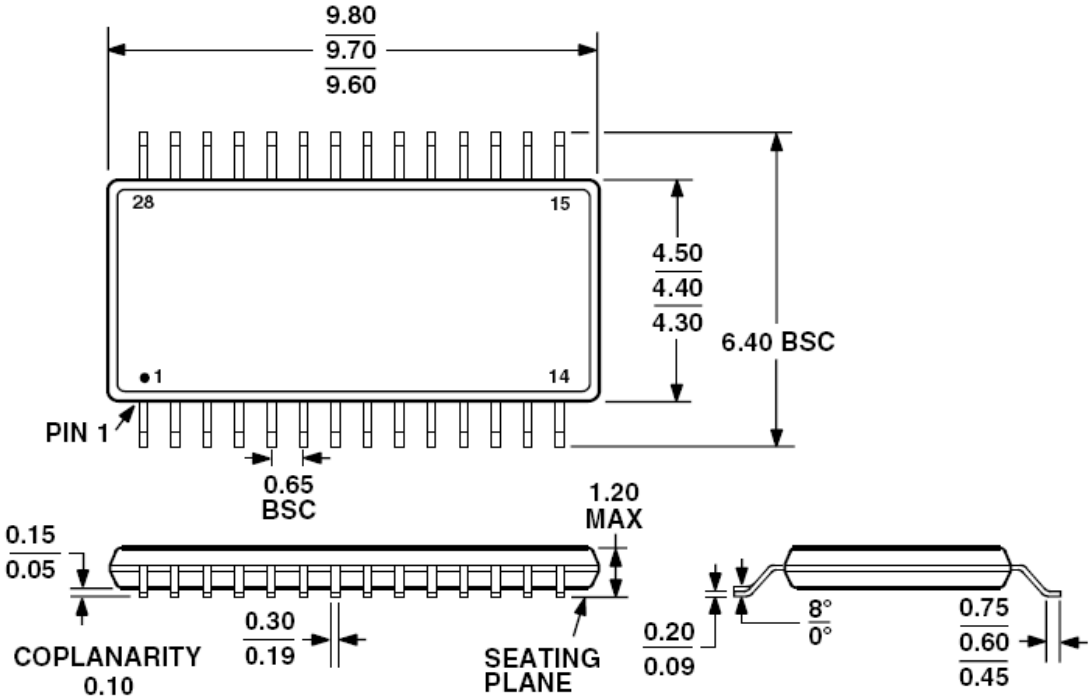

Figure 24. 28-Lead Thin Shrink Small Outline [TSSOP] (RU-28)—Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7765BRUZ	–40°C to +85°C	Thin Shrink Small Outline	RU-28

PR06519-0-11/06(PrC)

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