**Preliminary Data** **CMOS IC**

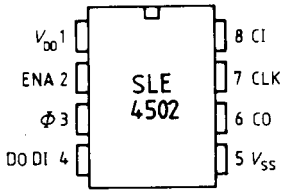
| Type | Ordering Code | Package |
|---|---|---|
| SLE 4502 | Q67100–H8378 | P-DIP-8 |

The SLE 4502 integrated circuit transforms the speed pulses for the SLE 4501 nonvolatile safety counter.

**Features**

- CMOS technology
- Inputs/outputs protected against latch-up
- NMOS-compatible inputs and outputs
- Low standby current (1 µA)
- Schmitt trigger input for counter
- 4-bit miles counter with a programmable prescaler (between 1 and 6,5 536)
- 16-bit register for miles-counter function with external time base
- 16-bit register for trip counter resettable
- Serial three-wire bus
- Power-fail flag
- Extended temperature range from −40 to +110 °C

**Pin Configuration**
(top view)




**Pin Description**

| Pin | Symbol | Function |
|---|---|---|
| 1 | $V_{DD}$ | Supply voltage +5 V |
| 2 | ENA | Enable input |
| 3 | Φ | Clock input for data input/output |
| 4 | DO DI | Data output – data input |
| 5 | $V_{SS}$ | Supply voltage 0 V |
| 6 | CO | Counter output |
| 7 | CLK | Clock input for IC timing |
| 8 | CI | Count pulse input |

## Circuit Description

### 1. Counter Function

The arriving count pulses are sent to the count output via a programmable 16-bit counter and a fixed 4-bit counter. At a 3-MHz clock frequency, the output pulse width is about 42 µs. The contents of the 4-bit counter is readable over the serial interface (first 4 bits).

### 2. Trip Counter

The output pulses of the programmable divider are counted in an additional 16-bit register. This counter is readable and resettable.

### 3. Speedometer

The clock frequency reaches a 16-bit interval counter, which is programmable in a 16-bit register, over a 5-bit prescaler. The speed pulses are counted during an interval and stored in a latch at the end of the interval. This latch may be read at any time.

### 4. Power-Fail Flag

Upon an increase in the supply voltage from 0V to 5V a reset is generated. The power-fail flag indicates this condition. The power-fail flag is reset when it is read out (first bit).

### 5. Instruction Code

| Function | B3 | B2 | B1 | B0 |
|---|---|---|---|---|
| Program divider factor of miles counter | 1 | 1 | 0 | 0 |
| Program divider factor of speedometer | 1 | 0 | 1 | 0 |
| Reset trip counter | 1 | 0 | 0 | 1 |
| Read out miles counter | 0 | 1 | 0 | 0 |
| Read out trip counter | 0 | 0 | 0 | 1 |
| Read out speedometer | 0 | 0 | 1 | 0 |
| Read out power-fail flag | 0 | 1 | 1 | 1 |

## Maximum Ratings

| Description | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | −0.3 | | 6 | V |
| Input voltage | $V_{IM1}$ | −0.3 | | $V_{DD}$ +0.3 | V |
| Power dissipation per output | $P_Q$ | | | 50 | mW |
| Total power dissipation | $P_{tot}$ | | | 150 | mW |
| Storage temperature | $T_{stg}$ | −50 | | 125 | °C |

## Operating Range

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 4.5 | 5 | 5.5 | V |
| DC supply current | $I_{DDS}$ | | | 1 | µA |
| Supply current (see measurement circuit) | $I_{DD}$ | | | 1 | mA |
| Operating frequency | $f_{CLK}$ | 1 | | 3 | MHz |
| Ambient temperature | $T_A$ | −40 | | +110 | °C |

## Characteristics

$T_A = 25\,°C$

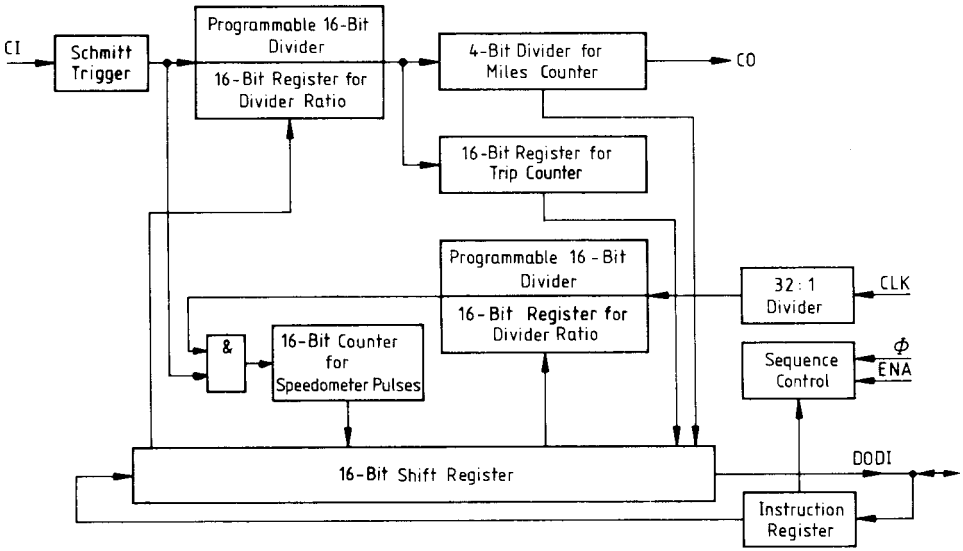
| Description | Symbol | min | max | Unit |
|---|---|---|---|---|
| **All input signals except CI** | | | | |
| H input voltage | $V_{IH}$ | 2.2 | $V_{DD}$ | V |
| L input voltage | $V_{IL}$ | 0 | 0.8 | V |
| Input capacitance | $C_I$ | | 10 | pF |
| L input current | $I_{IL}$ | | 1 | µA |
| H input current | $I_{IH}$ | | 1 | µA |
| **Input signal CI** | | | | |
| H input voltage | $V_{IH}$ | $V_{DD}-1$ | $V_{DD}$ | V |
| L input voltage | $V_{IL}$ | 0 | 1 | V |
| Input cpacitance | $C_I$ | | 10 | pF |
| L input current | $I_{IH}$ | | 1 | µA |
| H input current | $I_{IH}$ | | 1 | µA |
| Hysteresis | $V_{Hy}$ | 1 | 1.5 | V |
| **Output signals** | | | | |
| H output voltage $I_Q = 0.5$ mA | $V_{QH}$ | $V_{DD}-0.4$ | | V |
| L output voltage $I_Q = 1.6$ mA | $V_{QL}$ | | 0.4 | V |

## AC Characteristics

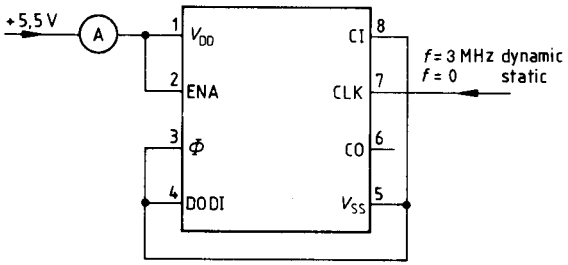
$T_A = 25\,°C$

| | | | | |
|---|---|---|---|---|
| Clock frequency | $f_{CLK}$ | 1 | 3 | MHz |
| Pulse duration CLK | $t_{CLKH}$ | 150 | 600 | ns |
| Pulse spacing CLK | $t_{CLKL}$ | 150 | 600 | ns |
| Pulse duration $\Phi$ | $t_{\Phi H}$ | 500 | | ns |
| Pulse spacing $\Phi$ | $t_{\Phi L}$ | 500 | | ns |
| Enable low to $\Phi$ | $t_{E\Phi}$ | $6/f_{CLK}$ | | |
| $\Phi$ low to enable | $t_{\Phi E}$ | 100 | | ns |
| Data setup | $t_S$ | 100 | | ns |
| Data hold | $t_H$ | 100 | | ns |
| Output delay | $t_D$ | | 150 | ns |
| Enable low to data high-impedance | $t_{HC}$ | | $6/f_{CLK}$ | |
| Output pulse width CO | $t_{CO}$ | $120/f_{CLK}$ | $136/f_{CLK}$ | |
| Pulse duration CI | $t_{CH}$ | $3/f_{CLK}$ | | |
| Pulse spacing CI | $t_{CL}$ | $3/f_{CLK}$ | | |
| Clock frequency at CI | $f_{CI}$ | | $f_{CLK}/6$ | |

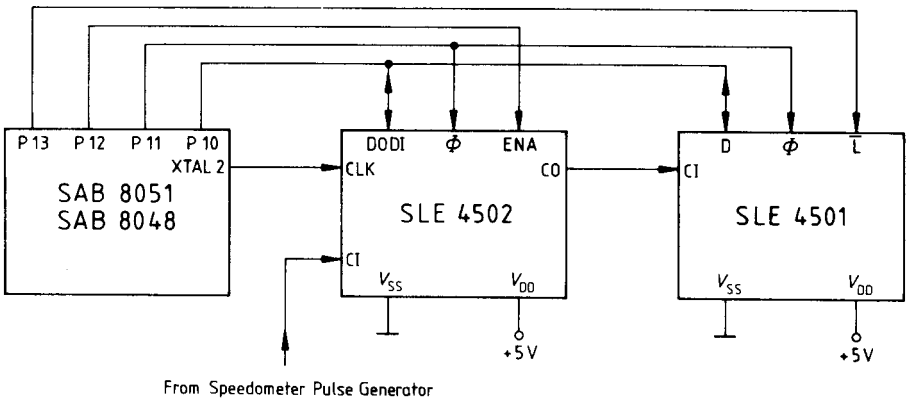
**Block Diagram**



## Measurement Circuit

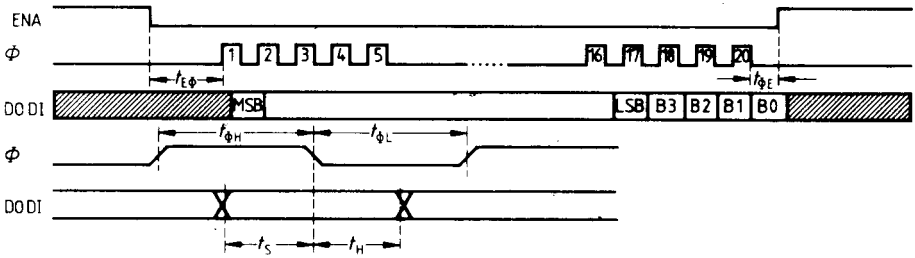


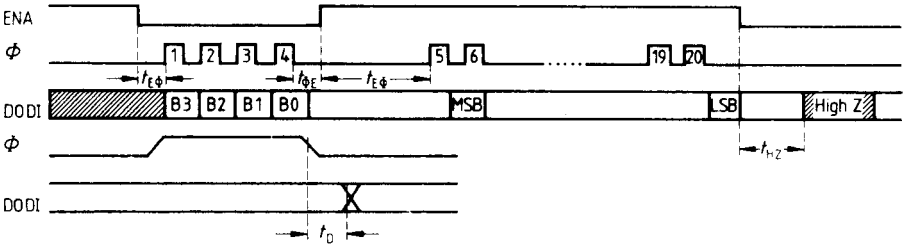

## Application Circuit



## Diagrams

Write

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