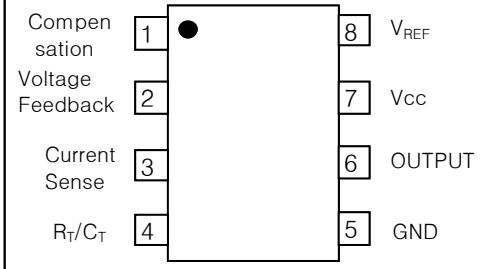
FEATURES

- Automatic feed forward compensation
- Optimized for offline converter
- Double pulse suppression
- Current mode operation to 500 KHz
- High gain totem pole output
- Internally trimmed bandgap reference
- Undervoltage lockout with hysteresis
- Low start up current : < 0.3 mA

8 SOP/ 8 DIP PIN Configulation



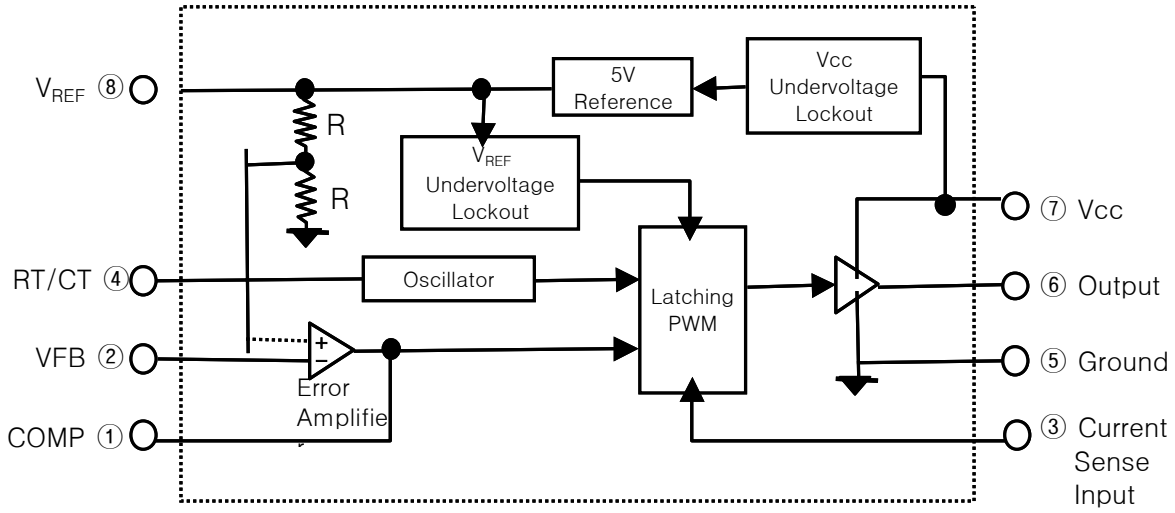
ORDERING INFORMATION

Device	Package
LM3842A/3A/4A/5A D	8 SOP
LM3842A/3A/4A/5A N	8 DIP

DESCRIPTION

The LM3842A is fixed frequency current-mode PWM controller. It is specially designed for Off-Line and DC-to-DC converter applications with minimal external components.
This integrated circuit features a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totempole output ideally suited for driving a power MOSFET.
Protection circuitry includes built in under-voltage lockout and current limiting.

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A= 25℃)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{cc}	30	V
Output Current	I	± 1	A
Analog Inputes Voltage	V_{IN}	-0.3 to 5.5V	V
Error Amp Output Sink Current	I_{SINK}	10	mA
Power Dissipation	P_D	1	W
Storage Temperature Range	Tstg	-65 to 150	℃
Lead Temperature (soldering 5 sec)	T	260	℃

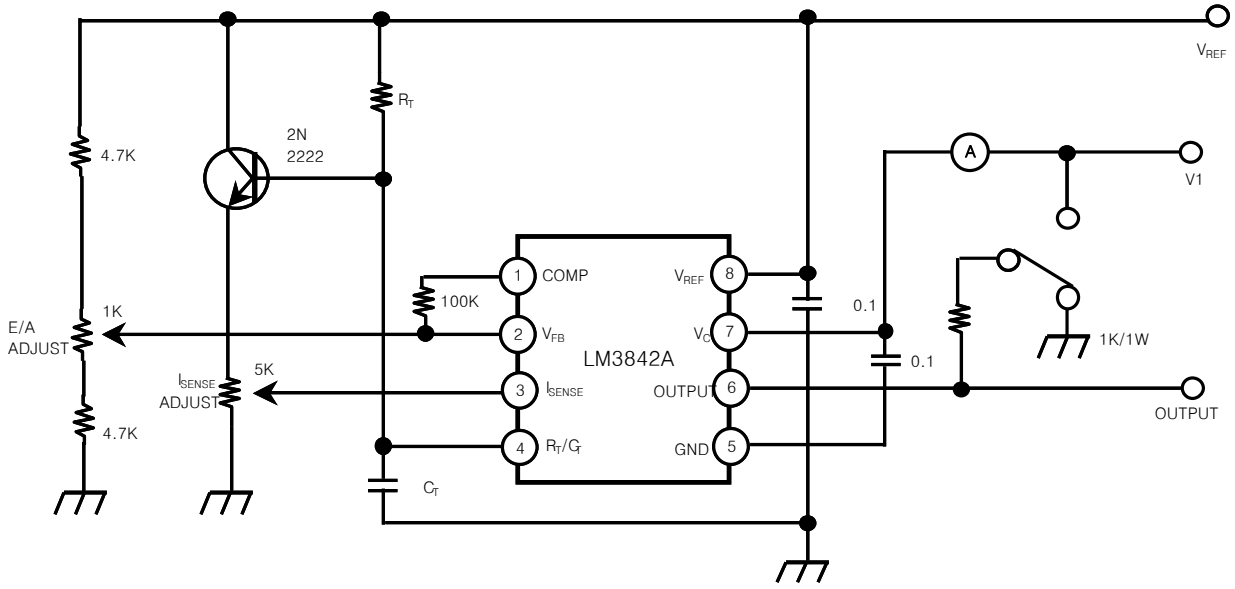
ELECTRICAL CHARACTERISTIC

(Vcc=15V(Note 1), R_T = 10kΩ, C_T=3.3nF 0 ≤ T_A ≤ 70℃ ; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
REFERENCE SECTION						
Reference Output Voltage	V_{REF}	T_j = 25℃, I_O=1 mA	4.90	5.00	5.10	V
Line Regulation	Vo	12V ≤ Vcc ≤ 25V		2	20	mV
Load Regulation	Vo	1mA ≤ Io ≤ 20mA		3	2.5	mV
Output Short Circuit Current	Isc	T_A = 25℃		−85	−180	mA
OSCILLATOR SECTION						
Normal Frequency	F_{OSC}	T_j = 25℃	47	52	57	kHz
Voltage Stability	Sv	12V ≤ Vcc ≤ 25V		0.2	1	%
Amplitude	Vosc			1.6		Vp-p
ERROR AMPLIFIER SECTION						
Input B Current	I_{IB}			−0.1	−2	μA
Feedback Input Voltage	V_{FB}	Vo=2.5V	2.42	2.50	2.58	V
Open Loop Voltage Gain	A_{VOL}	2V≤ Vo ≤ 4V	65	90		dB
Power Supplier Rejection Ratio	$PSRR_{EA}$	12V ≤ Vcc ≤ 25V	60	70		dB
Output Sink Current	I_{SI}	V_{FB}=2.7V, Vo − 1.1V	2	7		mA
Output source Current	I_{SO}	V = 2.3V, Vo=5V	−0.5	−1.0		mA
Output Voltage High	V_{OH}	V_{FB}=2.7V, R_L=15kΩ to GND	5	6		V
Output Voltage Low	V_{OL}	V_{FB}=2.7V, R_L=15kΩ to V_{RGR}		0.8	1.1	V
CURRENT SENSE SECTION						
Input Voltage Gain	Av	(Note 2 & 3)	2.85	3	3.15	V/V
Maximum Input Signal	V_{MAX}	Vo=5V (Note 2)	0.9	1	1.1	V
Power Supply Rejection Ratio	$PSRR_{SC}$	12V ≤ Vcc ≤ 25V		70		dB
Input Bias Current	I_{IB}			−2	−1.0	μA
OUTPUT SECTION						
Output Voltage Low	V_{OL}	I_{sink} = 20mA		0.1	0.4	V
		I_{sink} = 20mA		1.5	2.2	V
Output Voltage High	V_{OH}	I_{source} = 20mA	13	13.5		V
		I_{source} = 20mA	12	13.0		V
Rise Time	T	T_j = 25℃, C_L=1nF		45	150	nS
Fail Time	T	T_j = 25℃, C_L=1nF		35	150	nS
UNDERVOLTAGE LOCKOUT SECTION						
Start-up Threshold	V_{th}	3842A / 3844A	14.5	16	17.5	V
		3843A / 3845A	7.8	8.4	9	V
Minimum Operating Voltage (After Turn-On)	$V_{CC(MIN)}$	3842A / 3844A	8.5	10	11.5	V
		3843A / 3845A	7.0	7.6	8.2	V
TOTAL STANDBY CURRENT						
Start-up Current	I_{st}	Vcc=14V		0.17	0.3	mA
Operating Supply Current	I_{CC}			13	17	mA
Zener Voltage	V	Icc = 25mA	30	38		V

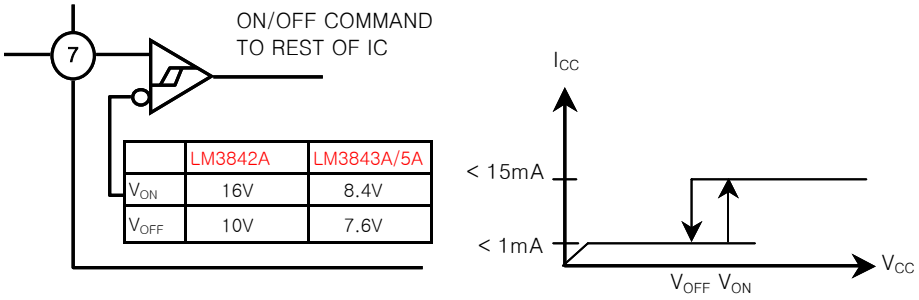
Note: 1. Adjust Vcc above the start threshould before setting at 15V.
2. Parameter measured at trip point of latch with V_{FB} − 0.
3. Comparator Gain defined as: $A_V = \frac{\Delta V \text{ Output Compensation(pin FB)}}{\Delta V \text{ Current Sanseinput(pin CS)}}$;

Fig.1 Open Loop Test Circuit



High peak currents associated with capacitive loads necessitate careful grounding techniques Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

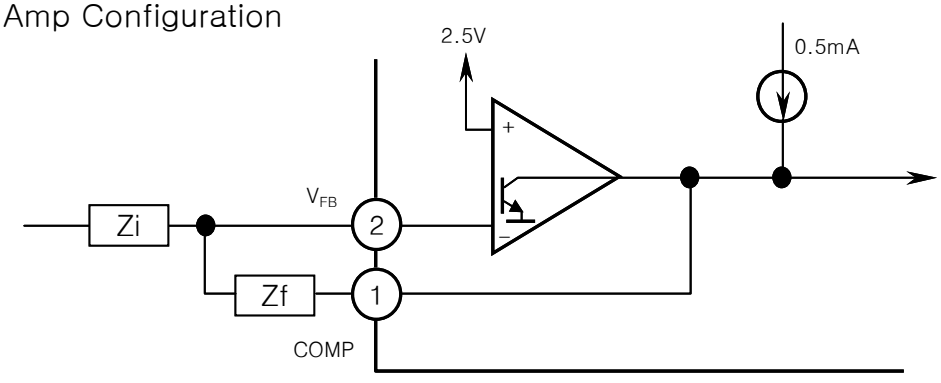
Fig.2 Under Voltage Lockout



	LM3842A	LM3843A/5A
V_{ON}	16V	8.4V
V_{OFF}	10V	7.6V

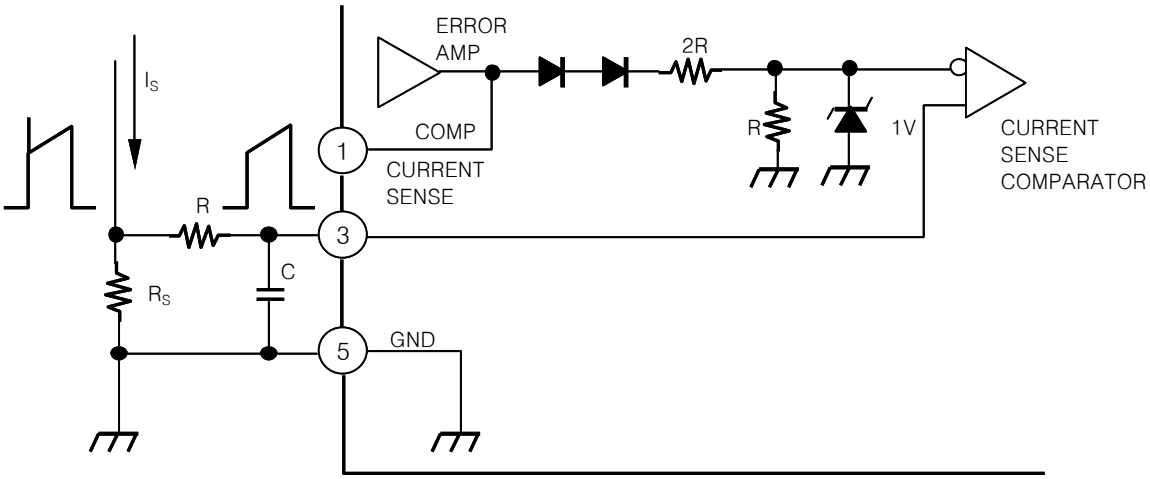
During Under-Voltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

Fig.3 Error Amp Configuration



Error amp can source or sink up to 0.5mA

Fig.4 Current Sense Circuit

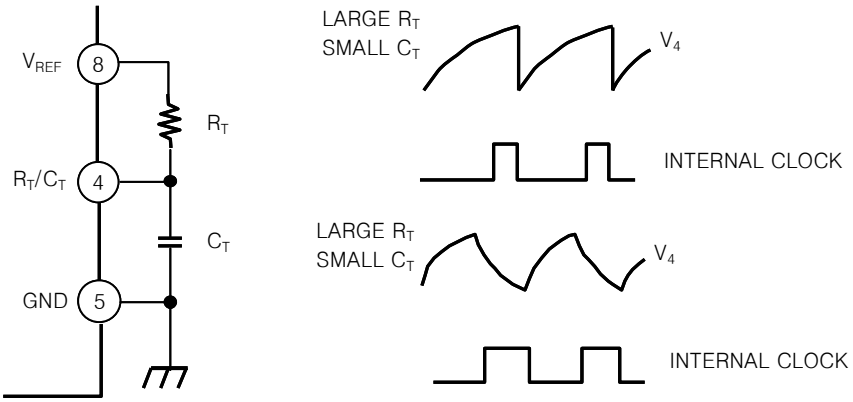


Peak current (I_S) is determined by the formula:

$$I_{S(MAX)} \approx \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Fig.5 Oscillator Waveforms and Maximum Duty Cycle



Oscillator timing capacitor, C_T, is charged by V_{REF} through R_T, and discharged by an internal current source. During the discharge time, the internal clock signal blanks the output to the low state. Selection of R_T and C_T therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulas:

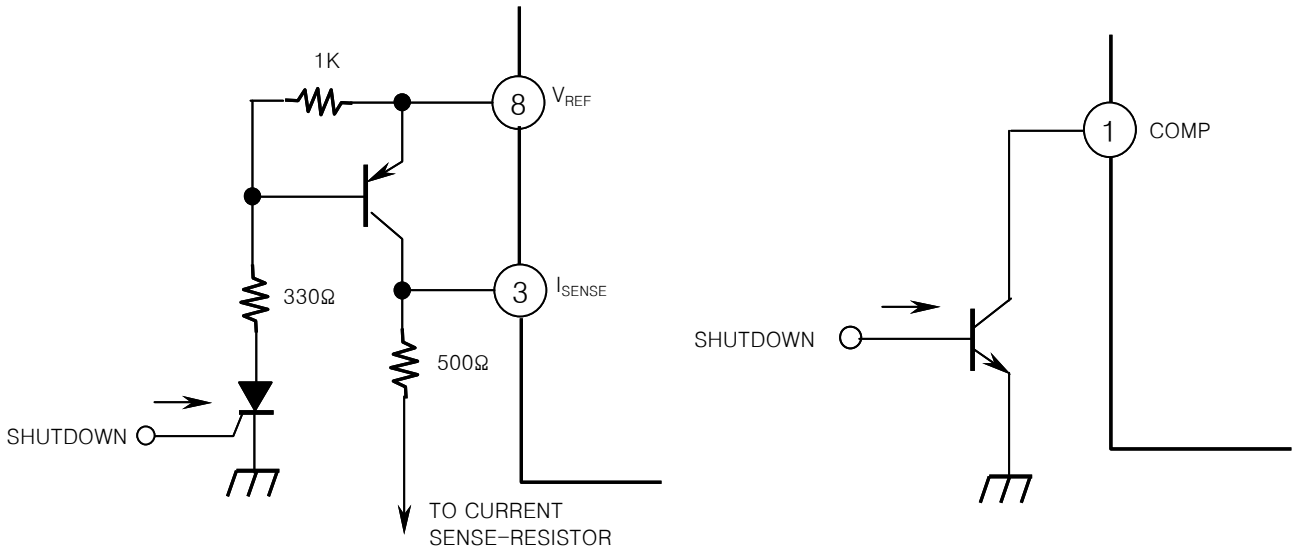
$t_c \approx 0.55\ R_T\ C_T$

$$t_d \sim R_T\ C_T\ \ln\left(\frac{0.0063\ R_T - 2.7}{0.0063\ R_T - 4}\right)$$

Frequency, then, is: $f = (t_c + t_d)^{-1}$

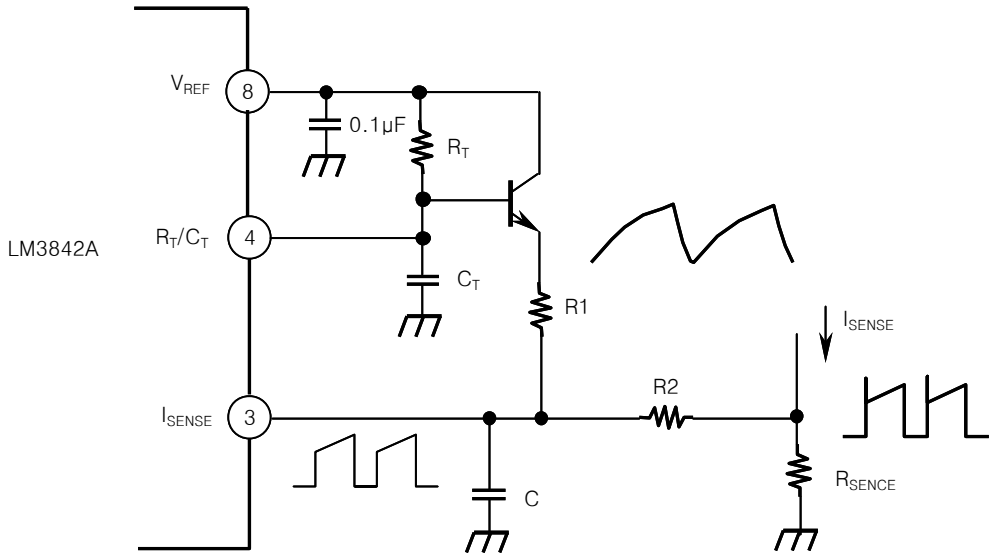
For $R_T > 5K\Omega$, $f \approx \frac{1.8}{R_T\ C_T}$

Fig.6 Shutdown Techniques



Shutdown of the LM3842A can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shoutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

Fig.7 Slope Compensation



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

Fig.1 Output Dead Time

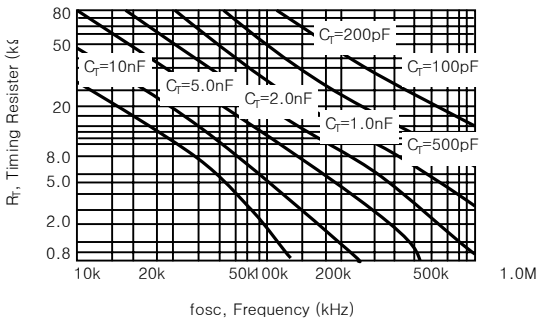


Fig.2 Timing Resistor vs Frequency

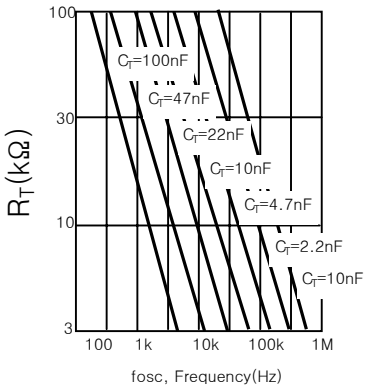


Fig.3 Output Saturation Characteristics

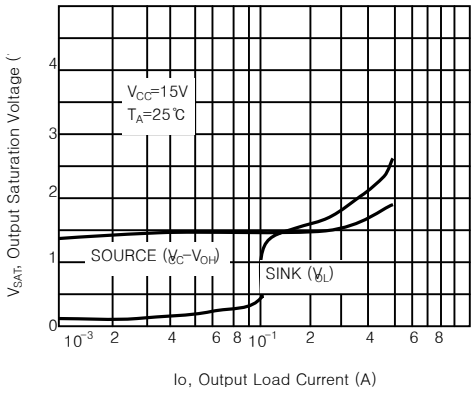
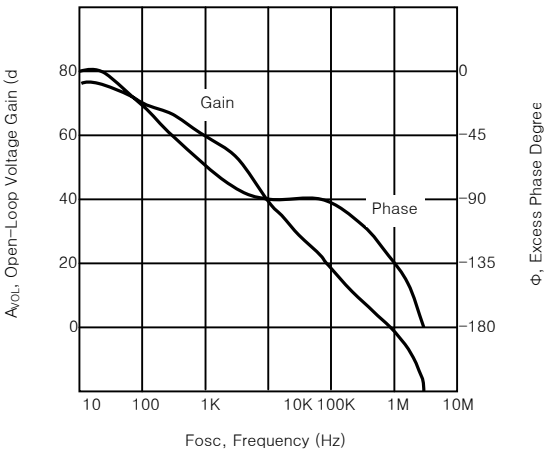


Fig.4 Error Amplifier Open Loop Gain and Phase Frequency



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	Voltage Feedback	This is the inverting input of the Error Amplitier. It is normally connected to the switching power supply output through a resister divider.
3	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to VR_{EF} and capacitor C_T to ground. Operation to 500kHz is possible.
5	GND	This pin is the combined control circuitry and power ground.
6	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0A are sourced and sunk by this pin.
7	Vcc	This pin is the positive supply of the control IC.
8	V_{REF}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.