Ordering number : ENN*8075

Preliminary

SANYO Semiconductors
DATA SHEET

LC822152 — CMOS IC CCD-LCD Interface ASIC

Overview

LC822152 is a chip which compresses and expands the image inputted from the CCD/CMOS by JPEG format, interfacing the LCD controller equipped with built-in CCD/CMOS sensor module and display memory for DSC-PHONEs. Since the I^2C master device circuit is embedded in the chip and the signal required for the CCD/CMOS module is supplied from this chip, regarding the CPU, it is not necessary to concern the interface with the CCD/CMOS module. In addition, the zooming function using the H/V scaling circuit allows an effective LCD display. The functions comprises the following blocks :

- Image-processing unit where the 8-bit video image data in YUV422 (211) format from CCD/CMOS is scaling processed, performed scaling down and cropping (to cut the four sides) to any size, converted to the RGB565 format and then sent to the LCD controller.
- JPEG processing unit where the YUV422 (211) image data (VGA size) input from CCD/CMOS or the image data which has been processed by scaling or cropping is compressed to the JPEG format, and the sign data is output. Or JPEG processing unit where the sign data input from the host is processed with JPEG decryption and sent to the image processing unit.
- Thumbnail image processing unit where the image data output to the LCD controller is thinned out and reduced to a maximum 40×40 sized image.
- Host control unit where CPU interface, register control, LCD bus switching, JPEG code data transfer, and thumbnail image data transfer are performed.
- I^2C interface unit for the CCD/CMOS module access.
- LCD controller interface processing unit allows the RGB666 output (260,000 colors) supporting the 18-bit parallel and various split transfer.

Features

• CCD/CMOS Interface	YUV422 (8-bit) format. Maximum VGA size : 640×480. MCKI : System clock supplied to the CCD/CMOS module. PCLK : Dot clock output from the CCD/CMOS module.
• CPU Interface	80-system 16-bit bus (D15-D0, WR, RD, A2-0, CS) Accessible to the JPEG controller, control register including I^2C master, JPEG code buffer, thumbnail image buffer, OSD display buffer, and LCD command buffer.
• LCD Interface	Connects the chip to the LCD controller system bus with the 80-system 16-bit bus interface. It is accessible by switching automatically the two masters, host CPU or LSI image-processing unit. Output image from LSI is RGB565 (16-bit) or RGB666 (18-bit, 9-bit×2, etc.). Maximum display size is 320×240 (without OSD) or 320×200 (with OSD). Camera image display to the sub LCD is possible.

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- I^2C Interface — Built-in I^2C master for CCD/CMOS module control. Without paying attention to the I^2C from the CPU, it is accessible to the CCD/CMOS module as well as the normal register (write/read).
- Scaling function — CCD output is a VGA size (640×480). The output is reduced/cropped to meet the LCD display range with a scaler. Low-pass filter and enhancer are equipped.
- JPEG codec — The YUV422/YUV420 image data is compressed into JPEG code, and the JPEG code data is expanded to the YUV422/YUV420 image data.
- Thumbnail — It performs thinning out, scaling down and cropping the LCD output images to an image size of maximum 40×40.
- Clock system — LSI includes PLL and it multiplies the clock input from outside to make a main clock. It divides this multiplied frequency to output to CCD/CMOS module as the clock.
- Package — FBGA96K
- Process — 0.18μm E/A
- Power source voltage — Internal 1.8V±0.18V, I/O 3.0V±0.3V

Specifications

Absolute Maximum Ratings at V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Source Voltage	$V_{DD}30$ max		-0.3 to 3.3	V
	$V_{DD}18$ max		-0.3 to 1.98	V
Input/Output Voltage	V_I, V_O		-0.3 to *$V_{DD}3$ max *+0.3 (max 3.3V)	V
Input/Output Current	I_I, I_O	*1	±20	mA
Allowable Power Dissipation	Pd max	Ta≤70°C *2	650	mW
Operating Temperature	Topr		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

*1 : Absolute maximum rating per input/output reference cell

*2 : This value is assured when the conditions for substrate mounting are as follows.
In other conditions, the assured value will be changed accordingly. (Conditions for substrate mounting)
Substrate size : FR4 (50mm×108mm×1.27mm)
Cu trace rate : 250%

Allowable Operating Range at Ta = -30 to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power Source Voltage (I/O unit)	$V_{DD}30$		2.7	3.0	3.3	V
Input Voltage Range (I/O unit)	$V_{IN}30$		0		$V_{DD}30$	V
Source Voltage (Internal logic unit)	$V_{DD}18$		1.62	1.8	1.98	V
Input Voltage Range (Internal logic unit)	$V_{IN}18$		0		$V_{DD}18$	V
Power Source Voltage (Analog part)	AV_{DD}		1.62	1.8	1.98	V
Input Voltage Range (Analog part)	AV_{IN}		0		AV_{DD}	V

Input/Output Pin Capacitance at Ta = 25°C, $V_{DD}18 = V_{DD}33 = V_{IN}18 = V_{IN}30$ = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input Pin	C_{IN}	f = 1MHz			10	pF
Output Pin	C_{OUT}	f = 1MHz			10	pF
Input/Output Pin	$C_{I/O}$	f = 1MHz			10	pF

Electric Characteristics

D.C. Characteristics : Input/Output Levels at Ta = -30 to +70°C, $V_{DD}30$ = 2.7 to 3.3V, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit	Applicable Pins
			min	typ	max		
Input High Level Voltage	V_{IH}	CMOS support	$0.7V_{DD}30$			V	2
Input Low Level Voltage	V_{IL}				$0.2V_{DD}30$	V	
Input High Level Voltage	V_{IH}	CMOS support Schmidt	$0.75V_{DD}30$			V	1
Input Low Level Voltage	V_{IL}				$0.15V_{DD}30$	V	
Input High Level Current	I_{IH}	$V_I = V_{DD}30$	-10		10	µA	7
		$V_I = V_{DD}30$, with pull-down resistor	-10		100	µA	6
Input Low Level Current	I_{IL}	$V_I = V_{SS}$	-10		10	µA	6, 7
Output High Level Voltage	V_{OH}	I_{OH} = -2mA	$V_{DD}30$-0.8			V	3
		I_{OH} = -4mA	$V_{DD}30$-0.8			V	8
		I_{OH} = -8mA	$V_{DD}30$-0.8			V	4
Output Low Level Voltage	V_{OL}	I_{OL} = 1.8mA			0.4	V	3
		I_{OL} = 3.6mA			0.4	V	8
		I_{OL} = 7.2mA			0.4	V	4
Output Leak Current	I_{OZ}	At HiZ Output	-10		10	µA	5
Pull-down Resistor	RDN		50	100	200	kΩ	6
Non-operating Current Dissipation	I_{DD}	Output release V_I=V_{SS} or $V_{DD}30$			300	µA	

1 : TEST[3:0], XRST, CLKSEL, STBY, SCANEN, SCANMOD
2 : Input pin and dual-directional pin except 1.
3 : Output pin except MCKI and dual-directional pin except 8.
4 : MCKI
5 : Dual-directional pin
6 : PCLK, HREF, VREF, CD[7:0]
7 : Input pin and dual-directional pin except 6.
8 : D[15:0]

Input Clock

When CLKSEL input is “H”.

Clock Pin	Maximum Input Frequency (MHz)	Duty
CKI	60	50±10%

Note : The internal operation clock would be 30MHz at a maximum. For 60MHz input, the clock divided by at least 2 must be used as the internal operation clock.

When CLKSEL input is “0” (PLL is used).

Clock Pin	Maximum Input Frequency (MHz)	Duty
CKI	100	50±10%

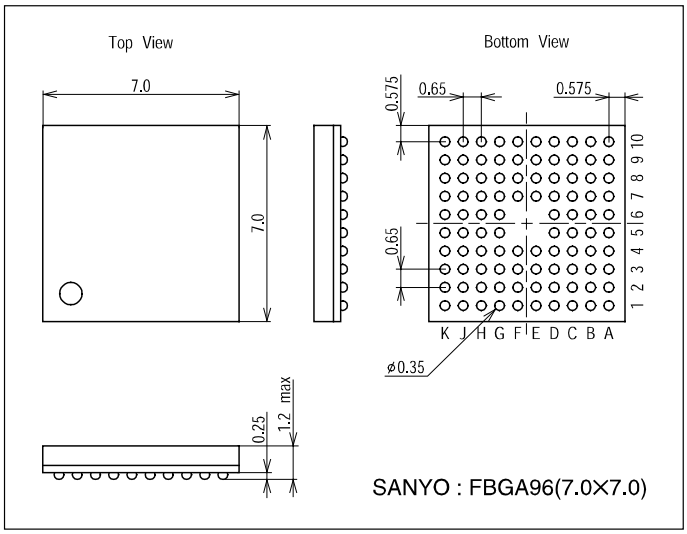
In addition, setup here must satisfy the following PLL input/output specifications.

Parameter	Symbol	min	typ	max	Unit
Maximum VCO Oscillation Frequency	f max		180		MHz
Minimum VCO Oscillation Frequency	f min		60		MHz
Phase Contrast Frequency	f ref			30.0	MHz

Package Dimensions

unit : mm

3306



Pin Description

No.	Pin Number	Pin Names	I/O	Pin Description	Initial Value
1	B1	V_{SS}		GND	
2	B2	AV_{DD}		Analog system V_{DD} 1.8V power source	
3	C1	VCNT	O	PLL VCNT pin	
4	D4	AV_{SS}		Analgo V_{SS}	
5	C2	TEST3	I	Test input 3	L
6	D1	$V_{DD}1.8$		1.8V power source	
7	D3	V_{SS}		GND	
8	D2	$V_{DD}3$		3V power source	
9	E1	CKI	I	Clock input	
10	E4	CLKSEL	I	Clock dividing select	
11	E3	STBY	I	Stand by	
12	E2	TEST0	I	Test input 0	L
13	F2	XRST	I	Reset	
14	F3	V_{SS}		GND	
15	F4	$V_{DD}3$		3V power source	
16	F1	CAMPWR	O	CCD power down	O
17	G2	REGRES	O	CCD reset	O
18	G3	MCKI	O	CCD master clock	O
19	G1	TEST1	I	Test input 1	L
20	H2	TEST2	I	Test input 2	L
21	H3	SDA	B	I^2C data	O
22	H1	SCL	O	I^2C clock	O
23	J1	$V_{DD}1.8$		1.8V power source	
24	K1	V_{SS}		GND	
25	K2	$V_{DD}3$		3V power source	
26	J2	PCLK	I	CCD pixel clock	PD
27	K3	HREF	I	Horizontal synchronous signal input	PD
28	G4	VREF	I	Vertical synchronous signal input	PD
29	J3	CD7	I	CCD data input	PD
30	K4	CD6	I	CCD data input	PD

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No.	Pin Number	Pin Names	I/O	Pin Description	Initial Value
31	H4	CD5	I	CCD data input	PD
32	J4	CD4	I	CCD data input	PD
33	K5	CD3	I	CCD data input	PD
34	G5	CD2	I	CCD data input	PD
35	H5	CD1	I	CCD data input	PD
36	J5	CD0	I	CCD data input	PD
37	J6	$V_{DD}1.8$		1.8V power source	
38	H6	V_{SS}		GND	
39	G6	$V_{DD}3$		3V power source	
40	K6	EX1	B	Expanded LCD data bus	
41	J7	EX0	B	Expanded LCD data bus	
42	H7	LCS2	O	Chip select output for sub LCD	1
43	K7	LA	O	LCD address output	-
44	J8	LCS	O	LCD chip select output	1
45	H8	LWR	O	LCD write signal output	1
46	K8	LRD	O	LCD read signal output	1
47	K9	$V_{DD}1.8$		1.8V power source	
48	K10	V_{SS}		GND	
49	J10	$V_{DD}3$		3V power source	
50	J9	LD15	B	LCD data bus	-
51	H10	LD14	B	LCD data bus	-
52	G7	LD13	B	LCD data bus	-
53	H9	LD12	B	LCD data bus	-
54	G10	LD11	B	LCD data bus	-
55	G8	LD10	B	LCD data bus	-
56	G9	LD9	B	LCD data bus	-
57	F10	LD8	B	LCD data bus	-
58	F7	LD7	B	LCD data bus	-
59	F8	LD6	B	LCD data bus	-
60	F9	LD5	B	LCD data bus	-
61	E9	$V_{DD}3$		3V power source	
62	E8	V_{SS}		GND	
63	E7	$V_{DD}1.8$		1.8V power source	
64	E10	LD4	B	LCD data bus	-
65	D9	LD3	B	LCD data bus	-
66	D8	LD2	B	LCD data bus	-
67	D10	LD1	B	LCD data bus	-
68	C9	LD0	B	LCD data bus	-
69	C8	CS	I	Chip select input	H
70	C10	CS2	I	Chip select input for sub LCD	H
71	B10	A1	I	Address input	-
72	A10	V_{SS}		GND	
73	A9	$V_{DD}3$		3V power source	
74	B9	A0	I	Address input	-
75	A8	WR	I	Write signal input	H
76	D7	RD	I	Read signal input	H
77	B8	INT	O	Interrupt output	1
78	A7	D15	B	Host data bus	-
79	C7	D14	B	Host data bus	-
80	B7	D13	B	Host data bus	-
81	A6	D12	B	Host data bus	-
82	D6	D11	B	Host data bus	-
83	C6	D10	B	Host data bus	-

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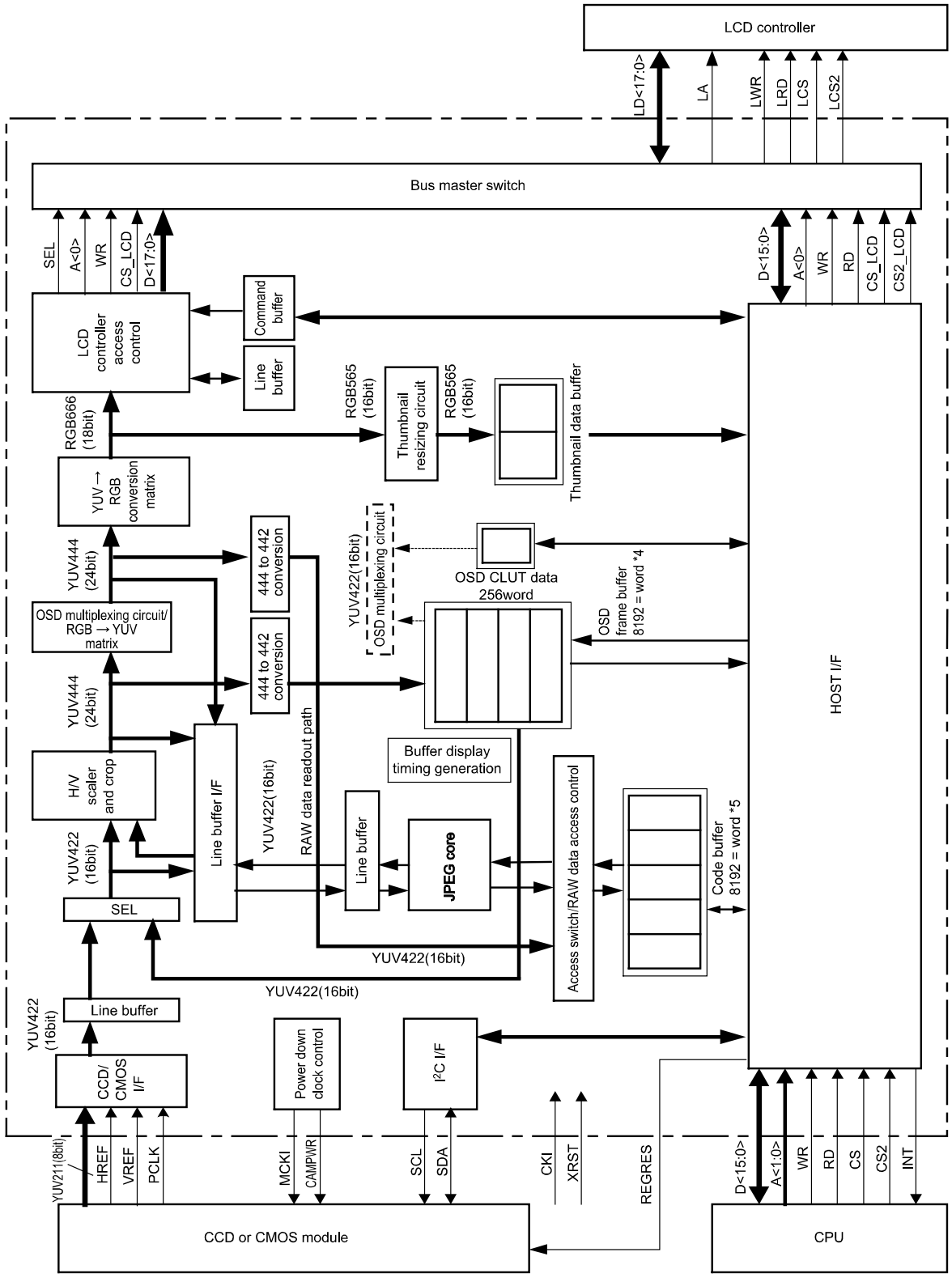
No.	Pin Number	Pin Names	I/O	Pin Description	Initial Value
84	B6	D9	B	Host data bus	-
85	B5	$V_{DD}1.8$		1.8V power source	
86	C5	V_{SS}		GND	
87	D5	D8	B	Host data bus	-
88	A5	D7	B	Host data bus	-
89	B4	D6	B	Host data bus	-
90	C4	D5	B	Host data bus	-
91	A4	D4	B	Host data bus	-
92	B3	D3	B	Host data bus	-
93	C3	D2	B	Host data bus	-
94	A3	D1	B	Host data bus	-
95	A2	D0	B	Host data bus	-
96	A1	$V_{DD}3$		3V power source	

Block Diagram



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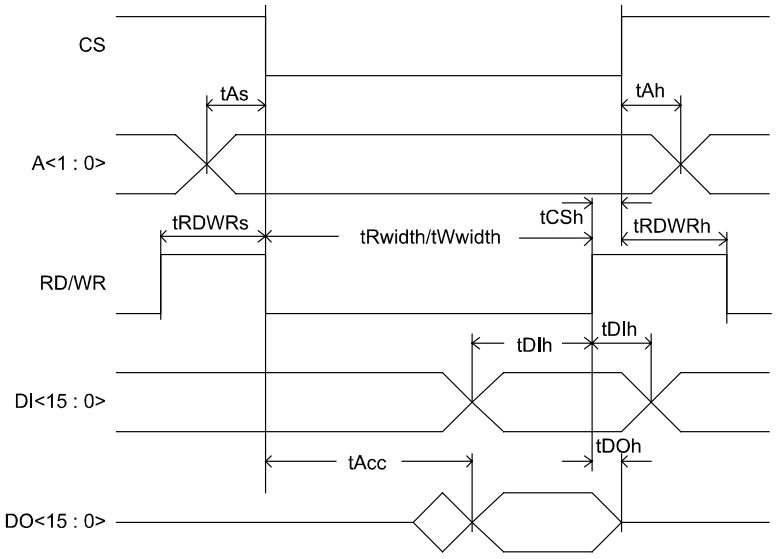
AC Characteristics

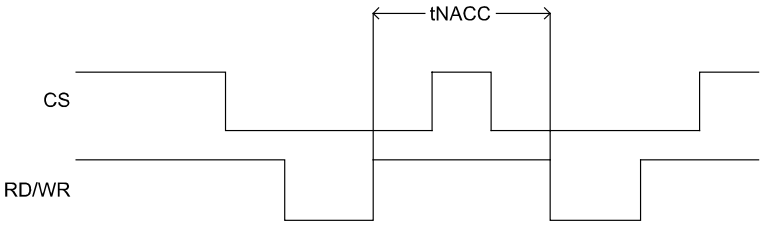
Host Interface Timing



Symbol	Contents	min	max	Unit
tAs	ADRESS setup time to CS↓	5*1		ns
tAh	ADRESS hold time from CS↑	5*2		ns
tCSh	CS hold time from RD/WR↑	0		ns
tRDWRs	RD/WR(CS↓)setup time from RD/WR↑	5*1		ns
tRDWRh	RD/WR(CS↑)hold time from RD/WR↓	5		ns
tRwidth	RD pulse width	T+5		ns
tWwidth	WR pulse width	20		ns
tDIs	Input DATA setup time to WR↑	20		ns
tDIh	Input DATA hold time from WR↑	0		ns
tAcc	Output DATA access time from RD↓		50	ns
tDOh	Output DATA hold time from RD↑	2		ns

*1 : Operation at times under 5 ns is also possible by delaying the internal CS with the CS delay setting (CSCHOP register). However, since incorrect operation may occur if an access is performed before the setting is changed, the application must change the setting immediately after power is first applied.

*2 : Operation with an internal command access of 0ns minimum is possible. However, if this signal is input at 0ns when the LCD controller is accessed directly, it is possible that small pulses, such as LCS and LCS2, may be generated.



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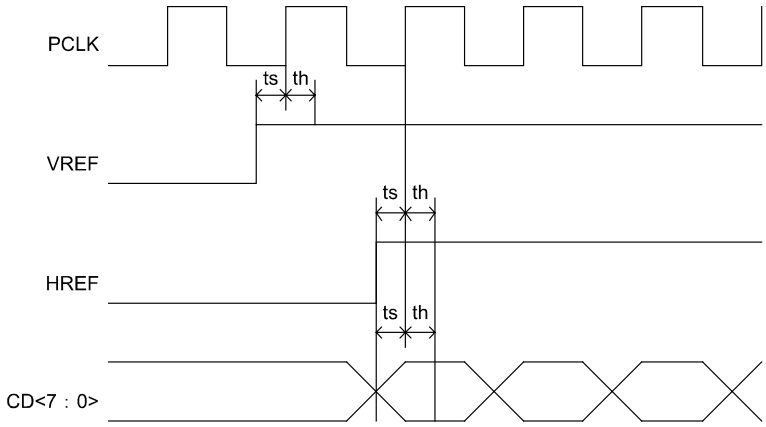
Symbol	Contents		min	Unit
tNACC	RD/WR No Access time	JPEG Q-Table Write	3T	ns
		JPEG Q-Table Read	7T	ns
		Code/Thumbnail buffer Read	4T	ns
		Other access	2T	ns

Note1 : T is a cycle of ASIC internal clock. (1, 2, 4, or 8 times the cycle of CKI input clock)

Note2 : Write access of JPEG Huffman table is subject to the data where access prohibited period is written.

CCD Interface Timing



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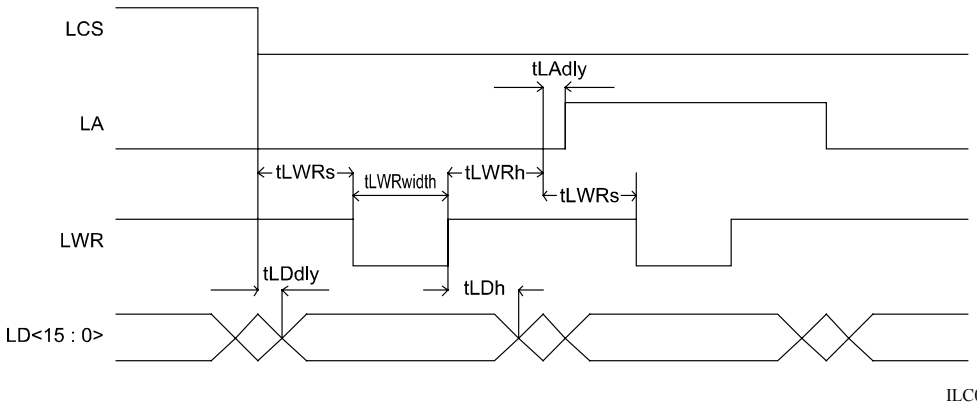
Symbol	Contents	min	typ	max	Unit
ts	Setup time to PCLK	10			ns
th	Hold time from PCLK	5			ns

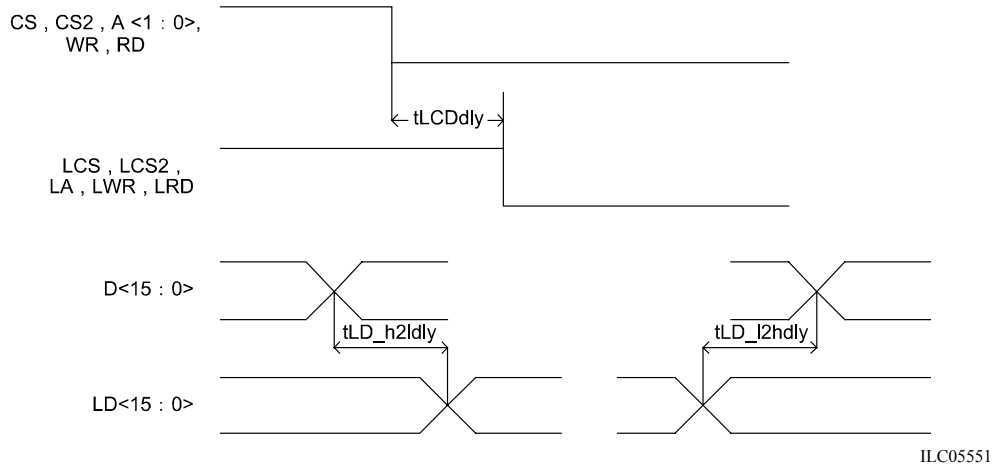
LCD Interface Timing



Symbol	Contents	min	max	Unit
tLWRs	LCD access setup time to LWR↓	T-5		ns
tLWRwidth	LWR pulse width	T*n-5		ns
tLWRh	LCD access hold time from LWR↑	T*m-5		ns
tLAdly	LA delay from cycle start		5	
tLDdly	LD delay from cycle start		10	
tLDh	LD hold time from LWR↑	0 (When m = 0 setup)	tLWRh+5	ns

Note1 : T is a cycle of ASIC internal clock. (1, 2, 4, or 8 times the cycle of CKI input clock)
Note2 : n is an ASIC register setting value. Minimum value is 1 (zero).
Note3 : m is an ASIC register setting value. Minimum value is 0 (zero).

Host-LCD Through Timing



Symbol	Contents	min	max	Unit
tLCDdly	HOST to LCD control signal delay		30	ns
tLD_h2ldly	HOST to LCD data delay		35	ns
tLD_l2hdly	LCD to HOST data delay		30	ns

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