Agilent HMPP-386x Series MiniPak Surface Mount RF PIN Diodes

Data Sheet

Features

- **Surface mount MiniPak package**
  - low height, 0.7 mm (0.028") max.
  - small footprint, 1.75 mm^2 (0.0028 $inch^2$)
- **Better thermal conductivity for higher power dissipation**
- **Single and dual versions**
- **Matched diodes for consistent performance**
- **Low capacitance at zero volts**
- **Low resistance**
- **Low FIT (Failure in Time) rate***
- **Six-sigma quality level**

* For more information, see the Surface Mount Schottky Reliability Data Sheet.

Description/Applications

These ultra-miniature products represent the blending of Agilent Technologies' proven semiconductor and the latest in leadless packaging technology.

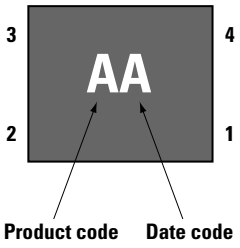
The HMPP-386x series of general purpose PIN diodes are designed for two classes of applications. The first is attenuators where current consumption is the most important design consideration. The second application for this series of diodes is in switches where low capacitance with no reverse bias is the driving issue for the designer.

The low dielectric relaxation frequency of the HMPP-386x insures that low capacitance can be reached at zero volts reverse bias at frequencies above 1 GHz, making this PIN diode ideal for hand held applications.

Low junction capacitance of the PIN diode chip, combined with ultra low package parasitics, mean that these products may be used at frequencies which are higher than the upper limit for conventional PIN diodes.

Note that Agilent's manufacturing techniques assure that dice packaged in pairs are taken from adjacent sites on the wafer, assuring the highest degree of match.

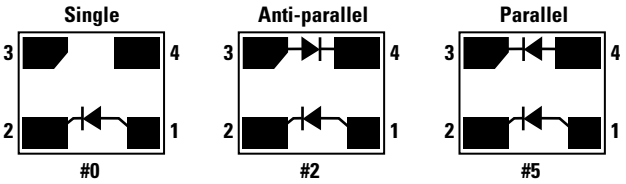
Pin Connections and Package Marking



Notes:

1. Package marking provides orientation and identification.
2. See "Electrical Specifications" for appropriate package marking.

Package Lead Code Identification (Top View)



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HMPP-386x Series Absolute Maximum Ratings[1], T_C = 25°C

Symbol	Parameter	Units	Value
I_f	Forward Current (1 μs pulse)	Amp	1
P_{IV}	Peak Inverse Voltage	V	100
T_j	Junction Temperature	°C	150
T_{stg}	Storage Temperature	°C	-65 to +150
θ_{jc}	Thermal Resistance[2]	°C/W	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

ESD WARNING:
Handling Precautions Should Be Taken To Avoid Static Discharge.

Electrical Specifications, T_C = +25°C, each diode

Part Number HMPP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage (V)	Typical Series Resistance (Ω)
3860	H	0	Single	50	3.0/1.5*
3862	F	2	Anti-parallel		
3865	E	5	Parallel		
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	I_F = 10 mA f = 100 MHz *I_F = 100 mA

Typical Parameters, T_C = +25°C

Part Number HMPP-	Total Resistance R_T (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance C_T (pF)
3860 3862 3865	22	500	80	0.20
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 50 mA T_R = 250 mA	V_R = 10 V I_F = 20 mA 90% Recovery	V_R = 50 V f = 1 MHz

HMPP-386x Series Typical Performance, T_c = 25°C, each diode

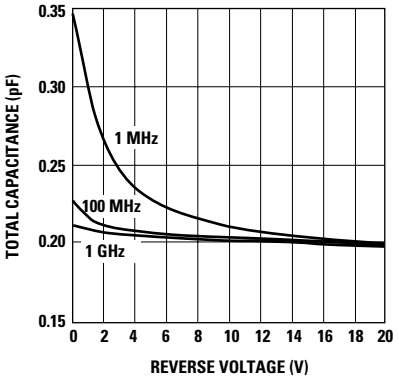


Figure 1. RF Capacitance vs. Reverse Bias.

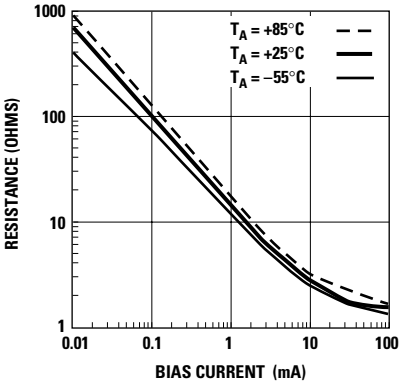


Figure 2. Typical RF Resistance vs. Forward Bias Current.

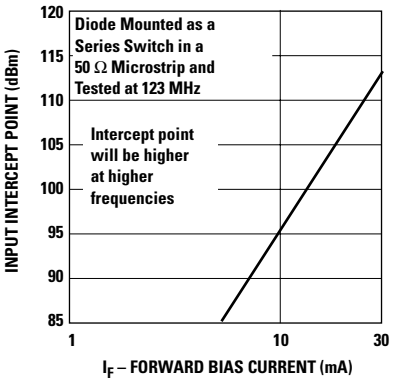


Figure 3. 2nd Harmonic Input Intercept Point vs. Forward Bias Current for Switch Diodes.

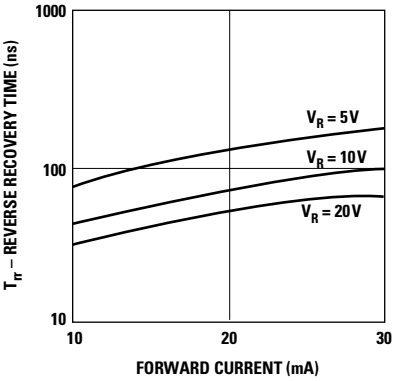


Figure 4. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages.

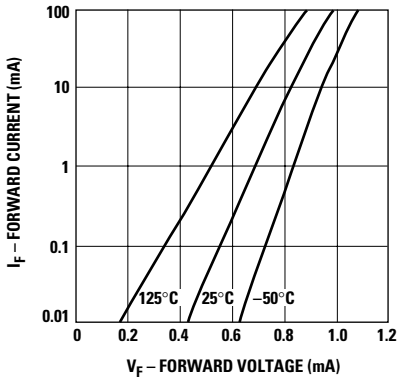


Figure 5. Forward Current vs. Forward Voltage.

Typical Applications

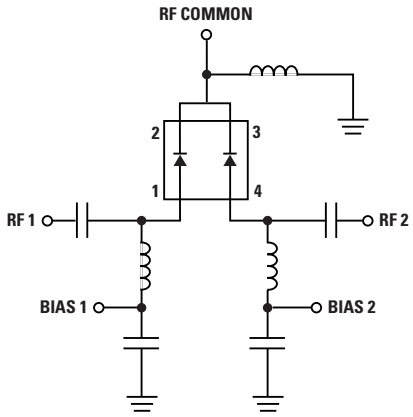


Figure 6. Simple SPDT Switch Using Only Positive Bias.

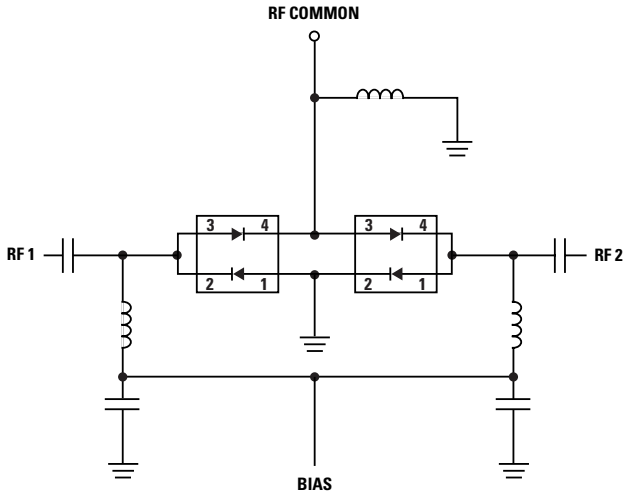


Figure 7. High Isolation SPDT Switch Using Dual Bias.

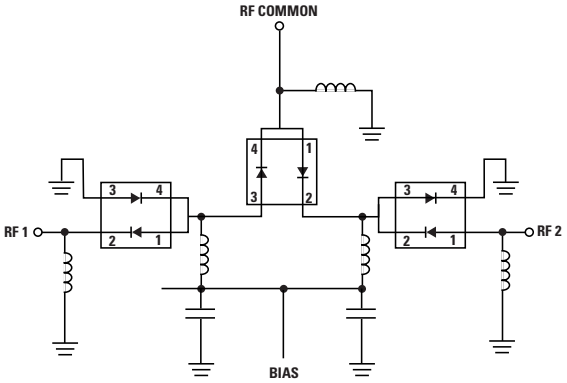


Figure 8. Very High Isolation SPDT Switch, Dual Bias.

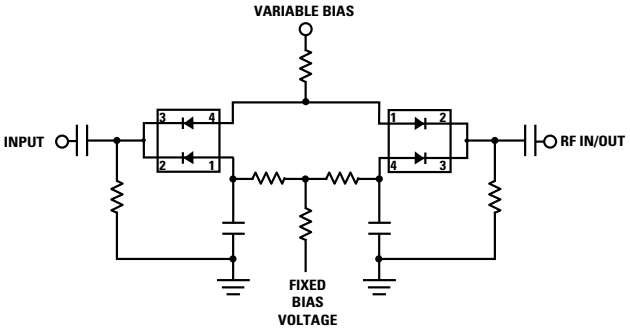


Figure 9. Four Diode π Attenuator. See AN1048 for details.

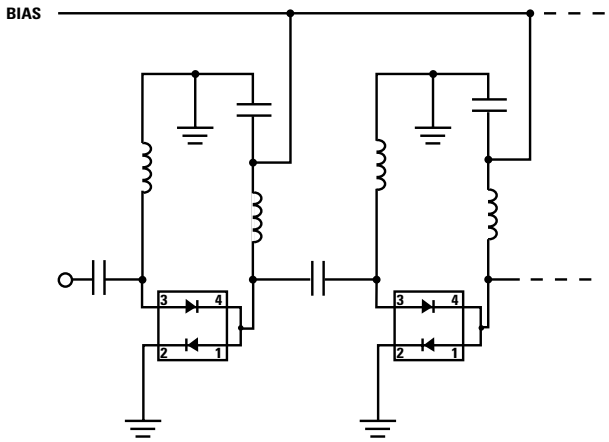


Figure 10. High Isolation SPST Switch (Repeat Cells as Required).

Diode Lifetime and Resistance

The resistance of a PIN diode is controlled by the conductivity (or resistivity) of the I layer. This conductivity is controlled by the density of the cloud of carriers (charges) in the I layer (which is, in turn, controlled by the DC bias). Minority carrier lifetime, indicated by the Greek symbol τ, is a measure of the time it takes for the charge stored in the I layer to decay, when forward bias is replaced with reverse bias, to some predetermined value. This lifetime can be short (35 to 200 nsec. for epitaxial diodes) or it can be relatively long (400 to 3000 nsec. for bulk diodes). Lifetime has a strong influence over a number of PIN diode parameters, among which are distortion and basic diode behavior.

To study the effect of lifetime on diode behavior, we first define a cutoff frequency $f_C = 1/\tau$. For short lifetime diodes, this cutoff frequency can be as high as 30 MHz while for our longer lifetime diodes $f_C \cong 400$ KHz. At frequencies which are ten times f_C (or more), a PIN diode does indeed act like a current controlled variable resistor. At frequencies which are one tenth (or less) of f_C, a PIN diode acts like an ordinary PN junction diode. Finally, at $0.1f_C \leq f \leq 10f_C$, the behavior of the diode is very complex. Suffice it to mention that in this frequency range, the diode can exhibit very strong capacitive or inductive reactance—it will not behave at all like a resistor.

The HMPP-386x family features a typical lifetime of 300 to 500 ns, so $10f_C$ for this part is 5 MHz. At any frequency over 5 MHz, the resistance of this diode will follow the curve given in Figure 2. From this curve, it can be seen that the HMPP-386x family produces a lower resistance at a given value of bias current than most attenuator PIN diodes, making it ideal for applications where current consumption is important.

Dielectric Relaxation Frequency and Diode Capacitance

f_{DR} (Dielectric Relaxation Frequency) for a PIN diode is given by the equation

$$f_{DR} = \frac{1}{2\pi\rho\varepsilon}$$

where…
ρ = bulk resistivity of the I-layer
$\varepsilon = \varepsilon_0 \varepsilon_R = 10^{-12}$ F/cm
= bulk susceptance of silicon

In the case of an epitaxial diode with a value for ρ of 10Ω-cm, f_{DR} will be in Ku-Band. For a bulk diode fabricated on very pure material, ρ can be as high as 2000, resulting in a value of f_{DR} of 80 MHz.

The implications of a low f_{DR} are very important in RF attenuator and switch circuits. At operating frequencies below f_{DR}, reverse bias (as much as 50 V) is needed to minimize junction capacitance. At operating frequencies well above f_{DR}, the curve of capacitance vs. reverse bias is flat.

For the HMPP-386x family, f_{DR} is around 500 MHz, resulting in very low capacitance at zero bias for frequencies above 1 GHz. See Figure 1.

Linear Equivalent Circuit

In order to predict the performance of the HMPP-386x as a switch or an attenuator, it is necessary to construct a model which can then be used in one of the several linear analysis programs presently on the market. Such a model is given in Figure 11, where $R_S + R_j$ is given in Figure 2 and C_j is provided in Figure 1. Careful examination of Figure 11 will reveal the fact that the package parasitics (inductance and capacitance) are much lower for the MiniPak than they are for leaded plastic packages such as the SOT-23, SOT-323 or others. This will permit the HMPP-386x family to be used at higher frequencies than its conventional leaded counterparts.

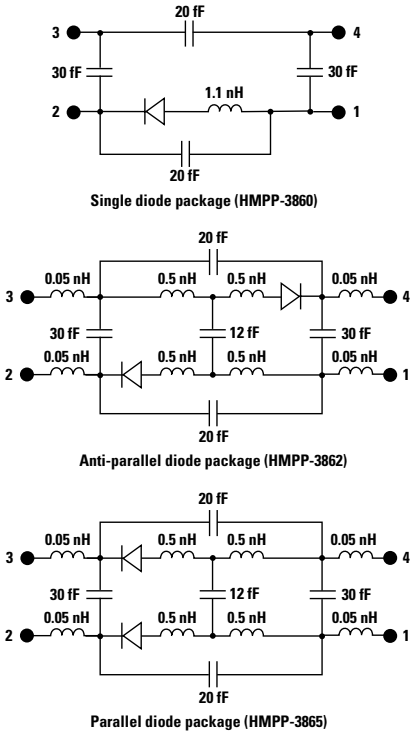
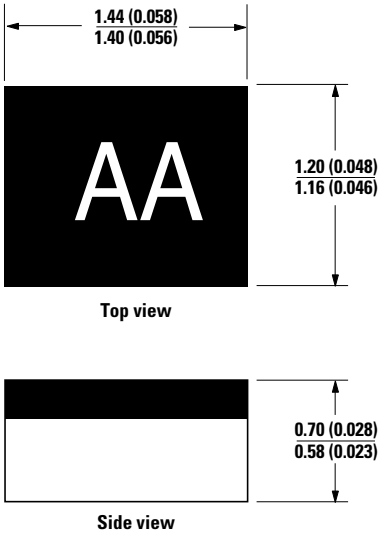
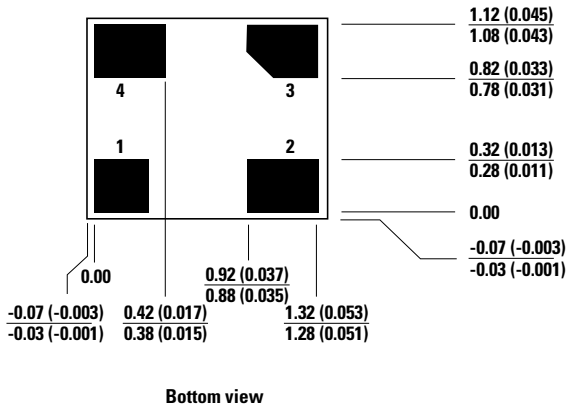


Figure 11. Linear Equivalent Circuit of the MiniPak PIN Diode.

MiniPak Outline Drawing





Assembly Information

The MiniPak diode is mounted to the PCB or microstrip board using the pad pattern shown in Figure 12.

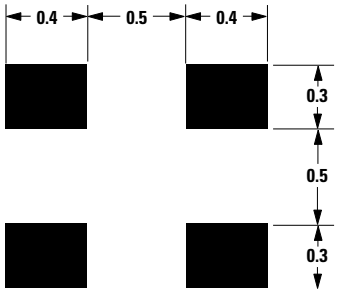


Figure 12. PCB Pad Layout, MiniPak (dimensions in mm).

This mounting pad pattern is satisfactory for most applications. However, there are applications where a high degree of isolation is required between one diode and the other is required. For such applications, the mounting pad pattern of Figure 13 is recommended.

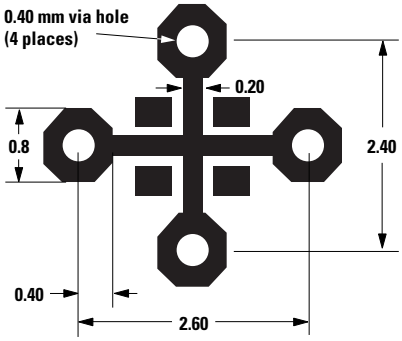


Figure 13. PCB Pad Layout, High Isolation MiniPak (dimensions in mm).

This pattern uses four via holes, connecting the crossed ground strip pattern to the ground plane of the board.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the MiniPak package, will reach solder reflow temperatures faster than those with a greater mass.

Agilent's diodes have been qualified to the time-temperature profile shown in Figure 14. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 255°C.

These parameters are typical for a surface mount assembly process for Agilent diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

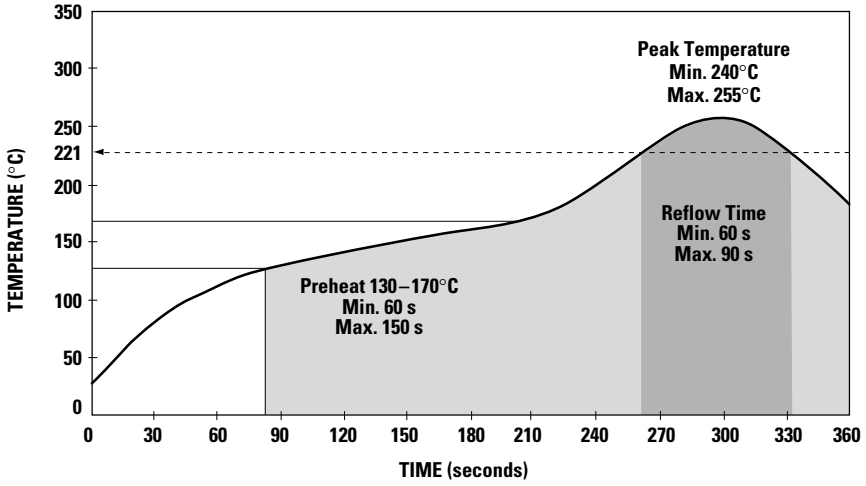
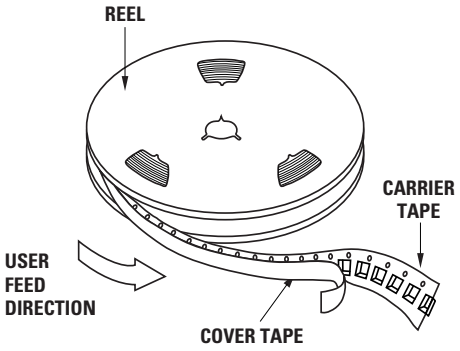
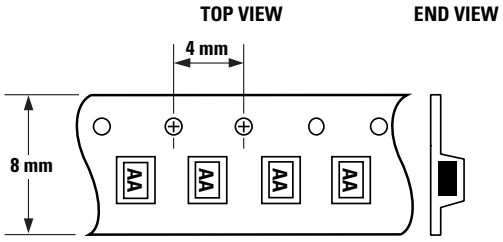


Figure 14. Surface Mount Assembly Temperature Profile.

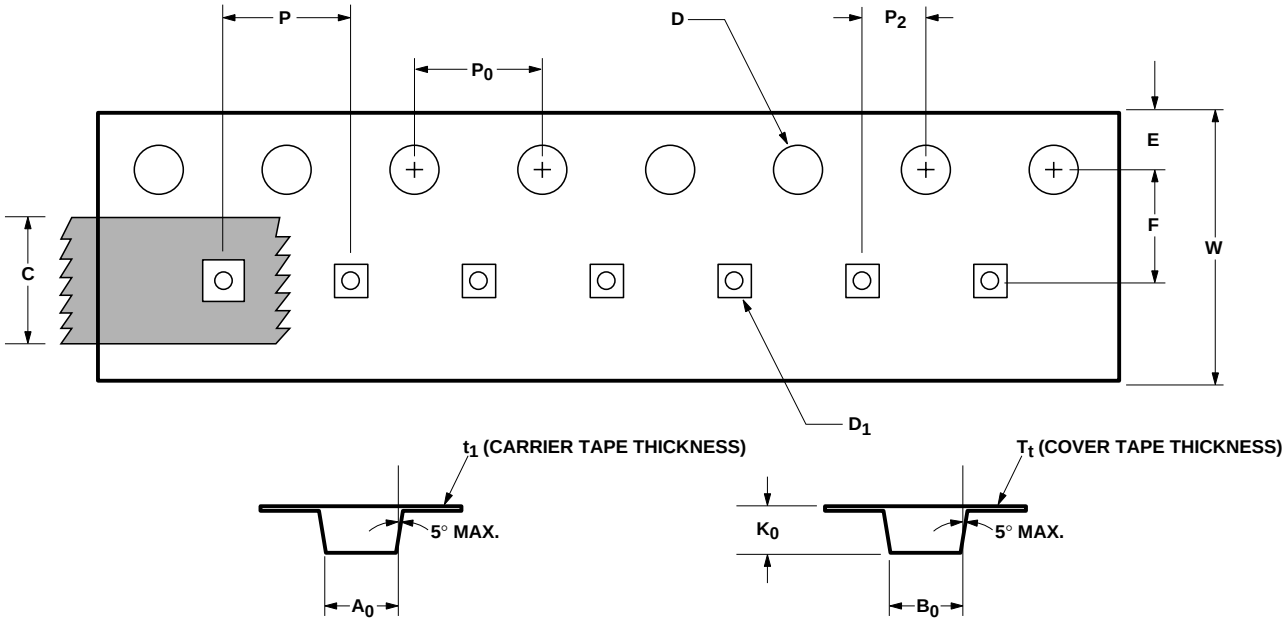
Device Orientation





Note: "AA" represents package marking code. Package marking is right side up with carrier tape perforations at top. Conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement." Standard quantity is 3,000 devices per reel.

Tape Dimensions and Product Orientation For Outline 4T (MiniPak 1412)



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	1.40 ± 0.05	0.055 ± 0.002
	WIDTH	B_0	1.63 ± 0.05	0.064 ± 0.002
	DEPTH	K_0	0.80 ± 0.05	0.031 ± 0.002
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	0.80 ± 0.05	0.031 ± 0.002
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.060 ± 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 - 0.10	0.315 + 0.012 - 0.004
	THICKNESS	t_1	0.254 ± 0.02	0.010 ± 0.001
COVER TAPE	WIDTH	C	5.40 ± 0.10	0.213 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.002 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

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