



## 512Kx8 MONOLITHIC SRAM

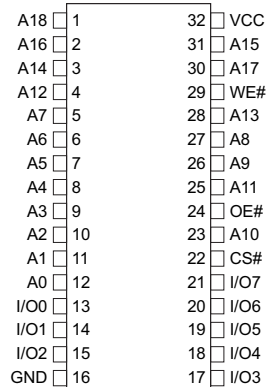
### FEATURES

- Access Times 70, 85, 100, 120ns
- MIL-STD-883 Compliant Devices Available
- Low Voltage Operation
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
  - 32 pin Ceramic DIP (Package 300)
  - 32 lead Ceramic SOJ (Package 101)
- Commercial, Industrial and Military Temperature Ranges
- Low Power CMOS
- Low Voltage Operation
  - 3.3V ± 10% Power Supply
- Low Power Data Retention
- TTL Compatible Inputs and Outputs

\* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

### EVOLUTIONARY PINOUT

32 DIP  
32 CSOJ (DE)  
TOP VIEW



### PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
Vcc	+3.3V Power Supply
GND	Ground



## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

## TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.6	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V
Operating Temp. (Mil.)	T <sub>A</sub>	-55	+125	°C

## CAPACITANCE

T<sub>A</sub> = +25°C

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	12	pF
Output capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V, f = 1.0MHz	12	pF

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

V<sub>CC</sub> = 3.3V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 3.6, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
Operating Supply Current	I <sub>CC</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6		25	mA
Standby Current	I <sub>SB</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6		400	μA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA, V <sub>CC</sub> = 3.0		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA, V <sub>CC</sub> = 3.0	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V



**AC CHARACTERISTICS**

V<sub>CC</sub> = 3.3V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	70		85		100		120		ns
Address Access Time	t <sub>AA</sub>		70		85		100		120	ns
Output Hold from Address Change	t <sub>OH</sub>	5		5		5		5		ns
Chip Select Access Time	t <sub>ACS</sub>		70		85		100		120	ns
Output Enable to Output Valid	t <sub>OE</sub>		35		40		50		60	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	10		10		10		10		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	5		5		5		5		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		25		25		35		35	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		25		25		35		35	ns

1. This parameter is guaranteed by design but not tested.

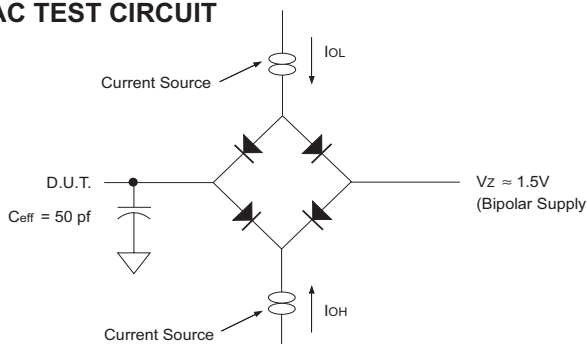
**AC CHARACTERISTICS**

V<sub>CC</sub> = 3.3V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	70		85		100		120		ns
Chip Select to End of Write	t <sub>CW</sub>	60		75		80		100		ns
Address Valid to End of Write	t <sub>AW</sub>	60		75		80		100		ns
Data Valid to End of Write	t <sub>DW</sub>	30		35		40		40		ns
Write Pulse Width	t <sub>WP</sub>	50		50		60		60		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		0		ns
Address Hold Time	t <sub>AH</sub>	5		5		5		5		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	5		5		5		5		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		25		25		35		35	ns
Data Hold from Write Time	t <sub>DH</sub>	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

**AC TEST CIRCUIT**



**AC TEST CONDITIONS**

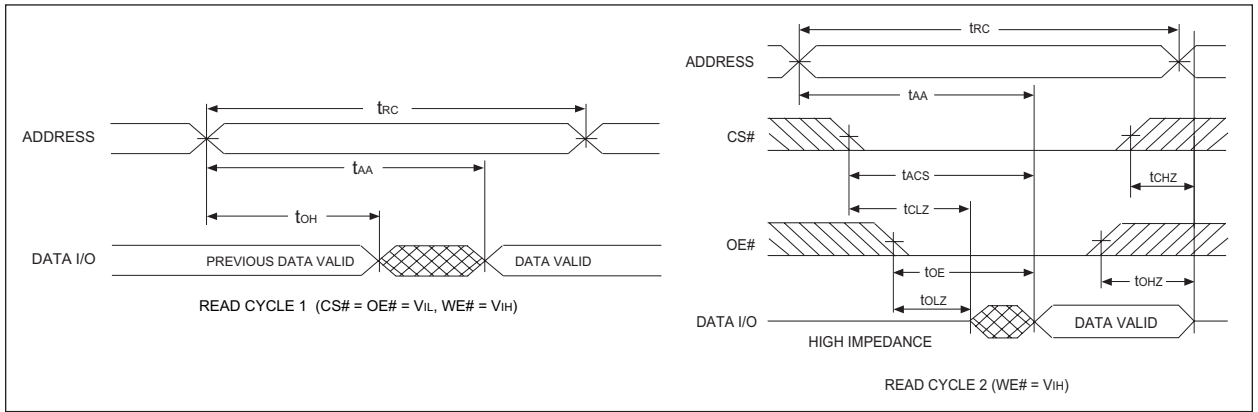
Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

**NOTES:**

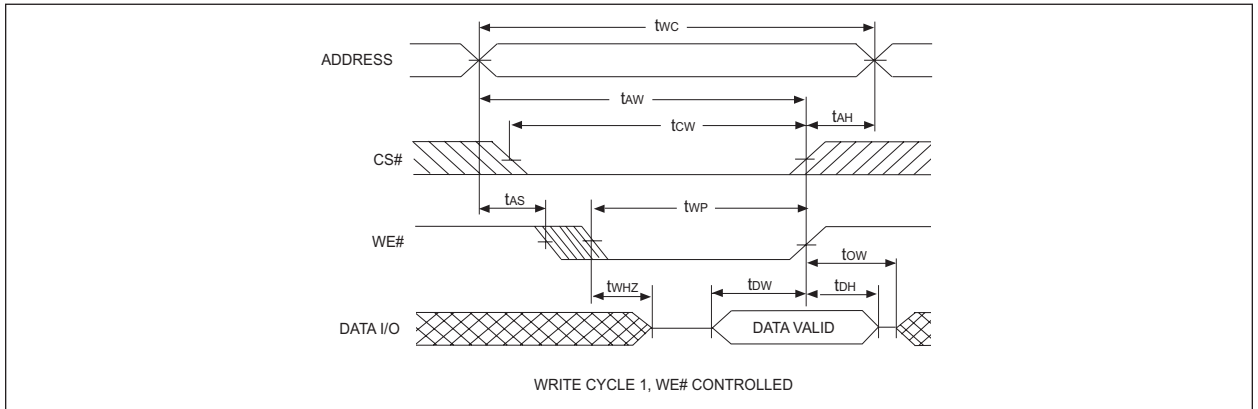
V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75 Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



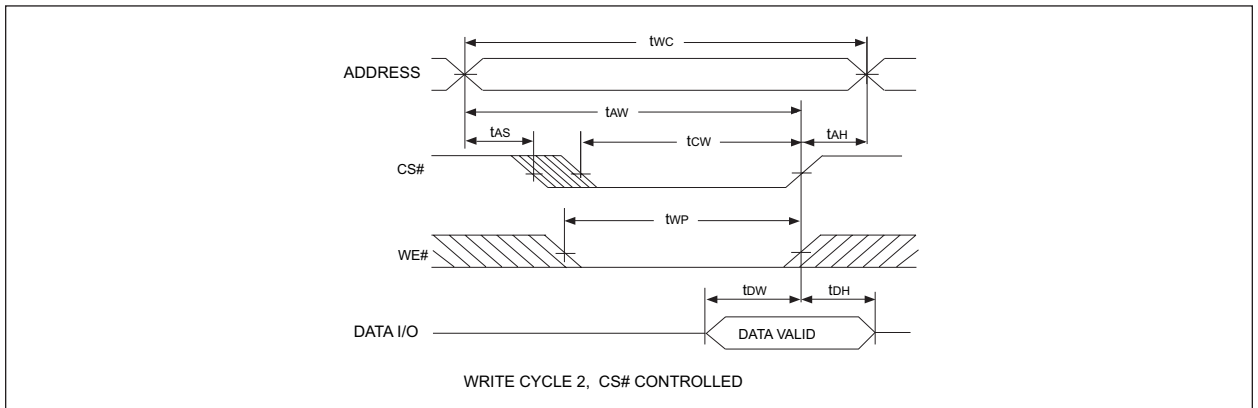
**TIMING WAVEFORM - READ CYCLE**



**WRITE CYCLE - WE# CONTROLLED**

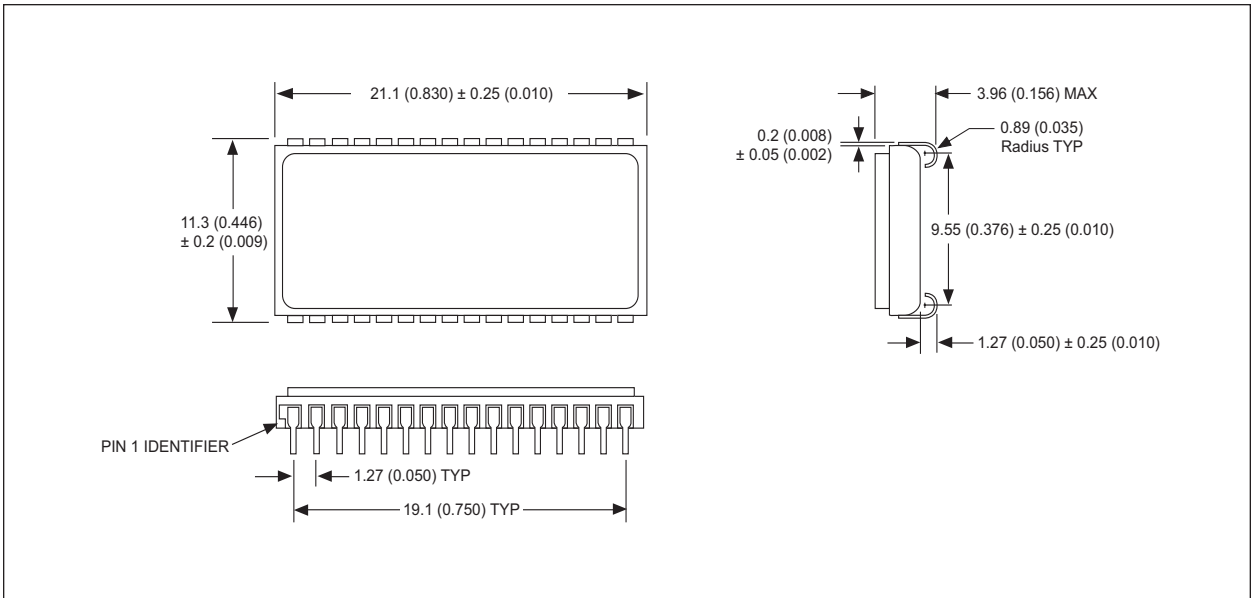


**WRITE CYCLE - CS# CONTROLLED**



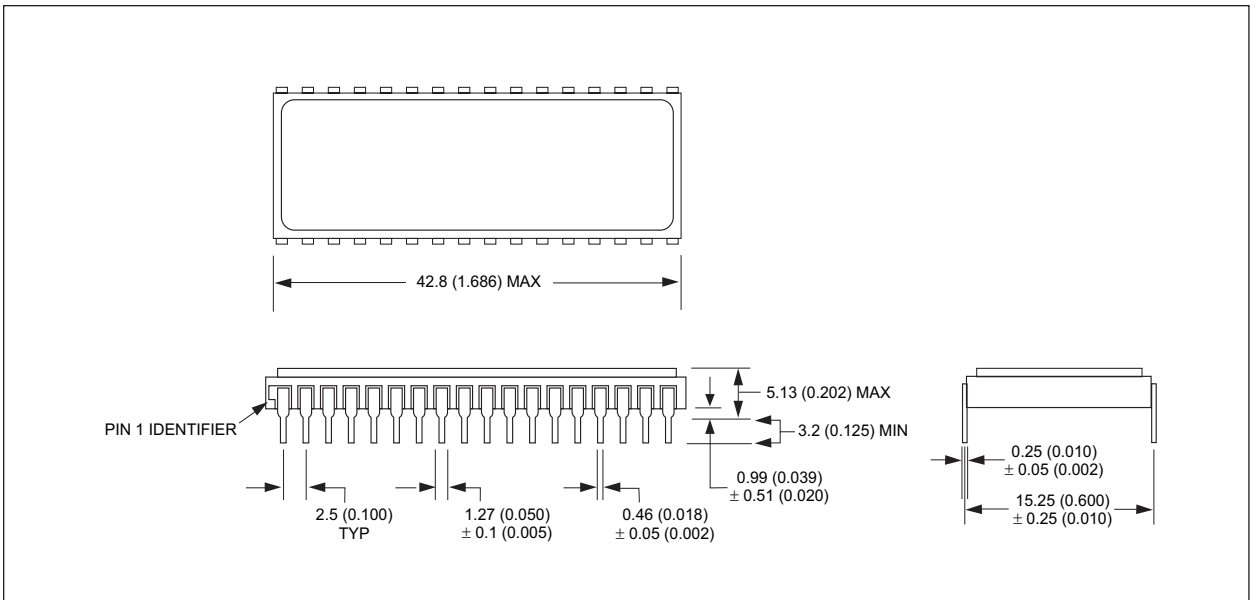


PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



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ORDERING INFORMATION

W M S 512K 8 V L - XXX X X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

SPECIAL PROCESSING:

- E = Epitaxial Layer

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE:

- C = 32 Pin Ceramic 0.600" DIP (Package 300)
- DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary

ACCESS TIME (ns)

IMPROVEMENT MARK

- L = Low Power Data Retention

Low Voltage Supply 3.3V ± 10%

ORGANIZATION, 512K x 8

SRAM

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.