4MX32 5V FLASH MODULE, SMD 5962-97612 (pending) *PRELIMINARY**

FEATURES

- Access Times of 100, 120, 150ns
- Packaging:
  - 66 pin, PGA Type, 1.385" square, Hermetic Ceramic HIP (Package 402).
  - 68 lead, 40mm Low Profile CQFP (Package 502), 3.5mm (0.140") height.
  - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880") square (Package 509) 4.57mm (0.180") height. Designed to fit JEDEC 68 lead 0.990CQFJ footprint (Fig. 3)
- Sector Architecture
  - 32 equal size sectors of 64KBytes per each 2Mx8 chip
  - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as 4Mx32
- User configurable as 8Mx16 or 16Mx8 in HIP and G4T packages.
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- $\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- $\overline{\text{RESET}}$ pin resets internal state machine to the read mode.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation, Separate Power and Ground Planes to improve noise immunity

**This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

Note:
For programming information refer to Flash Programming 16M5 Application Note.

FIG. 1 PIN CONFIGURATION FOR WF4M32-XH2X5

TOP VIEW

1	12	23		34	45	56
I/O8	$\overline{\text{RESET}}$	I/O15		I/O24	Vcc	I/O31
I/O9	$\overline{\text{CS2}}$	I/O14		I/O25	$\overline{\text{CS4}}$	I/O30
I/O10	GND	I/O13		I/O26	NC	I/O29
A14	I/O11	I/O12		A7	I/O27	I/O28
A16	A10	$\overline{\text{OE}}$		A12	A4	A1
A11	A9	A17		A21	A5	A2
A0	A15	$\overline{\text{WE}}$		A13	A6	A3
A18	Vcc	I/O7		A8	A20	I/O23
I/O0	$\overline{\text{CS1}}$	I/O6		I/O16	$\overline{\text{CS3}}$	I/O22
I/O1	A19	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-21	Address Inputs
$\overline{\text{WE}}$	Write Enables
$\overline{\text{CS}}$1-4	Chip Selects
$\overline{\text{OE}}$	Output Enable
Vcc	Power Supply
GND	Ground
$\overline{\text{RESET}}$	Reset

BLOCK DIAGRAM

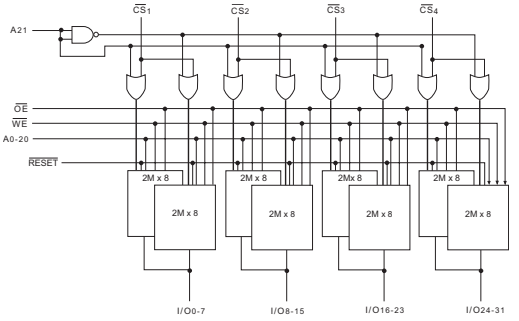
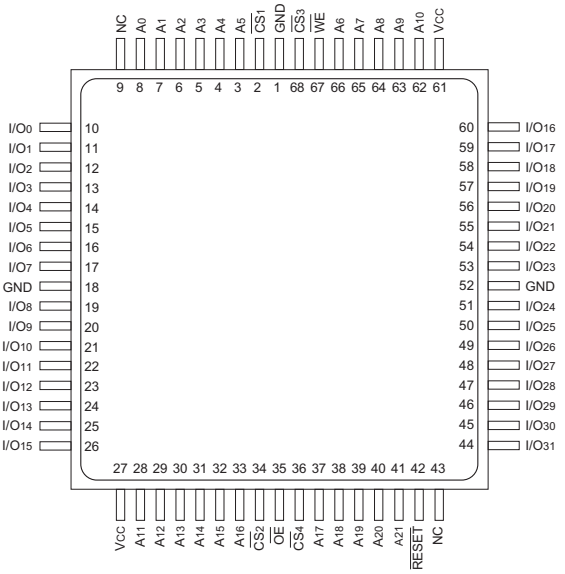


FIG. 2 PIN CONFIGURATION FOR WF4M32-XG4TX5

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-21	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
$\overline{RESET}$	Reset
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

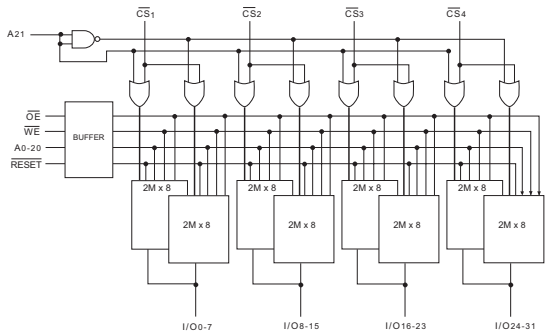
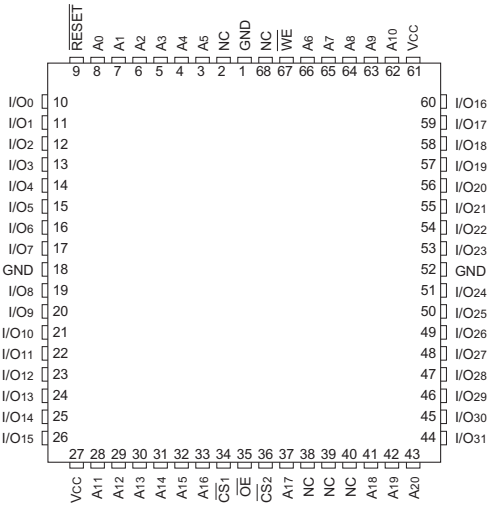
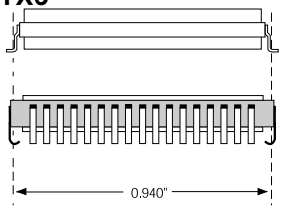


FIG. 3 PIN CONFIGURATION FOR WF4M32-XG2TX5

TOP VIEW



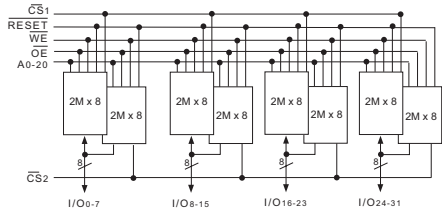


The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}_{1-2}$	Banks Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
$\overline{RESET}$	Reset

BLOCK DIAGRAM



Note: $\overline{CS1}$ & $\overline{CS2}$ are used as bank select

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-2.0 to +7.0	V
Power Dissipation	P_T	8	W
Storage Temperature	Tstg	-65 to +125	°C
Short Circuit Output Current	I_{OS}	100	mA
Endurance - Write/Erase Cycles (Mil Temp)		100,000 min	cycles
Data Retention (Mil Temp)		20	years

CAPACITANCE (pF)
(T_A = +25°C, V_{IN} = OV, f = 1.0MHz)

Parameter	Symbol	HIP (H2)	CQFP (G2T)	CQFP(G4T)
$\overline{OE}$ capacitance	C_{OE}	75	75	20
$\overline{WE}$ capacitance	C_{WE}	75	75	20
$\overline{CS}$ capacitance	C_{CS}	20	50	20
Data I/O capacitance	$C_{I/O}$	30	30	30
Address input capacitance	C_{AD}	75	75	20

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	-	+0.8	V
Operating Temperature (Mil.)	T_A	-55	-	+125	°C
Operating Temperature (Ind.)	T_A	-40	-	+85	°C

DC CHARACTERISTICS - CMOS COMPATIBLE
(V_{CC} = 5.0V, GND = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol	Conditions	HIP		G2T		G4T		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		320		215		345	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		420		295		445	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 5.5, CS = V_{IH}, f = 5MHz, RESET = $\overline{V_{IH}}$		20		2.0		95	mA
Output Low Voltage	V_{OL}	I_{OL} = 12.0 mA, V_{CC} = 4.5		0.45		0.45		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x Vcc		0.85 x Vcc		0.85 x Vcc		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	4.2	3.2	4.2	3.2	4.2	V

NOTES:

1. *The Icc current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *Icc active while Embedded Algorithm (program or erase) is in progress.*
3. *DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V*

HIP = 66 pin, PGA Type, 1.385" square, Hermetic Ceramic HIP (Package 402).

G2T = 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880") square. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3) (Package 509)

G4T = 68 lead, 40mm Low Profile CQFP, 3.5mm (0.140") (Package 502)

AC CHARACTERISTICS FOR G2T PACKAGE – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED (VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns
$\overline{RESET}$ Pulse Width		t_{RP}	500		500		500		ns

NOTES:
1. Typical value for tWHWH1 is 7µs.
2. Typical value for tWHWH2 is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS FOR G2T PACKAGE – READ-ONLY OPERATIONS (VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	100		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		100		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		100		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	t_{EHQZ}	t_{DF}		20		30		35	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		30		35	ns
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		ns
RST Low to Read Mode (1)		t_{Ready}		20		20		20	µs

1. Guaranteed by design, not tested.

AC CHARACTERISTICS FOR G2T PACKAGE – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED
(VCC = 5.0V, GND = 0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns

NOTES:

1. *Typical value for tWHWH1 is 7µs.*
2. *Typical value for tWHWH2 is 1sec.*
3. *Typical value for Chip Erase Time is 32sec.*
4. *For Toggle and Data Polling.*

AC CHARACTERISTICS FOR G4T AND H2 PACKAGES – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED (VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	15		15		15		ns
Address Hold Time (1)	t_{WLAX}	t_{AH}	45		50		50		ns
Write Enable Pulse Width High (2)	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Programming Operation (3)	t_{WHWH1}			300		300		300	µs
Sector Erase (4)	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (5)				256		256		256	sec
Output Enable Hold Time (6)		t_{OEH}	10		10		10		ns
$\overline{RESET}$ Pulse Width		t_{RP}	500		500		500		ns

NOTES:

1. *A21 must be held constant until $\overline{WE}$ or $\overline{CS}$ go high, whichever occurs first.*
2. *Guaranteed by design, but not tested.*
3. *Typical value for tWHWH1 is 7µs.*
4. *Typical value for tWHWH2 is 1sec.*
5. *Typical value for Chip Erase Time is 32sec.*
6. *For Toggle and Data Polling.*

AC CHARACTERISTICS FOR G4T AND H2 PACKAGES – READ-ONLY OPERATIONS (VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	100		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		100		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		100		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		50		50		55	ns
Chip Select High to Output High Z	t_{EHQZ}	t_{DF}		40		45		45	ns
Output Enable High to Output High Z	t_{GHQZ}	t_{DF}		40		45		45	ns
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		ns
$\overline{RST}$ Low to Read Mode		t_{Ready}		20		20		20	µs

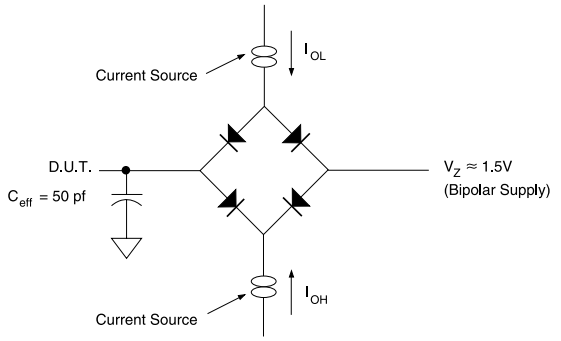
AC CHARACTERISTICS FOR G4T AND H2 PACKAGES – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED (VCC = 5.0V, GND = 0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	15		15		15		ns
Address Hold Time (1)	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (2)	t_{WHWH1}			300		300		300	µs
Sector Erase Time (3)	t_{WHWH2}			15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (4)				256		256		256	sec
Output Enable Hold Time (5)		t_{OEH}	10		10		10		ns

NOTES:

1. *A21 must be held constant until $\overline{WE}$ or $\overline{CS}$ go high, whichever occurs first.*
2. *Typical value for tWHWH1 is 7µs.*
3. *Typical value for tWHWH2 is 1sec.*
4. *Typical value for Chip Erase Time is 32sec.*
5. *For Toggle and Data Polling.*

FIG. 4 AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0$, $V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
VZ is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance Z0 = 75Ω.
VZ is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 5 RESET TIMING DIAGRAM

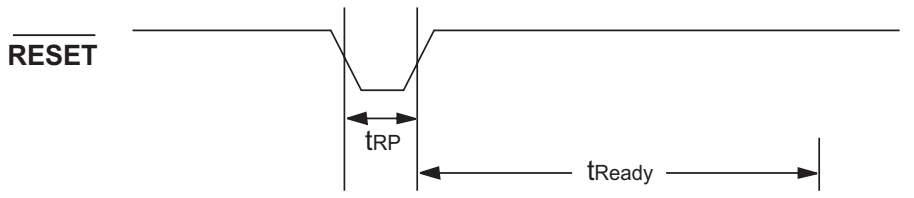


FIG. 6 AC WAVEFORMS FOR READ OPERATIONS

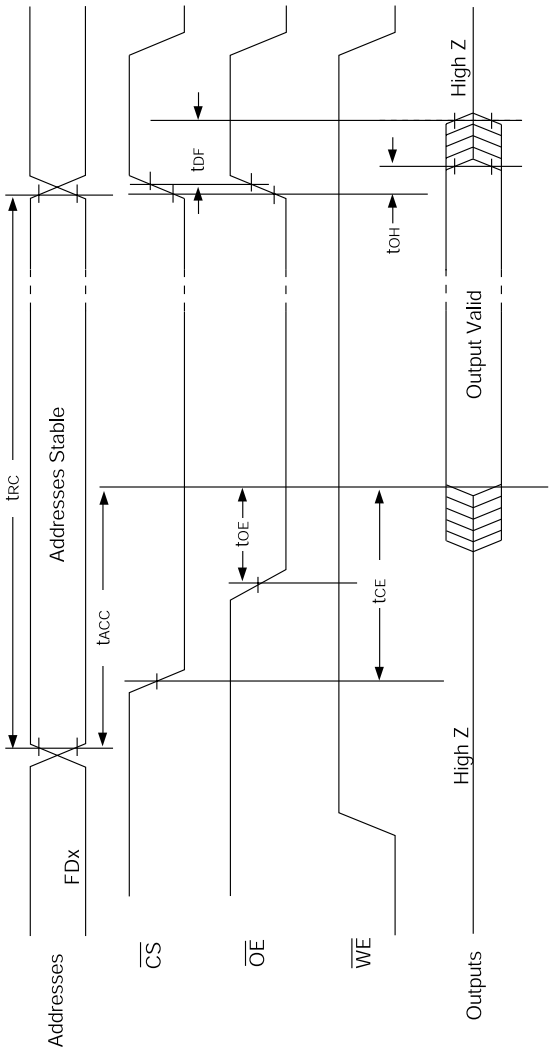
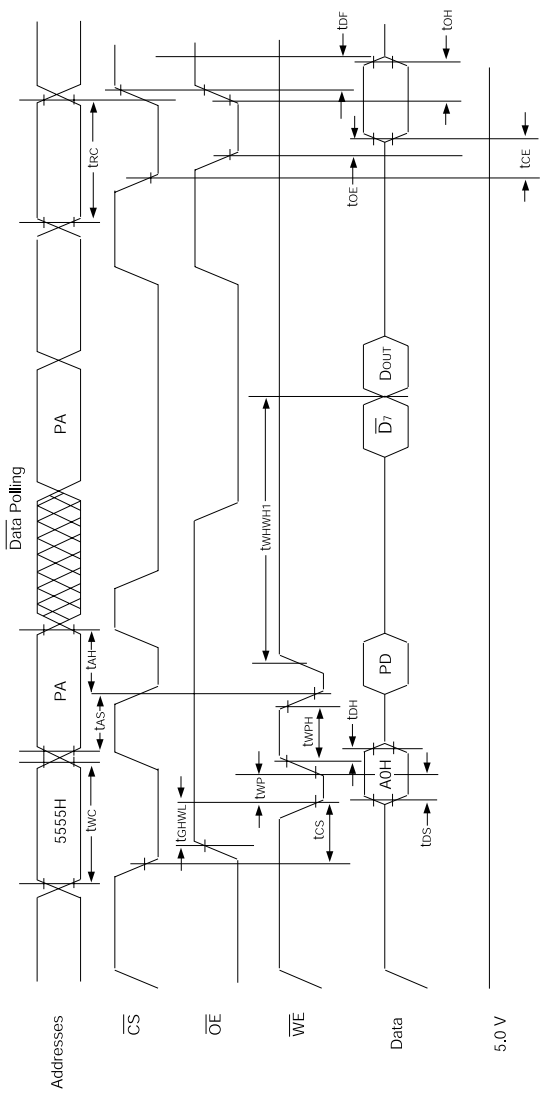


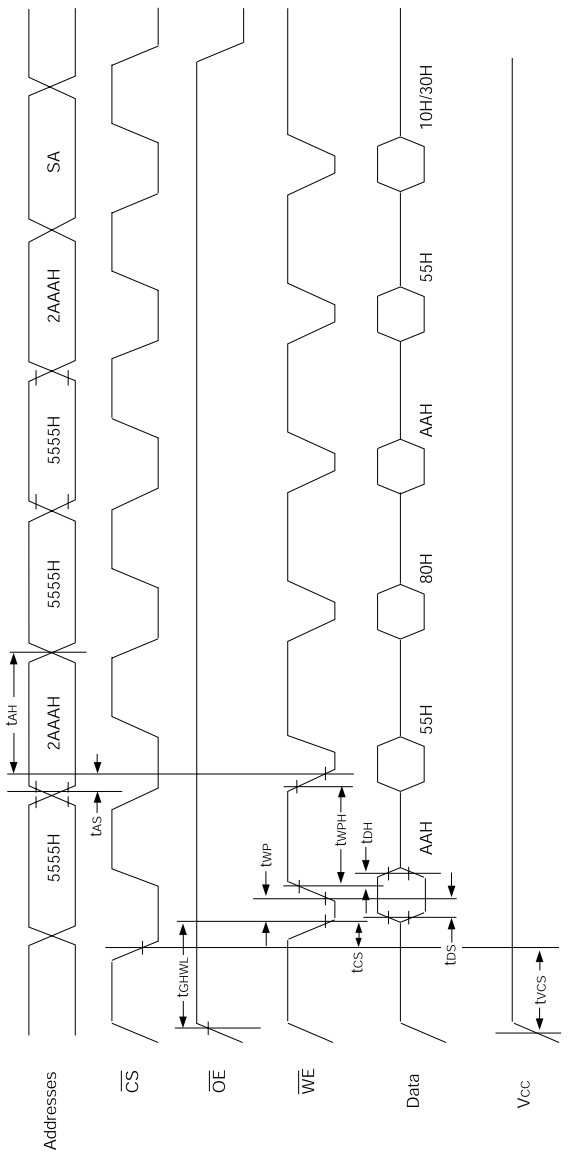
FIG. 7 WRITE/ERASE/PROGRAM OPERATION, $\overline{WE}$ CONTROLLED



NOTES:

1. *PA is the address of the memory location to be programmed.*
2. *PD is the data to be programmed at byte address.*
3. *$\overline{D_7}$ is the output of the complement of the data written to each chip.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

FIG. 8 AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:
1. SA is the sector address for Sector Erase.

FIG. 9 AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS

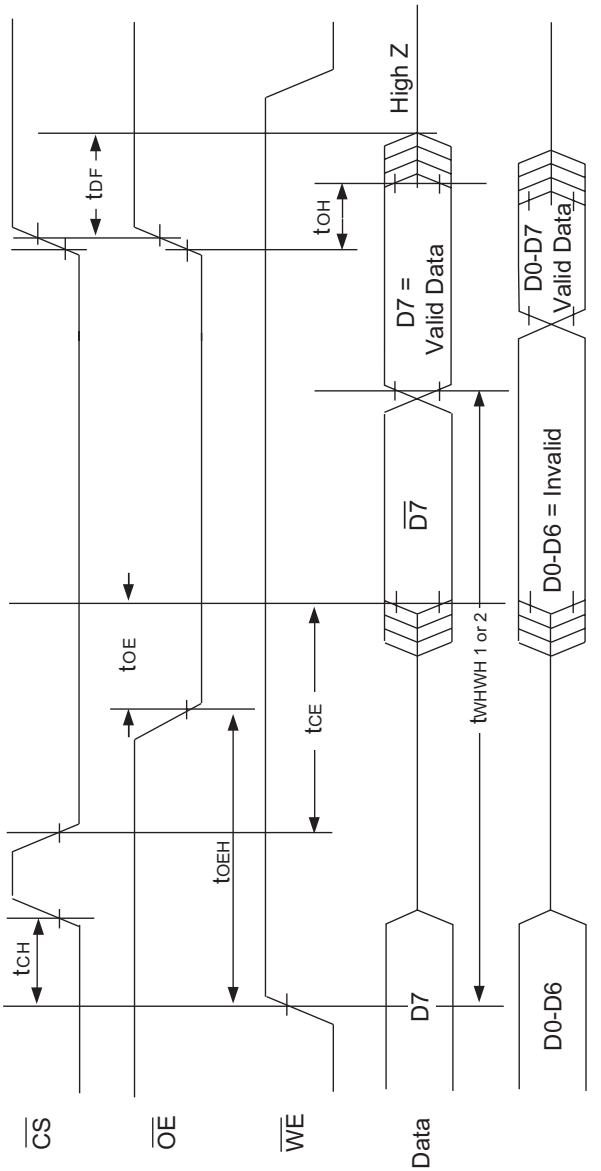
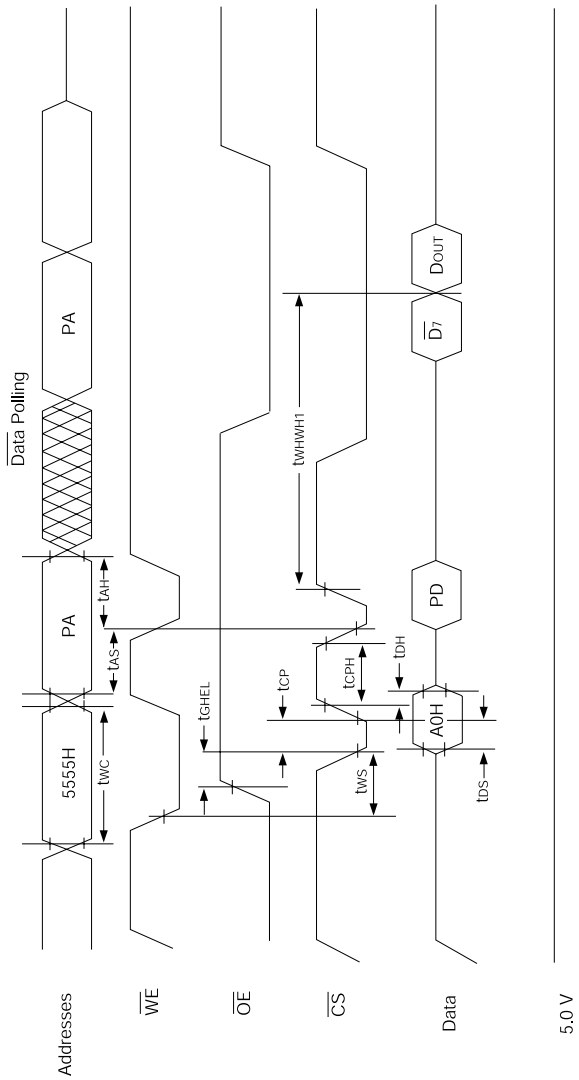


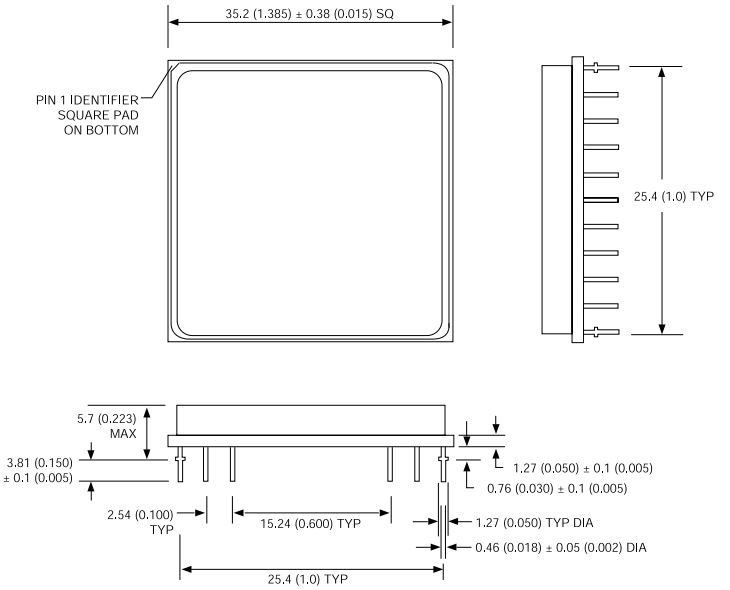
FIG. 10 ALTERNATE $\overline{CS}$ CONTROLLED PROGRAMMING OPERATION TIMINGS



Notes:

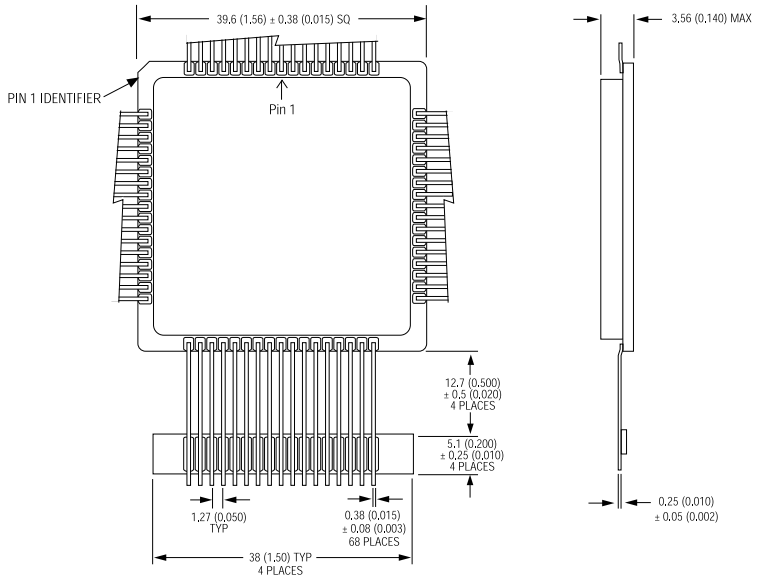
1. *PA represents the address of the memory location to be programmed.*
2. *PD represents the data to be programmed at byte address.*
3. *$\overline{D7}$ is the output of the complement of the data written to each chip.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates the last two bus cycles of a four bus cycle sequence.*

PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



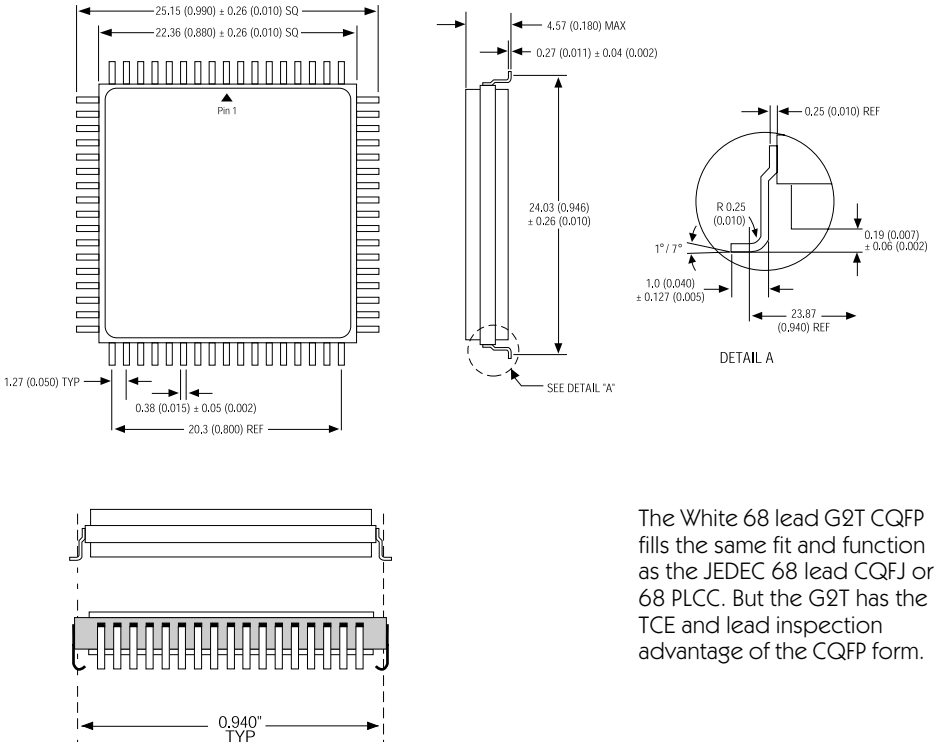
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

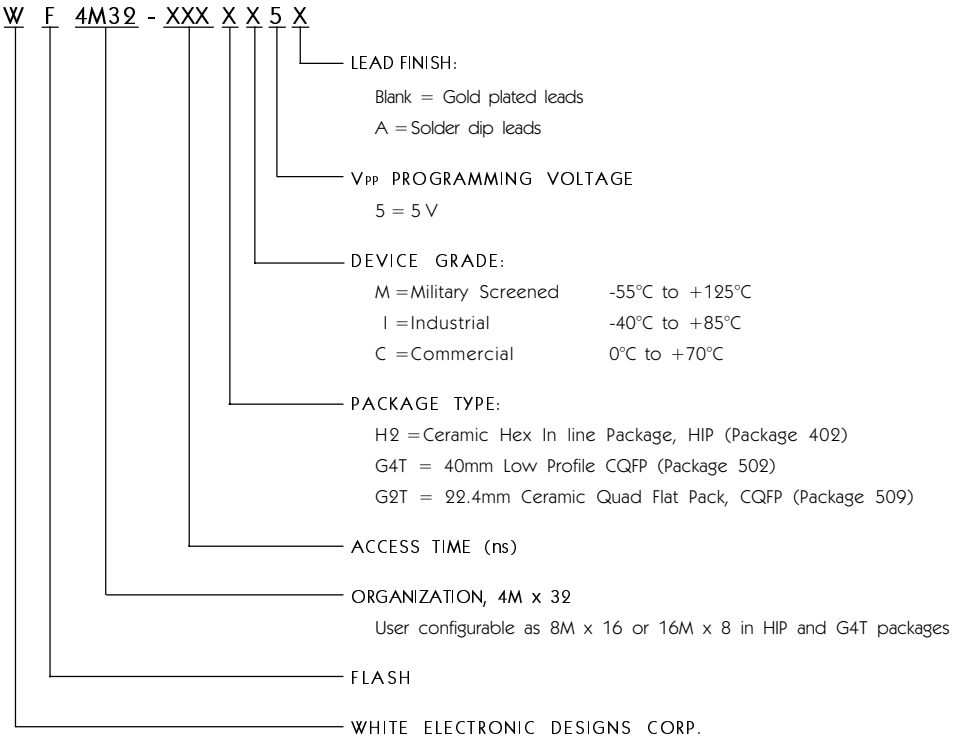
PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



DEVICE	TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
4M x 32	5V Flash Module	64KByte	150ns	66 pin HIP (H2)	5962-97612 01HXX*
4M x 32	5V Flash Module	64KByte	120ns	66 pin HIP (H2)	5962-97612 02HXX*
4M x 32	5V Flash Module	64KByte	100ns	66 pin HIP (H2)	5962-97612 03HXX*
4M x 32	5V Flash Module	64KByte	150ns	68 lead CQFP Low Profile (G4T)	5962-97612 01HXX*
4M x 32	5V Flash Module	64KByte	120ns	68 lead CQFP Low Profile (G4T)	5962-97612 02HXX*
4M x 32	5V Flash Module	64KByte	100ns	68 lead CQFP Low Profile (G4T)	5962-97612 03HXX*
4M x 32	5V Flash Module	64KByte	150ns	68 lead CQFP Low Profile (G2T)	5962-97612 01HXX*
4M x 32	5V Flash Module	64KByte	120ns	68 lead CQFP Low Profile (G2T)	5962-97612 02HXX*
4M x 32	5V Flash Module	64KByte	100ns	68 lead CQFP Low Profile (G2T)	5962-97612 03HXX*

Pending