V43648Y04V(C)TG-10PC
3.3 VOLT 8M x 64 HIGH PERFORMANCE 100 MHZ SDRAM UNBUFFERED SODIMM

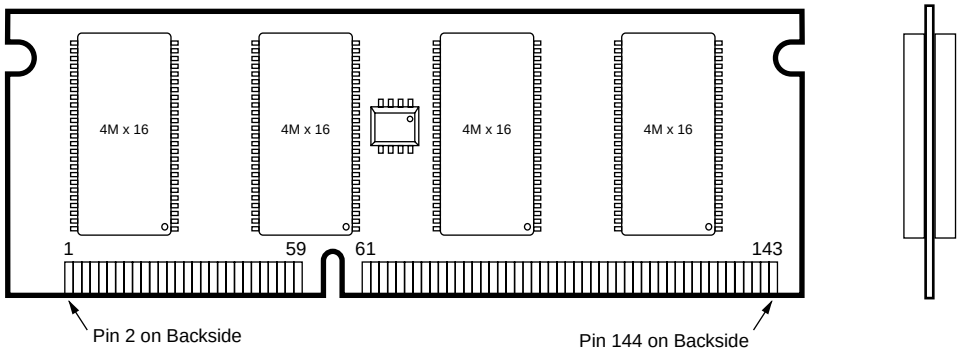
Features

- JEDEC-standard 144 pin, Small-Outline, Dual in line Memory Module (SODIMM)
- Serial Presence Detect with E^2PROM
- Nonbuffered
- Fully Synchronous, All Signals Registered on Positive Edge of System Clock
- Single +3.3V (± 0.3V) Power Supply
- All Device Pins are LVTTL Compatible
- 4096 Refresh Cycles every 64 ms
- Self-Refresh Mode
- Internal Pipelined Operation; Column Address can be changed every System Clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- Auto Precharge and Piecharge all Banks by A10
- Data Mask Function by DQM
- Mode Register Set Programming
- Programmable ($\overline{CAS}$ Latency: 2, 3 Clocks)

Description

The V43648Y04V(C)TG-10PC memory module is organized 8,388,608 x 64 bits in a 144 pin SODIMM. The 8M x 64 memory module uses 8 Mosel-Vitelic 4M x 16 SDRAM. The x64 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

Part Number	Speed Grade	Configuration
V43648Y04V(C)TG-10PC	-10PC (100 MHz)	8M x 64



Pin Configurations (Front Side/Back Side)

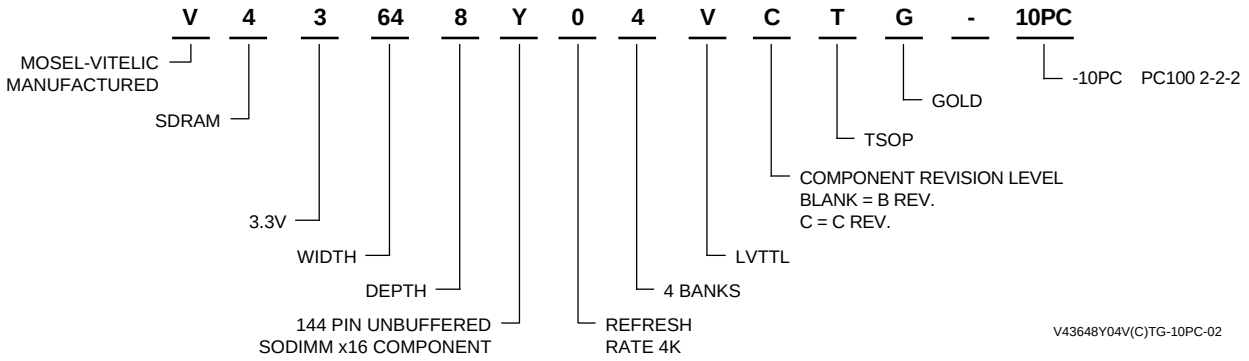
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	25	DQMB1	49	DQ13	73	NC	97	DQ22	121	DQ24
2	VSS	26	DQMB5	50	DQ45	74	CLK1	98	DQ54	122	DQ56
3	DQ0	27	VDD	51	DQ14	75	VSS	99	DQ23	123	DQ25
4	DQ32	28	VDD	52	DQ46	76	VSS	100	DQ55	124	DQ57
5	DQ1	29	A0	53	DQ15	77	NC	101	VDD	125	DQ26
6	DQ33	30	A3	54	DQ47	78	NC	102	VDD	126	DQ58
7	DQ2	31	A1	55	VSS	79	NC	103	A6	127	DQ27
8	DQ34	32	A4	56	VSS	80	NC	104	A7	128	DQ59
9	DQ3	33	A2	57	NC	81	VDD	105	A8	129	VDD
10	DQ35	34	A5	58	NC	82	VDD	106	BA0	130	VDD
11	VDD	35	VSS	59	NC	83	DQ16	107	VSS	131	DQ28
12	VDD	36	VSS	60	NC	84	DQ48	108	VSS	132	DQ60
13	DQ4	37	DQ8	61	CLK0	85	DQ17	109	A9	133	DQ29
14	DQ36	38	DQ40	62	CKE0	86	DQ49	110	BA1	134	DQ61
15	DQ5	39	DQ9	63	VDD	87	DQ18	111	A10	135	DQ30
16	DQ37	40	DQ41	64	VDD	88	DQ50	112	A11	136	DQ62
17	DQ6	41	DQ10	65	$\overline{RAS}$	89	DQ19	113	VDD	137	DQ31
18	DQ38	42	DQ42	66	$\overline{CAS}$	90	DQ51	114	VDD	138	DQ63
19	DQ7	43	DQ11	67	$\overline{WE}$	91	VSS	115	DQMB2	139	VSS
20	DQ39	44	DQ43	68	CKE1	92	VSS	116	DQMB6	140	VSS
21	VSS	45	VDD	69	$\overline{CS0}$	93	DQ20	117	DQMB3	141	SDA
22	VSS	46	VDD	70	NC	94	DQ52	118	DQMB7	142	SCL
23	DQMB0	47	DQ12	71	$\overline{CS1}$	95	DQ21	119	VSS	143	VDD
24	DQMB4	48	DQ44	72	NC	96	DQ53	120	VSS	144	VDD

Note:
1. $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ $\overline{CAS}$x, $\overline{CS}$x are active low signals.

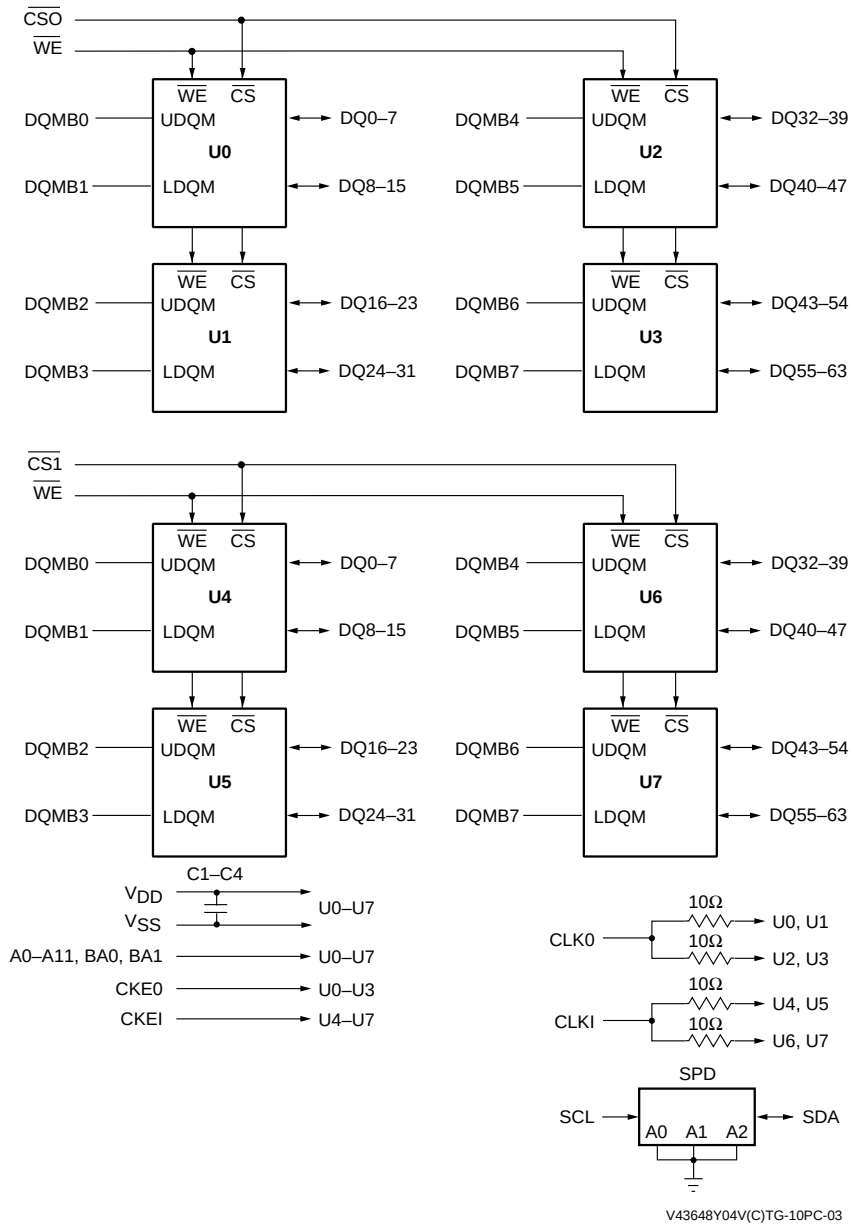
Pin Names

A0–A11, BA0, BA1	Address, Bank Select
DQ0–DQ63	Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobes
$\overline{CAS}$	Column Address Strobes
$\overline{WE}$	Write Enable
$\overline{CS0}$, $\overline{CS1}$	Chip Select
DQMB0–DQMB7	Output Enable
CKE0, CKE1	Clock Enable
CLK0, CLK1	Clock
SDA	Serial Input/Output
SCL	Serial Clock
VDD	Power Supply
VSS	Ground
NC	No Connect (Open)

Part Number Information



Block Diagram



Serial Presence Detect Information

A serial presence detect storage device – E^2PROM – is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus)

SPD-Table for -10 PC modules:

Byte Number	Function Described	SPD Entry Value	Hex Value
			100 MHz -10PC
0	Number of SPD bytes	128	80
1	Total bytes in Serial PD	256	08
2	Memory Type	SDRAM	04
3	Number of Row Addresses (without BS bits)	12	0C
4	Number of Column Addresses (for x16 SDRAM)	8	08
5	Number of DIMM Banks	2	02
6	Module Data Width	64	40
7	Module Data Width (continued)	0	00
8	Module Interface Levels	LVTTL	01
9	SDRAM Cycle Time at CL=3	10.0 ns	A0
10	SDRAM Access Time from Clock at CL=3	6.0 ns	60
11	Dimm Config (Error Det/Corr.)	none	00
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80
13	SDRAM width, Primary	x16	10
14	Error Checking SDRAM Data Width	n/a / x8	00
15	Minimum Clock Delay from Back to Back Random Column Address	t_{ccd} = 1 CLK	01
16	Burst Length Supported	1, 2, 4, 8 & full Page	8F
17	Number of SDRAM Banks	4	04
18	Supported $\overline{CAS}$ Latencies	CL = 2 & 3	06
19	$\overline{CS}$ Latencies	$\overline{CS}$ Latency = 0	01
20	$\overline{WE}$ Latencies	WL = 0	01
21	SDRAM DIMM Module Attributes	Non Buffered/Non Reg.	00
22	SDRAM Device Attributes: General	Vcc tol ± 10%	0E
23	Minimum Clock Cycle Time at $\overline{CAS}$ Latency = 2	10.0 ns	A0
24	Maximum Data Access Time from Clock for CL = 2	6.0 ns	60
25	Minimum Clock Cycle Time at CL = 1	Not Supported	00
26	Maximum Data Access Time from Clock at CL = 1	Not Supported	00
27	Minimum Row Precharge Time t_{RP}	20 ns	14
28	Minimum Row Active to Row Active Delay t_{RRD}	16 ns	10
29	Minimum RAS to $\overline{CAS}$ Delay t_{RCD}	20 ns	14

SPD-Table for -10 PC modules: (Continued)

Byte Number	Function Described	SPD Entry Value	Hex Value 100 MHz -10PC
30	Minimum RAS Pulse Width t_{RAS}	45 ns	2D
31	Module Bank Density (Per Bank)	32 MByte	08
32	SDRAM Input Setup Time	2.0 ns	20
33	SDRAM Input Hold Time	1 ns	10
34	SDRAM Data Input Setup Time	2.0 ns	20
35	SDRAM Data Input Hold Time	1 ns	10
36-61	Superset Information (May be used in Future)		00
62	SPD Revision	Revision 1	12
63	Checksum for Bytes 0 - 62		FD
64-125	Manufacturers's Information (Optional) (FFh if not used)		XX
126	Max. Frequency Specification	100 MHz	64
127	100 MHz Support Details		AF
128+	Unused Storage Location		00

Absolute Maximum Ratings

Parameter	Max.	Units
Voltage on VDD Supply Relative to V_{SS}	-1 to 4.6	V
Voltage on Input Relative to V_{SS}	-1 to 4.6	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to 125	°C
Power Dissipation	4	W

DC Characteristics

T_A = 0°C to 70°C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3V ± 0.3V

Symbol	Parameter	Limit Values Min.	Limit Values Max.	Unit
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	–0.3	0.8	V
V_{OH}	Output High Voltage (I_{OUT} = –2.0 mA)	2.4	—	V
V_{OL}	Output Low Voltage (I_{OUT} = 2.0 mA)	—	0.4	V
$I_{I(L)}$	Input Leakage Current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0V)	–20	20	µA
$I_{O(L)}$	Output leakage current (DQ is disabled, 0V < V_{OUT} < V_{CC})	–20	20	µA

Capacitance

T_A = 0°C to 70°C; V_{DD} = 3.3V ± 0.3V, f = 1 MHz

Symbol	Parameter	Limit Values	Unit
C_{I1}	Input Capacitance (A0 to A11, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	20	pF
C_{I2}	Input Capacitance ($\overline{CS0}$, $\overline{CSI}$)	25	pF
C_{ICL}	Input Capacitance (CLK0-CLK1)	28	pF
C_{I3}	Input Capacitance (CKE0, CKEI)	20	pF
C_{I4}	Input Capacitance (DQMB0-DQMB7)	10	pF
C_{SC}	Input Capacitance (SCL, SA0-2)	8	pF
C_{IO}	Input/Output Capacitance	10	pF

Standby and Refresh Currents[1]

T_A = 0°C to 70°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions	8M x 64	Unit	Note
$I_{CC}1$	Operating Current	Burst length = 4, CL = 3 t_{RC}> = t_{RC}(min), t_{CK}> = t_{CK}(min), IO = 0 mA 2 Bank Interleave Operation	440	mA	1,2
$I_{CC}2P$	Precharged Standby Current in Power Down Mode	CKE< = V_{IL}(max), t_{CK}> = t_{CK}(min)	16	mA	
$I_{CC}2N$	Precharged Standby Current in Non-Power Down Mode	CKE> = V_{IH}(min), t_{CK}> = t_{CK}(min), Input changed once in 3 cycles	140	mA	$\overline{CS}$ = High
$I_{CC}3P$	Active Standby Current in Power Down Mode	CKE< = V_{IL}(max), t_{CK}> = t_{CK}(min)	40	mA	
$I_{CC}3N$	Active Standby Current in Non-Power Down Mode	CKE> = V_{IH}(min), t_{CK}> = t_{CK}(min), Input changed one time	260	mA	$\overline{CS}$ = High
$I_{CC}4$	Burst Operating Current	Burst length = Full Page, t_{RC} = Infinite, CL = 3, t_{CK}> = t_{CK}(min), IO = 0 mA 2 Banks Activated	440	mA	1, 2
$I_{CC}5$	Auto Refresh Current	t_{RC}>= t_{RC}(min)	1100	mA	1,2
$I_{CC}6$	Self Refresh Current	CKE = <0,2 V	4	mA	1,2

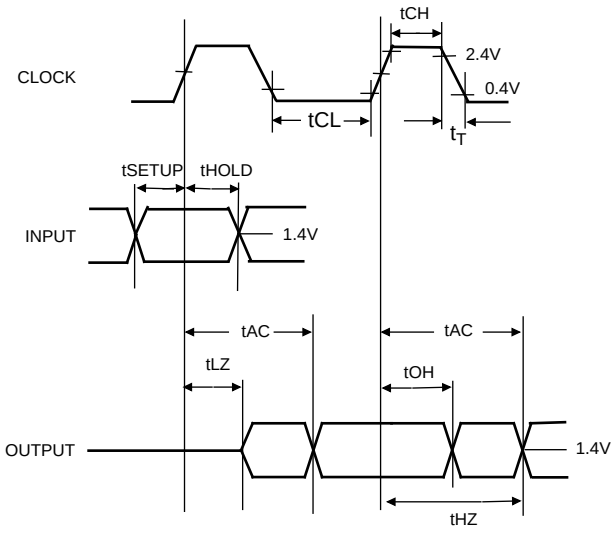
AC Characteristics [3,4]

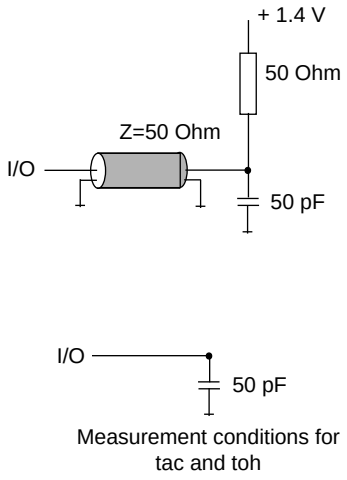
T_A = 0° to 70°C; V_{SS} = 0V; V_{CC} = 3.3V ± 0.3V, t_T = 1 ns

#	Symbol	Parameter	Limit Values -10PC Min.	Limit Values -10PC Max.	Unit	Note
Clock and Clock Enable						
1	t_{CK}	Clock Cycle Time				
		$\overline{CAS}$ Latency = 3	10		ns	
		$\overline{CAS}$ Latency = 2	10		ns	
2	f_{CK}	System frequency				
		$\overline{CAS}$ Latency = 3	–	100	MHz	
		$\overline{CAS}$ Latency = 2	–	100	MHz	
3	t_{AC}	Clock Access Time				4,5
		$\overline{CAS}$ Latency = 3	–	6	ns	
		$\overline{CAS}$ Latency = 2	–	6	ns	
4	t_{CH}	Clock High Pulse Width	3	–	ns	6
5	t_{CL}	Clock Low Pulse Width	3	–	ns	6
6	t_{CS}	Input Setup time	2	–	ns	7
7	t_{CH}	Input Hold Time	1	–	ns	7
8	t_{CKSP}	CKE Setup Time (Power down mode)	2	–	ns	8
9	t_{CKSR}	CKE Setup Time (Self Refresh Exit)	8	–	ns	9
10	t_T	Transition time (rise and fall)	1	–	ns	
Common Parameters						
11	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay	20	–	ns	
12	t_{RC}	Cycle Time	70	120k	ns	
13	t_{RAS}	Active Command Period	45	–	ns	
14	t_{RP}	Precharge Time	20	–	ns	
15	t_{RRD}	Bank to Bank Delay Time	16	–	ns	
16	t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	1	–	CLK	
Refresh Cycle						
17	t_{SREX}	Self Refresh Exit Time	10	–	ns	9
18	t_{REF}	Refresh Period (4096 cycles)	64	–	ms	8
Read Cycle						
19	t_{OH}	Data Out Hold Time	3	–	ns	4
20	t_{LZ}	Data Out to Low Impedance Time	0	–	ns	
21	t_{HZ}	Data Out to High Impedance Time	3	9	ns	10
22	t_{DQZ}	DQM Data Out Disable Latency	2	–	CLK	
Write Cycle						
23	t_{DPL}	Data input to Precharge (write recovery)	1	–	CLK	
24	t_{DAL}	Data In to Active/refresh	5	–	CLK	11
25	t_{DQW}	DQM Write Mask Latency	0	–	CLK	

Notes:

1. The specified values are valid when addresses are changed no more than once during t_{CK}(min.) and when No Operation commands are registered on every rising clock edge during t_{RC}(min). Values are shown per module bank.
2. The specified values are valid when data inputs (DQ's) are stable during t_{RC}(min.).
3. All AC characteristics are shown for device level.
   An initial pause of 100 µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have V_{IL} = 0.4V and V_{IH} = 2.4V with the timing referenced to the 1.4V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown. Specific tac and toh parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0V.



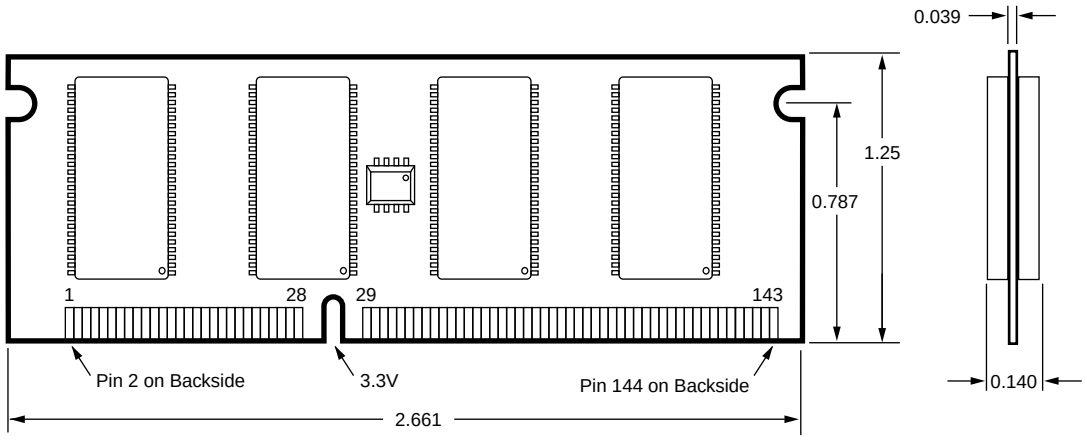


Measurement conditions for tac and toh

5. If clock rising time is longer than 1 ns, a time (t_T/2 -0.5) ns has to be added to this parameter.
6. Rated at 1.5V
7. If t_T is longer than 1 ns, a time (t_T -1) ns has to be added to this parameter.
8. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
11. t_{DAL} is equivalent to t_{DPL} + t_{RP}.

Package Diagram

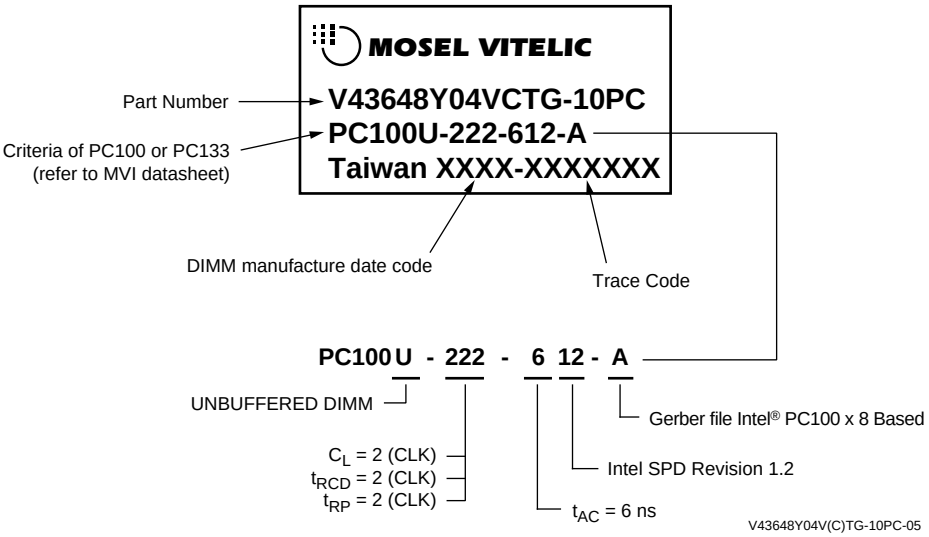
144 Pin SODIMM



NOTE:
1. All dimensions in inches.
   Tolerances ±0.005 unless otherwise specified.

V43648Y04V(C)TG-10PC-04

Label Information



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