

## V850E/MS2™ 32-BIT SINGLE-CHIP MICROCONTROLLER

The  $\mu$ PD703130 is a member of the V850 Family™ of 32-bit single-chip microcontrollers designed for real-time control operations. These microcontrollers provide on-chip features, including a 32-bit CPU, RAM, interrupt controller, real-time pulse unit, serial interface, A/D converter, and DMA controller.

The  $\mu$ PD703130 is a ROMless version product.

**Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.**

**V850E/MS2 User's Manual Hardware: U14985E**

**V850E/MS1™ User's Manual Architecture: U12197E**

### FEATURES

- Number of instructions: 81
- Minimum instruction execution time 30 ns (@ 33 MHz operation)
- General-purpose registers 32 bits  $\times$  32
- Instruction set suitable for control applications
- Internal memory ROM: None  
RAM: 4 KB
- Advanced on-chip interrupt controller
- Real-time pulse unit suitable for control operations
- Powerful serial interface (on-chip dedicated baud rate generator)
- On-chip clock generator
- 10-bit resolution A/D converter: 4 channels
- DMA controller: 4 channels
- Power saving functions

### APPLICATIONS

- Optical storage equipment (DVD players, etc.)
- System control for digital consumer equipment, etc.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

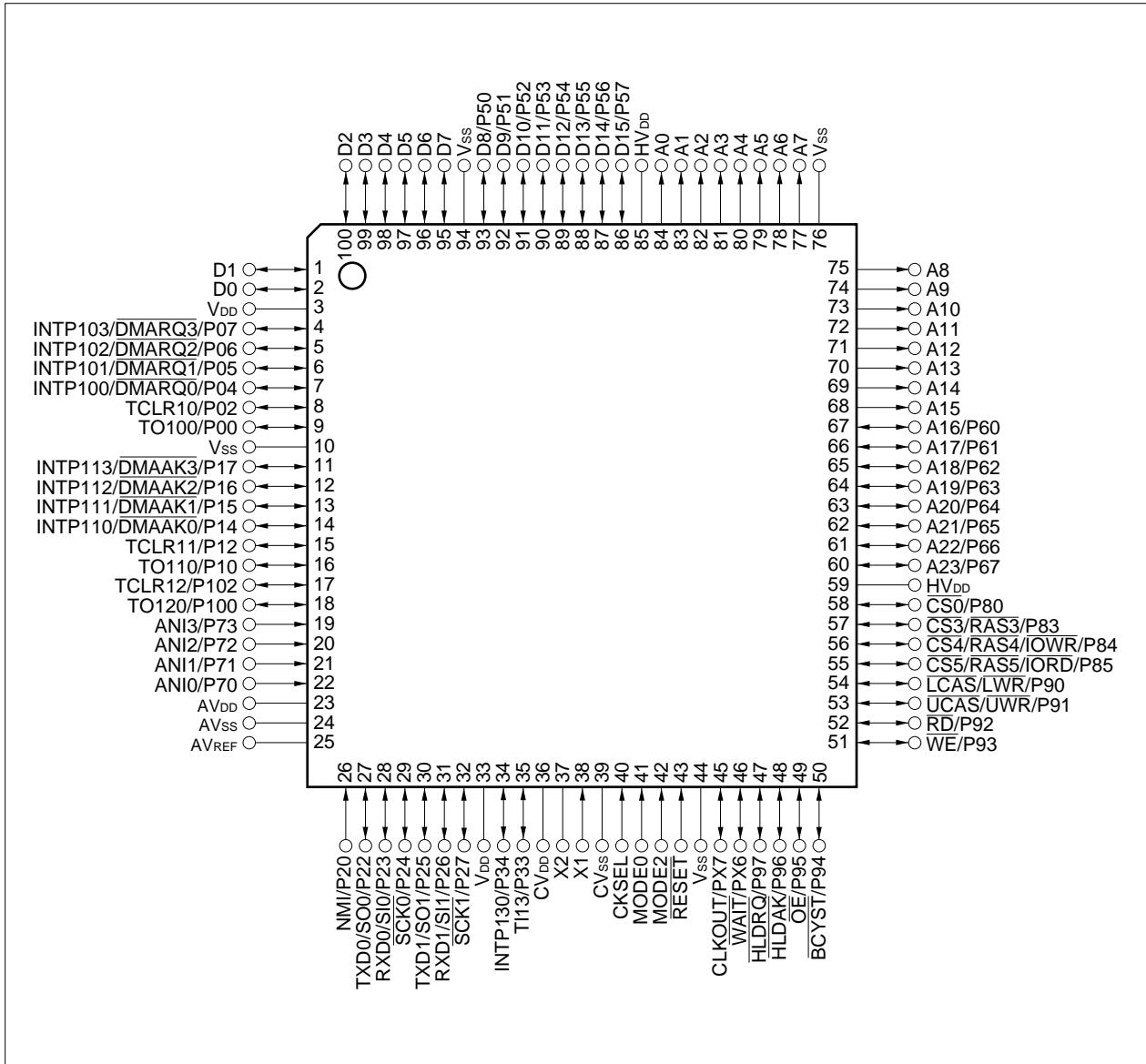
ORDERING INFORMATION

Part Number	Package	Maximum Operating Frequency	Internal ROM
μPD703130GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	33 MHz	None

PIN CONFIGURATION (TOP VIEW)

100-pin plastic LQFP (fine pitch) (14 × 14)

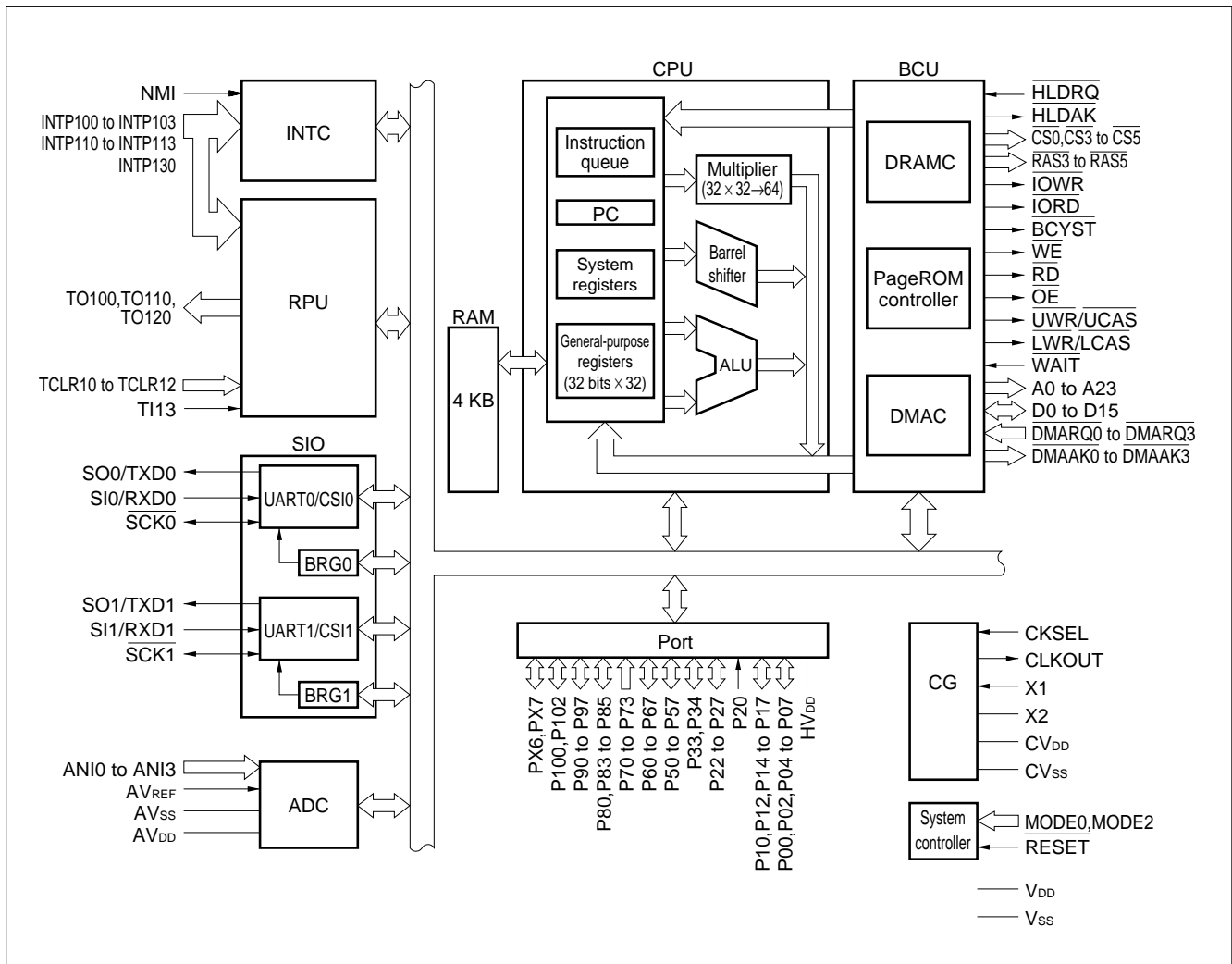
- μPD703130GC-8EU



## PIN NAMES

A0 to A23:	Address bus	P20, P22 to P27:	Port 2
ANI0 to ANI3:	Analog input	P33, P34:	Port 3
AV <sub>DD</sub> :	Analog power supply	P50 to P57:	Port 5
AV <sub>REF</sub> :	Analog reference voltage	P60 to P67:	Port 6
AV <sub>SS</sub> :	Analog ground	P70 to P73:	Port 7
$\overline{\text{BCYST}}$ :	Bus cycle start timing	P80, P83 to P85:	Port 8
CKSEL:	Clock generator operating mode select	P90 to P97:	Port 9
CLKOUT:	Clock output	P100, P102:	Port 10
$\overline{\text{CS0}}$ , $\overline{\text{CS3}}$ to $\overline{\text{CS5}}$ :	Chip select	PX6, PX7:	Port X
CV <sub>DD</sub> :	Clock generator power supply	$\overline{\text{RAS3}}$ to $\overline{\text{RAS5}}$ :	Row address strobe
CV <sub>SS</sub> :	Clock generator ground	$\overline{\text{RD}}$ :	Read
D0 to D15:	Data bus	$\overline{\text{RESET}}$ :	Reset
$\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK3}}$ :	DMA acknowledge	RXD0, RXD1:	Receive data
$\overline{\text{DMARQ0}}$ to $\overline{\text{DMARQ3}}$ :	DMA request	$\overline{\text{SCK0}}$ , $\overline{\text{SCK1}}$ :	Serial clock
$\overline{\text{HLDK}}$ :	Hold acknowledge	SI0, SI1:	Serial input
$\overline{\text{HLDRQ}}$ :	Hold request	SO0, SO1:	Serial output
HV <sub>DD</sub> :	Power supply for external pins	TCLR10 to TCLR12:	Timer clear
INTP100 to INTP103, :	Interrupt request from peripherals	TI13:	Timer input
INTP110 to INTP113, INTP130		TO100, TO110:	Timer output
$\overline{\text{IORD}}$ :	I/O read strobe	TO120	
$\overline{\text{IOWR}}$ :	I/O write strobe	TXD0, TXD1:	Transmit data
$\overline{\text{LCAS}}$ :	Lower column address strobe	$\overline{\text{UCAS}}$ :	Upper column address strobe
$\overline{\text{LWR}}$ :	Lower write strobe	$\overline{\text{UWR}}$ :	Upper write strobe
MODE0, MODE2:	Mode	V <sub>DD</sub> :	Power supply for internal unit
NMI:	Non-maskable interrupt request	V <sub>SS</sub> :	Ground
$\overline{\text{OE}}$ :	Output enable	$\overline{\text{WAIT}}$ :	Wait
P00, P02, P04 to P07:	Port 0	$\overline{\text{WE}}$ :	Write enable
P10, P12, P14 to P17:	Port 1	X1, X2:	Crystal

INTERNAL BLOCK DIAGRAM



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1. DIFFERENCES BETWEEN V850E/MS2 AND V850E/MS1

Product Name Item	V850E/MS2	V850E/MS1	
	μPD703130	μPD703100-33	μPD703102-33
Internal ROM	None	None	128 KB (mask ROM)
Maximum operating frequency	33 MHz	33 MHz	
Memory space	64 MB linear (only 22 MB supports on-chip $\overline{CS}$ signal)	64 MB linear	
Chip select output	4 spaces	8 spaces	
Interrupt function	External: 10, internal: 35	External: 25, internal: 47	
I/O lines	Input: 5, I/O: 52	Input: 9, I/O: 114	
Timer	16-bit timer/event counter: 4 channels 16-bit timer: 2 channels	16-bit timer/event counter: 6 channels 16-bit timer: 2 channels	
Serial interface	CSI/UART: 2 channels Dedicated baud rate generator: 2 channels	CSI: 2 channels CSI/UART: 2 channels Dedicated baud rate generator: 3 channels	
A/D converter	10-bit resolution × 4 channels	10-bit resolution × 8 channels	
Package	100-pin plastic LQFP (fine-pitch) (14 × 14)	144-pin plastic LQFP (fine-pitch) (20 × 20)	
Other	Noise tolerance and noise radiation will differ due to differences in circuit scale and mask layout.		

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 6-bit I/O port Input/output can be specified in 1-bit units.	TO100
P02			TCLR10
P04			INTP100/DMARQ0
P05			INTP101/DMARQ1
P06			INTP102/DMARQ2
P07			INTP103/DMARQ3
P10			I/O
P12	TCLR11		
P14	INTP110/DMAAK0		
P15	INTP111/DMAAK1		
P16	INTP112/DMAAK2		
P17	INTP113/DMAAK3		
P20	Input	Port 2 P20 is an input only port. When a valid edge is input, this pin operates as NMI input. Also, bit 0 of the P2 register indicates the NMI input status. P22 to P27 are 6-bit I/O port. Input/output can be specified in 1-bit units.	
P22	I/O		TXD0/SO0
P23			RXD0/SI0
P24			SCK0
P25			TXD1/SO1
P26			RXD1/SI1
P27			SCK1
P33	I/O		Port 3 2-bit I/O port Input/output can be specified in 1-bit units.
P34		INTP130	
P50 to P57	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units.	D8 to D15
P60 to P67	I/O	Port 6 8-bit I/O port Input/output can be specified in 1-bit units.	A16 to A23
P70 to P73	Input	Port 7 4-bit input only port	ANI0 to ANI3
P80	I/O	Port 8 4-bit I/O port Input/output can be specified in 1-bit units.	CS0
P83			CS3/RAS3
P84			CS4/RAS4/IOWR
P85			CS5/RAS5/IORD

(2/2)

Pin Name	I/O	Function	Alternate Function
P90	I/O	Port 9 8-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{LCAS/LWR}}$
P91			$\overline{\text{UCAS/UWR}}$
P92			$\overline{\text{RD}}$
P93			$\overline{\text{WE}}$
P94			$\overline{\text{BCYST}}$
P95			$\overline{\text{OE}}$
P96			$\overline{\text{HLDK}}$
P97			$\overline{\text{HLDRQ}}$
P100	I/O	Port 10 2-bit I/O port Input/output can be specified in 1-bit units.	TO120
P102			TCLR12
PX6	I/O	Port X 2-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WAIT}}$
PX7			CLKOUT



2.2 Non-Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
TO100	Output	Pulse signal output for timers 10 to 12	P00
TO110			P10
TO120			P100
TCLR10	Input	External clear signal input for timers 10 to 12	P02
TCLR11			P12
TCLR12			P102
TI13	Input	External count clock input for timer 13	P33
INTP100	Input	External maskable interrupt request input, shared as external capture trigger input for timer 10	P04/ $\overline{\text{DMARQ0}}$
INTP101			P05/ $\overline{\text{DMARQ1}}$
INTP102			P06/ $\overline{\text{DMARQ2}}$
INTP103			P07/ $\overline{\text{DMARQ3}}$
INTP110	Input	External maskable interrupt request input, shared as external capture trigger input for timer 11	P14/ $\overline{\text{DMAAK0}}$
INTP111			P15/ $\overline{\text{DMAAK1}}$
INTP112			P16/ $\overline{\text{DMAAK2}}$
INTP113			P17/ $\overline{\text{DMAAK3}}$
INTP130	Input	External maskable interrupt request input, shared as external capture trigger input for timer 13	P34
SO0	Output	Serial transmit data output (3-wire) for CSI0 and CSI1	P22/TXD0
SO1			P25/TXD1
SI0	Input	Serial receive data input (3-wire) for CSI0 and CSI1	P23/RXD0
SI1			P26/RXD1
$\overline{\text{SCK0}}$	I/O	Serial clock I/O (3-wire) for CSI0 and CSI1	P24
$\overline{\text{SCK1}}$			P27
TXD0	Output	Serial transmit data output for UART0 and UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input for UART0 and UART1	P23/SI0
RXD1			P26/SI1
D0 to D7	I/O	16-bit data bus for external memory	–
D8 to D15			P50 to P57
A0 to A15	Output	24-bit address bus for external memory	–
A16 to A23			P60 to P67
$\overline{\text{LWR}}$	Output	Lower byte write-enable signal output for external data bus	P90/ $\overline{\text{LCAS}}$
$\overline{\text{UWR}}$	Output	Higher byte write-enable signal output for external data bus	P91/ $\overline{\text{UCAS}}$
$\overline{\text{RD}}$	Output	Read strobe signal output for external data bus	P92
$\overline{\text{WE}}$	Output	Write enable signal output for DRAM	P93
$\overline{\text{OE}}$	Output	Output enable signal output for DRAM	P95

(2/2)

Pin Name	I/O	Function	Alternate Function
$\overline{\text{LCAS}}$	Output	Column address strobe signal output for DRAM's lower data	P90/ $\overline{\text{LWR}}$
$\overline{\text{UCAS}}$	Output	Column address strobe signal output for DRAM's higher data	P91/ $\overline{\text{UWR}}$
$\overline{\text{RAS3}}$	Output	Row address strobe signal output for DRAM	P83/ $\overline{\text{CS3}}$
$\overline{\text{RAS4}}$			P84/ $\overline{\text{CS4/IOWR}}$
$\overline{\text{RAS5}}$			P85/ $\overline{\text{CS5/IORD}}$
$\overline{\text{BCYST}}$	Output	Strobe signal output indicating start of bus cycle	P94
$\overline{\text{CS0}}$	Output	Chip select signal output	P80
$\overline{\text{CS3}}$			P83/ $\overline{\text{RAS3}}$
$\overline{\text{CS4}}$			P84/ $\overline{\text{RAS4/IOWR}}$
$\overline{\text{CS5}}$			P85/ $\overline{\text{RAS5/IORD}}$
$\overline{\text{WAIT}}$	Input	Control signal input for inserting waits in bus cycle	PX6
$\overline{\text{IOWR}}$	Output	DMA write strobe signal output	P84/ $\overline{\text{RAS4/CS4}}$
$\overline{\text{IORD}}$	Output	DMA read strobe signal output	P85/ $\overline{\text{RAS5/CS5}}$
$\overline{\text{DMARQ0}}$ to $\overline{\text{DMARQ3}}$	Input	DMA request signal input	P04/ $\overline{\text{INTP100}}$ to P07/ $\overline{\text{INTP103}}$
$\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK3}}$	Output	DMA acknowledge signal output	P14/ $\overline{\text{INTP110}}$ to P17/ $\overline{\text{INTP113}}$
$\overline{\text{HLDK}}$	Output	Bus hold acknowledge output	P96
$\overline{\text{HLDRQ}}$	Input	Bus hold request input	P97
ANI0 to ANI3	Input	Analog input to A/D converter	P70 to P73
NMI	Input	Non-maskable interrupt request input	P20
CLKOUT	Output	System clock output	PX7
CKSEL	Input	Input for specifying clock generator's operation mode	–
MODE0, MODE2	Input	Specify operation modes	–
$\overline{\text{RESET}}$	Input	System reset input	–
X1	Input	Connecting resonator for system clock. Input is via X1 when using an external clock.	–
X2	–		–
$\text{AV}_{\text{REF}}$	Input	Reference voltage input for A/D converter	–
$\text{AV}_{\text{DD}}$	–	Positive power supply for A/D converter	–
$\text{AV}_{\text{SS}}$	–	Ground potential for A/D converter	–
$\text{CV}_{\text{DD}}$	–	Positive power supply for dedicated clock generator	–
$\text{CV}_{\text{SS}}$	–	Ground potential for dedicated clock generator	–
$\text{V}_{\text{DD}}$	–	Positive power supply (power supply for internal units)	–
$\text{HV}_{\text{DD}}$	–	Positive power supply (power supply for external pins)	–
$\text{V}_{\text{SS}}$	–	Ground potential	–

**2.3 Pin I/O Circuits and Recommended Connection of Unused Pins**

Table 2-1 shows the I/O circuit type of each pin and recommended connection of unused pins. Figure 2-1 shows the various circuit types using partially abridged diagrams.

When connecting to V<sub>DD</sub> or V<sub>SS</sub> via a resistor, a resistance value in the range of 1 to 10 kΩ is recommended.

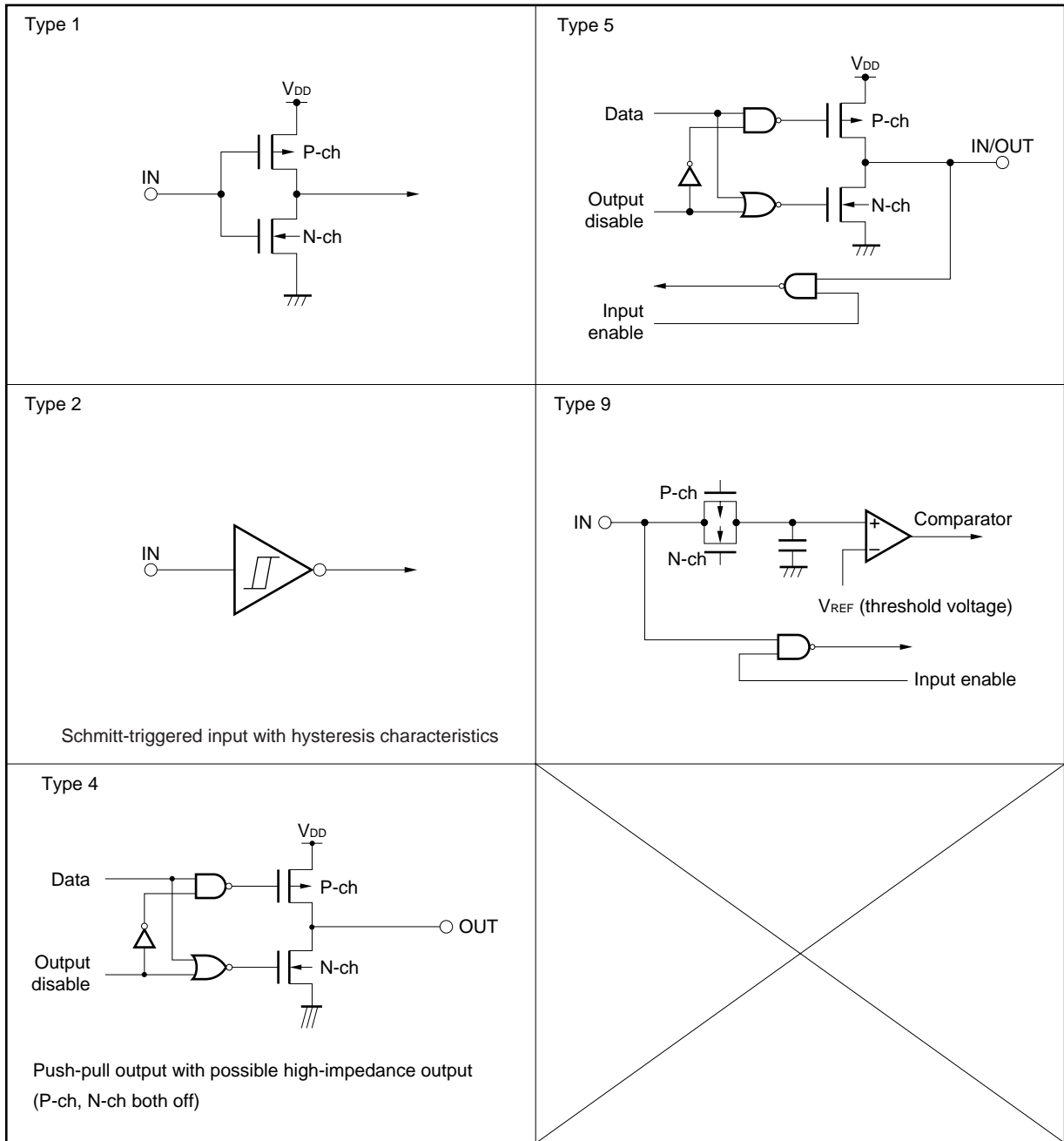
**Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (1/2)**

Pin	I/O Circuit Type	Recommended Connection of Unused Pins
P00/TO100	5	Input: Independently connect to HV <sub>DD</sub> or V <sub>SS</sub> via a resistor Output: Leave open
P02/TCLR10		
P04/INTP100/DMARQ0 to P07/INTP103/DMARQ3		
P10/TO110		
P12/TCLR11		
P14/INTP110/DMAAK0 to P17/INTP113/DMAAK3		
P20/NMI	2	Connect directly to V <sub>SS</sub>
P22/TXD0/SO0	5	Input: Independently connect to HV <sub>DD</sub> or V <sub>SS</sub> via a resistor Output: Leave open
P23/RXD0/SI0		
P24/SCK0		
P25/TXD1/SO1		
P26/RXD1/SI1		
P27/SCK1		
P33/TI13		
P34/INTP130		
P50/D8 to P57/D15		
P60/A16 to P67/A23		
P70/ANI0 to P73/ANI3		
P80/CS0, to P83/CS3/RAS3	5	Input: Independently connect to HV <sub>DD</sub> or V <sub>SS</sub> via a resistor Output: Leave open
P84/CS4/RAS4/IOWR, P85/CS5/RAS5/IORD		
P90/LCAS/LWR		
P91/UCAS/UWR		
P92/RD		
P93/WE		
P94/BCYST		
P95/OE		
P96/HLDAK		
P97/HLDRQ		
P100/TO120		
P102/TCLR12		

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (2/2)

Pin	I/O Circuit Type	Recommended Connection of Unused Pins
PX6/ $\overline{\text{WAIT}}$	5	Input: Independently connect to $\text{HV}_{\text{DD}}$ or $\text{V}_{\text{SS}}$ via a resistor Output: Leave open
PX7/CLKOUT		
A0 to A15	4	-
D0 to D7	5	
CKSEL	1	
$\overline{\text{RESET}}$	2	
MODE0, MODE2		
$\text{AV}_{\text{REF}}$ , $\text{AV}_{\text{SS}}$	-	Connect directly to $\text{V}_{\text{SS}}$
$\text{AV}_{\text{DD}}$	-	Connect directly to $\text{HV}_{\text{DD}}$

Figure 2-1. Pin I/O Circuits



**Caution** Replace  $V_{DD}$  by  $HV_{DD}$  when referencing the circuit diagrams shown above.

3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (TA = 25°C)

Parameter	Symbol	Condition	Rating	Unit	
Power supply voltage	V <sub>DD</sub>	V <sub>DD</sub> pin	-0.5 to +4.6	V	
	HV <sub>DD</sub>	HV <sub>DD</sub> pin, HV <sub>DD</sub> ≥ V <sub>DD</sub>	-0.5 to +7.0	V	
	CV <sub>DD</sub>	CV <sub>DD</sub> pin	-0.5 to +4.6	V	
	CV <sub>SS</sub>	CV <sub>SS</sub> pin	-0.5 to +0.5	V	
	AV <sub>DD</sub>	AV <sub>DD</sub> pin	-0.5 to HV <sub>DD</sub> + 0.5 <sup>Note</sup>	V	
	AV <sub>SS</sub>	AV <sub>SS</sub> pin	-0.5 to +0.5	V	
Input voltage	V <sub>I</sub>	Except X1 pin	-0.5 to HV <sub>DD</sub> + 0.5 <sup>Note</sup>	V	
Clock input voltage	V <sub>K</sub>	X1, V <sub>DD</sub> = 3.0 to 3.6 V	-0.5 to V <sub>DD</sub> + 1.0 <sup>Note</sup>	V	
Output current, low	I <sub>OL</sub>	1 pin	4.0	mA	
		Total of all pins	100	mA	
Output current, high	I <sub>OH</sub>	1 pin	-4.0	mA	
		Total of all pins	-100	mA	
Output voltage	V <sub>O</sub>	HV <sub>DD</sub> = 5.0 V ±10%	-0.5 to HV <sub>DD</sub> + 0.5 <sup>Note</sup>	V	
Analog input voltage	V <sub>IAN</sub>	P70/ANI0 to P73 pins	AV <sub>DD</sub> > HV <sub>DD</sub>	-0.5 to HV <sub>DD</sub> + 0.5 <sup>Note</sup>	V
			HV <sub>DD</sub> ≥ AV <sub>DD</sub>	-0.5 to AV <sub>DD</sub> + 0.5 <sup>Note</sup>	V
A/D converter reference input voltage	AV <sub>REF</sub>	AV <sub>DD</sub> > HV <sub>DD</sub>	-0.5 to HV <sub>DD</sub> + 0.5 <sup>Note</sup>	V	
		HV <sub>DD</sub> ≥ AV <sub>DD</sub>	-0.5 to AV <sub>DD</sub> + 0.5 <sup>Note</sup>	V	
Operating ambient temperature	T <sub>A</sub>		-40 to +85	°C	
Storage temperature	T <sub>stg</sub>		-60 to +150	°C	

**Note** Be sure not to exceed the absolute maximum ratings (MAX. value) of the each power supply voltage.

- Cautions**
1. Do not make direct connections of the output (or input/output) pins of the IC product with each other, and also avoid direct connections to V<sub>DD</sub>, V<sub>CC</sub>, or GND. However, the open drain pins or the open collector pins can be directly connected to each other. A direct connection can also be made for an external circuit designed with timing specifications that prevent conflicting output from pins subject to a high-impedance state.
  2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

**Capacitance (T<sub>A</sub> = 25°C, V<sub>DD</sub> = HV<sub>DD</sub> = CV<sub>DD</sub> = V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I</sub>	f <sub>c</sub> = 1 MHz Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C <sub>IO</sub>				15	pF
Output capacitance	C <sub>O</sub>				15	pF

**Operating Conditions**

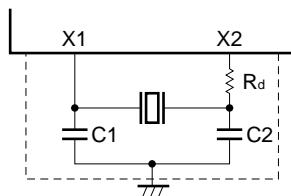
Operation Mode	Internal Operating Clock Frequency (f <sub>x</sub> )	Operating Ambient Temperature (T <sub>A</sub> )	Power Supply Voltage (V <sub>DD</sub> , HV <sub>DD</sub> )
Direct mode	10 to 33 MHz <sup>Note 1</sup>	-40 to +85°C	V <sub>DD</sub> = 3.0 to 3.6 V, HV <sub>DD</sub> = 5.0 V ±10%
PLL mode <sup>Note 2</sup>	20 to 33 MHz <sup>Note 3</sup>	-40 to +85°C	

- Notes**
1. Set the input clock frequency used in direct mode to 20 to 66 MHz.
  2. The internal operating clock frequency in PLL mode is the value for 5× operation. When used for 1× or 1/2× operation as set by the CKDIV<sub>n</sub> (n = 0, 1) bit of the CKC register, operation at a frequency of 20 MHz or less is possible.
  3. Set the input clock frequency used in PLL mode to 4.0 to 6.6 MHz.

**Recommended Oscillator**

**(a) Ceramic resonator**

**(i) Murata Mfg. Co., Ltd. (T<sub>A</sub> = -40 to +85°C)**



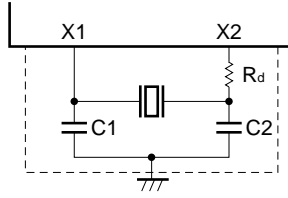
Manu- facturer	Part Number	Oscillation Frequency f <sub>xx</sub> (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T <sub>OST</sub> (ms)
			C1 (pF)	C2 (pF)	R <sub>d</sub> (kΩ)	MIN. (V)	MAX. (V)	
Murata Mfg.	CSTS400MG06 <sup>Note</sup> (CSTLS4M00G56-B0)	4.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTCR4M00G55-R0	4.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTS0500MG06 <sup>Note</sup> (CSTLS5M00G56-B0)	5.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTCR5M00G55-R0	5.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTS066MG06 <sup>Note</sup> (CSTLS6M60G56-B0)	6.6	On-chip	On-chip	0	3.0	3.6	0.6
	CSTCR6M60G55-R0	6.6	On-chip	On-chip	0	3.0	3.6	0.6

**Note** The part number will be changed to the part number in the parentheses from June 2001.

- Cautions**
1. Connect the oscillator as close to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area enclosed by broken lines.
  3. Sufficiently evaluate the matching between the μPD703130 and the resonator.



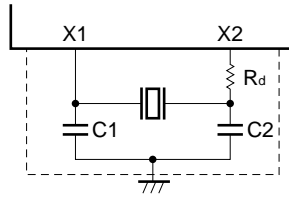
(ii) TDK (T<sub>A</sub> = -40 to +85°C)



Manu- facturer	Part Number	Oscillation Frequency f <sub>xx</sub> (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T <sub>OST</sub> (ms)
			C1 (pF)	C2 (pF)	R <sub>d</sub> (kΩ)	MIN. (V)	MAX. (V)	
TDK	FCR4.0MC5	4.0	On-chip	On-chip	0	3.0	3.6	0.73
	FCR5.0MC5	5.0	On-chip	On-chip	0	3.0	3.6	0.68
	FCR6.0MC5	6.0	On-chip	On-chip	0	3.0	3.6	0.58

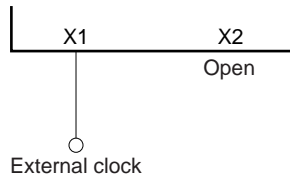
- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area enclosed by broken lines.
  3. Sufficiently evaluate the matching between the μPD703130 and the resonator.

(iii) Kyocera Corporation (T<sub>A</sub> = -20 to +80°C)



Type	Part Number	Oscillation Frequency f <sub>xx</sub> (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T <sub>OST</sub> (ms)
			C1 (pF)	C2 (pF)	R <sub>d</sub> (kΩ)	MIN. (V)	MAX. (V)	
Lead	KBR-4.0MKC	4.0	On-chip	On-chip	0	3.0	3.6	0.80
	KBR-5.0MKC	5.0	On-chip	On-chip	0	3.0	3.6	0.70
	KBR-6.0MKC	6.0	On-chip	On-chip	0	3.0	3.6	0.76
SMD	PBRC4.00HR	4.0	On-chip	On-chip	0	3.0	3.6	0.80
	PBRC5.00HR	5.0	On-chip	On-chip	0	3.0	3.6	0.70
	PBRC6.00HR	6.0	On-chip	On-chip	0	3.0	3.6	0.76

- Cautions**
1. Connect the oscillator as close to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area enclosed by broken lines.
  3. Sufficiently evaluate the matching between the μPD703130 and the resonator.

**(b) External clock input ( $T_A = -40$  to  $+85^\circ\text{C}$ )**

**Caution** Input CMOS-level voltage to the X1 pin.

DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = CV<sub>DD</sub> = 3.0 to 3.6 V, HV<sub>DD</sub> = 5.0 ±10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V <sub>IH</sub>	Except <b>Note 1</b>	2.2		HV <sub>DD</sub> + 0.3	V	
		<b>Note 1</b>	0.8HV <sub>DD</sub>		HV <sub>DD</sub> + 0.3	V	
Input voltage, low	V <sub>IL</sub>	Except <b>Note 1</b> and <b>Note 2</b>	-0.5		+0.8	V	
		<b>Note 1</b>	-0.5		0.2HV <sub>DD</sub>	V	
Clock input voltage, high	V <sub>XH</sub>	X1 pin	0.8V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V	
Clock input voltage, low	V <sub>XL</sub>	X1 pin	-0.3		0.15V <sub>DD</sub>	V	
Schmitt-triggered input threshold voltage	HV <sub>T</sub> <sup>+</sup>	<b>Note 1</b> , rising edge		3.0		V	
	HV <sub>T</sub> <sup>-</sup>	<b>Note 1</b> , falling edge		2.0		V	
Output voltage, high	V <sub>OH</sub>	I <sub>OH</sub> = -2.5 mA	0.7HV <sub>DD</sub>			V	
		I <sub>OH</sub> = -100 μA	HV <sub>DD</sub> - 0.4			V	
Output voltage, low	V <sub>OL</sub>	I <sub>OL</sub> = 2.5 mA			0.45	V	
Input leakage current, high	I <sub>LIH</sub>	V <sub>I</sub> = HV <sub>DD</sub> , except <b>Note 2</b>			10	μA	
Input leakage current, low	I <sub>LIL</sub>	V <sub>I</sub> = 0 V, except <b>Note 2</b>			-10	μA	
Output leakage current, high	I <sub>LOH</sub>	V <sub>O</sub> = HV <sub>DD</sub>			10	μA	
Output leakage current, low	I <sub>LOL</sub>	V <sub>O</sub> = 0 V			-10	μA	
Power supply current	Normal mode	I <sub>DD1</sub>	V <sub>DD</sub> + CV <sub>DD</sub>		2.0 × f <sub>x</sub>	3.0 × f <sub>x</sub>	mA
			HV <sub>DD</sub>		1.5 × f <sub>x</sub>	2.5 × f <sub>x</sub>	mA
	HALT mode	I <sub>DD2</sub>	V <sub>DD</sub> + CV <sub>DD</sub>		1.4 × f <sub>x</sub>	1.8 × f <sub>x</sub>	mA
			HV <sub>DD</sub>		0.7 × f <sub>x</sub>	1.2 × f <sub>x</sub>	mA
	IDLE mode	I <sub>DD3</sub>	V <sub>DD</sub> + CV <sub>DD</sub>		1.4	2.5	mA
			HV <sub>DD</sub>		20	100	μA
STOP mode	I <sub>DD4</sub>	V <sub>DD</sub> + CV <sub>DD</sub>		20	100	μA	
		HV <sub>DD</sub>		10	50	μA	

**Notes** 1. P20/NMI, MODE0, MODE2, CKSEL, RESET

2. When the P70/ANI0 to P73/ANI3 pins are used as analog input.

**Remarks** 1. TYP. values are reference values for when T<sub>A</sub> = 25°C, V<sub>DD</sub> = CV<sub>DD</sub> = 3.3 V, and HV<sub>DD</sub> = 5.0 V.

2. Direct mode: f<sub>x</sub> = 10 to 33 MHz

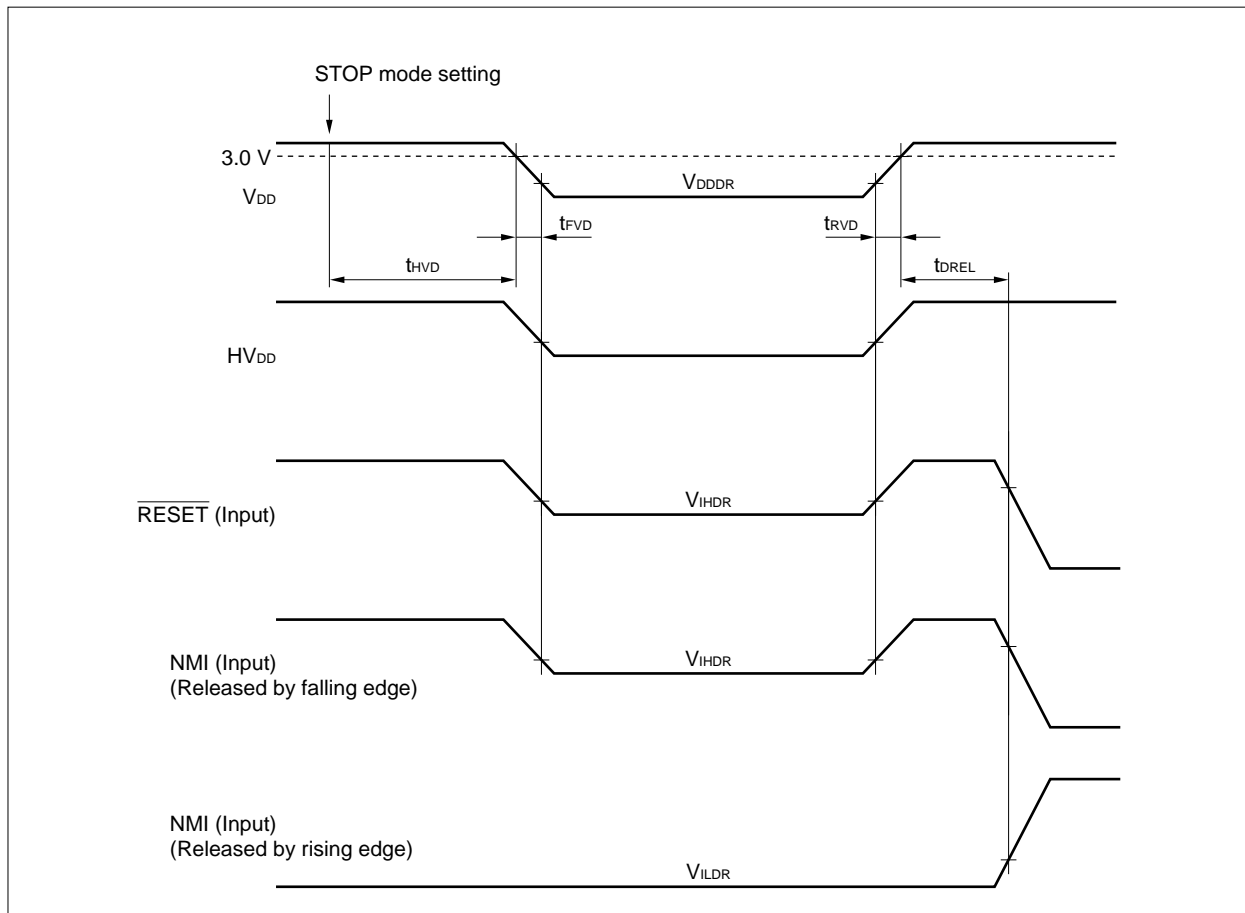
PLL mode: f<sub>x</sub> = 20 to 33 MHz

3. The unit for f<sub>x</sub> is MHz.

Data Hold Characteristics (T<sub>A</sub> = -40 to +85°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data hold voltage	V <sub>DDDR</sub>	STOP mode, V <sub>DD</sub> = V <sub>DDDR</sub>	1.5		3.6	V
	HV <sub>DDDR</sub>	STOP mode, HV <sub>DD</sub> = HV <sub>DDDR</sub>	V <sub>DDDR</sub>		5.5	V
Data hold current	I <sub>DDDR</sub>	V <sub>DD</sub> = V <sub>DDDR</sub>		30	150	μA
Power supply voltage rise time	t <sub>RV</sub>		200			μs
Power supply voltage fall time	t <sub>FV</sub>		200			μs
Power supply voltage hold time (from STOP mode setting)	t <sub>HV</sub>		0			ms
STOP mode release signal input time	t <sub>DREL</sub>		0			ns
Data hold input voltage, high	V <sub>IHDR</sub>	P20/NMI, MODE0, MODE2, CKSEL, RESET	0.8HV <sub>DDDR</sub>		HV <sub>DDDR</sub>	V
Data hold input voltage, low	V <sub>ILDR</sub>	P20/NMI, MODE0, MODE2, CKSEL, RESET	0		0.2HV <sub>DDDR</sub>	V

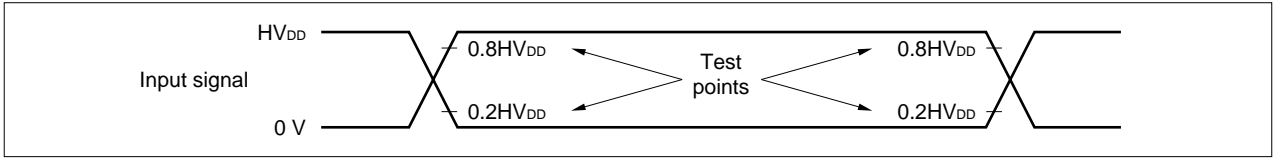
**Remark** TYP. values are reference values for when T<sub>A</sub> = 25°C.



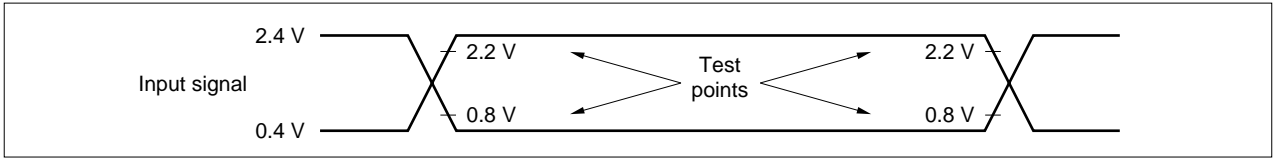
**AC Characteristics** ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = CV_{DD} = 3.0$  to  $3.6$  V,  $HV_{DD} = 5.0 \pm 10\%$ ,  $V_{SS} = 0$  V, output pin load capacitance:  $C_L = 50$  pF)

**AC Test Input Test Points**

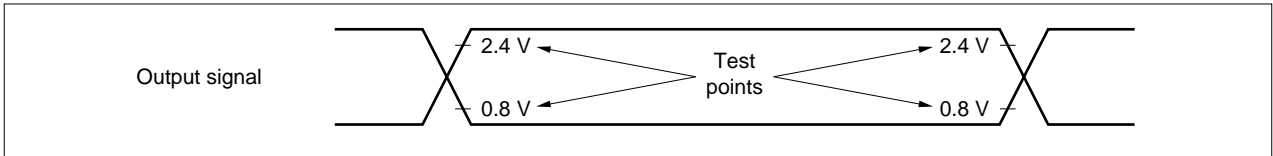
(a) P20/NMI, MODE0, MODE2, CKSEL,  $\overline{\text{RESET}}$



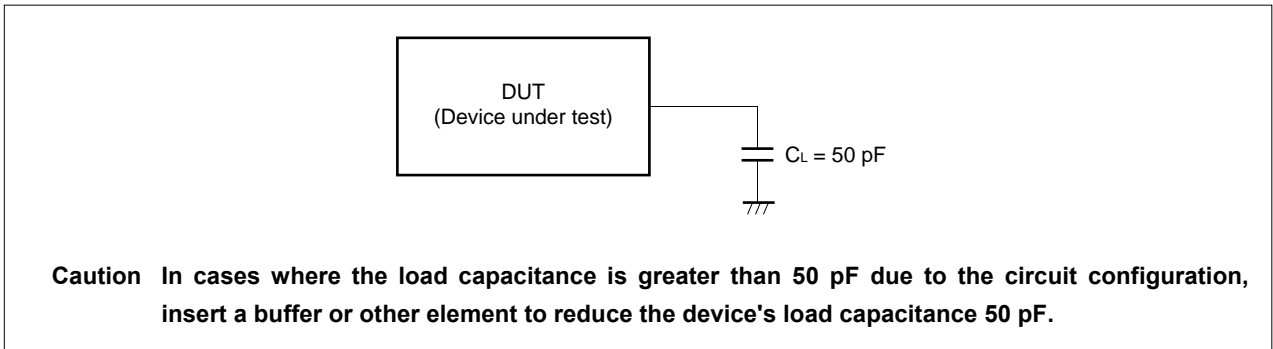
(b) Pins other than those listed in (a) above



**AC Test Output Test Points**



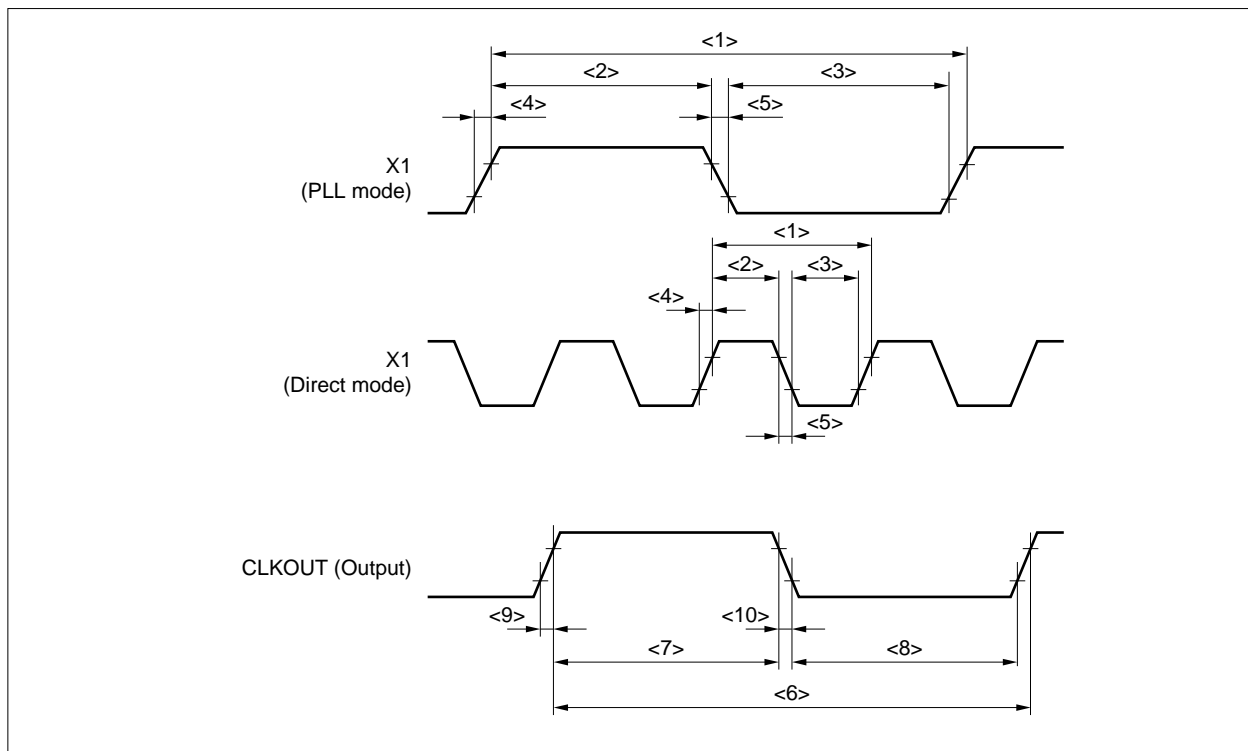
**Load Condition**



(1) Clock timing

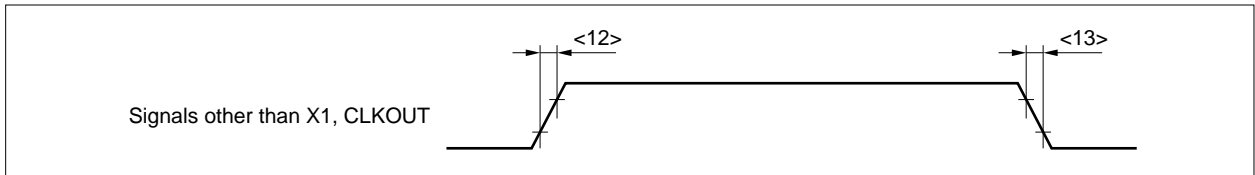
Parameter	Symbol	Condition	MIN.	MAX.	Unit	
X1 input cycle	<1>	$t_{CYX}$	Direct mode	15	50	ns
			PLL mode	150	250	ns
X1 input high-level width	<2>	$t_{WXH}$	Direct mode	5		ns
			PLL mode	50		ns
X1 input low-level width	<3>	$t_{WXL}$	Direct mode	5		ns
			PLL mode	50		ns
X1 input rise time	<4>	$t_{XR}$	Direct mode		4	ns
			PLL mode		10	ns
X1 input fall time	<5>	$t_{XF}$	Direct mode		4	ns
			PLL mode		10	ns
CLKOUT output cycle	<6>	$t_{CYK}$	30	100	ns	
CLKOUT high-level width	<7>	$t_{WKH}$	$0.5T - 7$		ns	
CLKOUT low-level width	<8>	$t_{WKL}$	$0.5T - 4$		ns	
CLKOUT rise time	<9>	$t_{KR}$		5	ns	
CLKOUT fall time	<10>	$t_{KF}$		5	ns	

Remark T =  $t_{CYK}$



(2) Output waveform (other than X1, CLKOUT)

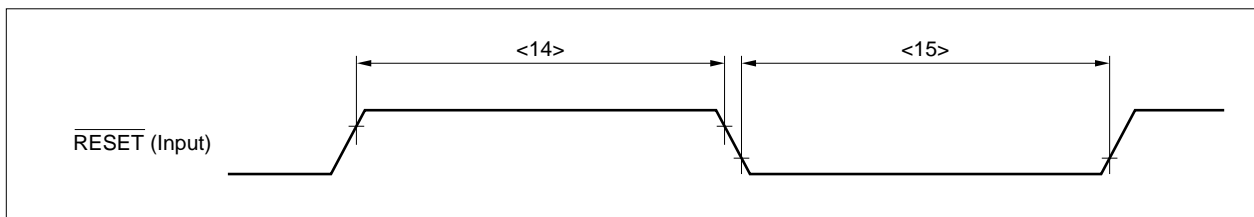
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<12>	t <sub>OR</sub>			10	ns
Output fall time	<13>	t <sub>OF</sub>			10	ns



(3) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	<14>	t <sub>WRSH</sub>		500		ns
$\overline{\text{RESET}}$ low-level width	<15>	t <sub>WRSL</sub>	When power supply is on, and STOP mode has been released	500 + T <sub>OS</sub>		ns
			Other than when power supply is on, and STOP mode has been released	500		ns

**Remark** T<sub>OS</sub>: Oscillation stabilization time



(4) SRAM, external ROM, or external I/O access timing

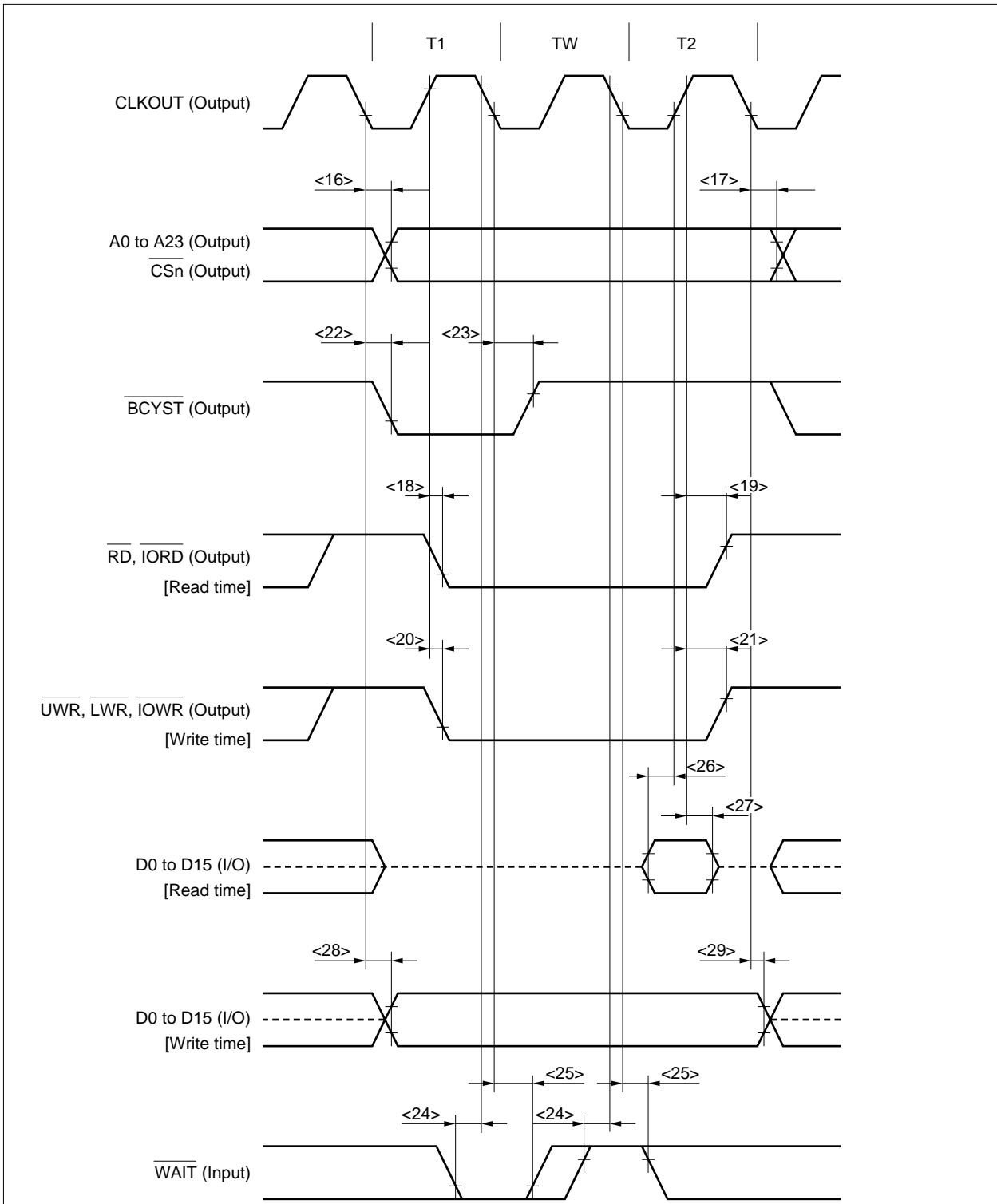
(a) Access timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address, $\overline{CSn}$ output delay time (from CLKOUT ↓)	<16> $t_{DKA}$		2	10	ns
Address, $\overline{CSn}$ output hold time (from CLKOUT ↓)	<17> $t_{HKA}$		2	10	ns
$\overline{RD}$ , $\overline{IORD}$ ↓ delay time (from CLKOUT ↑)	<18> $t_{DKRDL}$		2	14	ns
$\overline{RD}$ , $\overline{IORD}$ ↑ delay time (from CLKOUT ↑)	<19> $t_{HKRDH}$		2	14	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↓ delay time (from CLKOUT ↑)	<20> $t_{DKWRL}$		2	10	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↑ delay time (from CLKOUT ↑)	<21> $t_{HKWRH}$		2	10	ns
$\overline{BCYST}$ ↓ delay time (from CLKOUT ↓)	<22> $t_{DKBSL}$		2	10	ns
$\overline{BCYST}$ ↑ delay time (from CLKOUT ↓)	<23> $t_{HKBSH}$		2	10	ns
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24> $t_{SWK}$		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25> $t_{HKW}$		2		ns
Data input setup time (to CLKOUT ↑)	<26> $t_{SKID}$		18		ns
Data input hold time (from CLKOUT ↑)	<27> $t_{HKID}$		2		ns
Data output delay time (from CLKOUT ↓)	<28> $t_{DKOD}$		2	10	ns
Data output hold time (from CLKOUT ↓)	<29> $t_{HKOD}$		2	10	ns

- Remarks**
1. Maintain at least one of the data input hold times  $t_{HKID}$  and  $t_{HRDID}$ .
  2.  $n = 0, 3$  to  $5$



(a) Access timing (SRAM, external ROM, or external I/O) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.
  2. The broken lines indicate high impedance.
  3. n = 0, 3 to 5

(b) Read timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data input setup time (to address)	<30>	t <sub>SAID</sub>		(1.5 + w <sub>D</sub> + w)T - 28	ns
Data input setup time (to $\overline{RD}$ )	<31>	t <sub>SRDID</sub>		(1 + w <sub>D</sub> + w)T - 32	ns
$\overline{RD}$ , $\overline{IORD}$ low-level width	<32>	t <sub>WRDL</sub>	(1 + w <sub>D</sub> + w)T - 10		ns
$\overline{RD}$ , $\overline{IORD}$ high-level width	<33>	t <sub>WRDH</sub>	T - 10		ns
Delay time from address, $\overline{CSn}$ to $\overline{RD}$ , $\overline{IORD} \downarrow$	<34>	t <sub>DARD</sub>	0.5T - 10		ns
Delay time from $\overline{RD}$ , $\overline{IORD} \uparrow$ to address	<35>	t <sub>ORDA</sub>	(0.5 + i)T - 10		ns
Data input hold time (from $\overline{RD}$ , $\overline{IORD} \uparrow$ )	<36>	t <sub>HRDID</sub>	0		ns
Delay time from $\overline{RD}$ , $\overline{IORD} \uparrow$ to data output	<37>	t <sub>DRDOD</sub>	(0.5 + i)T - 10		ns
$\overline{WAIT}$ setup time (to address)	<38>	t <sub>SAW</sub>	<b>Note</b>	T - 25	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST} \downarrow$ )	<39>	t <sub>SBSW</sub>	<b>Note</b>	T - 25	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST} \uparrow$ )	<40>	t <sub>HBSW</sub>	<b>Note</b>	0	ns

**Note** For first  $\overline{WAIT}$  sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

**Remarks** 1. T = t<sub>CYK</sub>

2. w: The number of waits due to  $\overline{WAIT}$ .

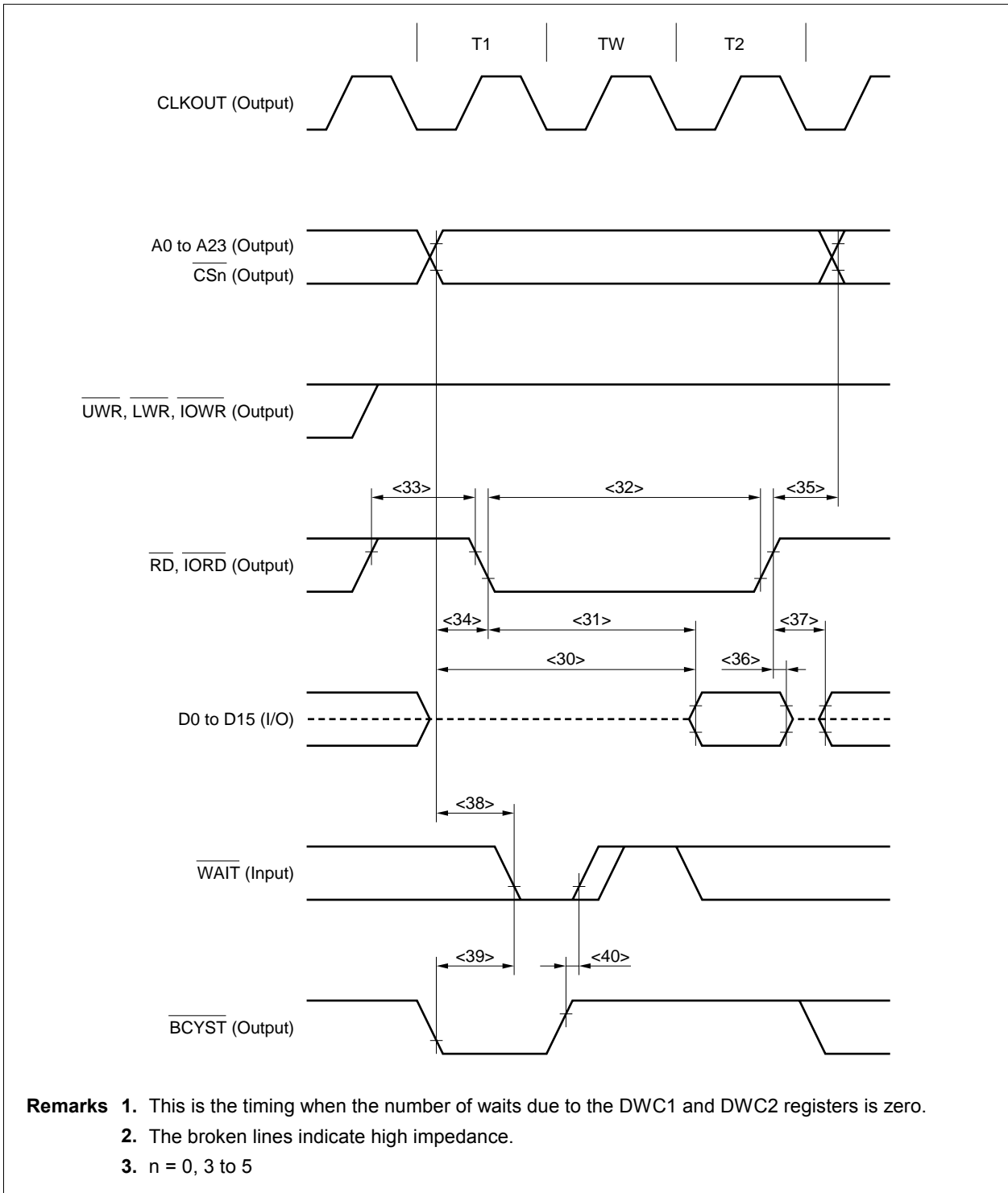
3. w<sub>D</sub>: The number of waits due to the DWC1 and DWC2 registers.

4. i: The number of idle states that are inserted when a write cycle follows a read cycle.

5. Maintain at least one of the data input hold times, t<sub>HKID</sub> or t<sub>HRDID</sub>.

6. n = 0, 3 to 5

(b) Read timing (SRAM, external ROM, or external I/O) (2/2)



## (c) Write timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to address)	<38> $t_{\text{SAW}}$	<b>Note</b>		$T - 25$	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}} \downarrow$ )	<39> $t_{\text{SBSW}}$	<b>Note</b>		$T - 25$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}} \uparrow$ )	<40> $t_{\text{HBSW}}$	<b>Note</b>	0		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}} \downarrow$	<41> $t_{\text{DAWR}}$		$0.5T - 10$		ns
Address setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}} \uparrow$ )	<42> $t_{\text{SAWR}}$		$(1.5 + \text{WD} + \text{w})T - 10$		ns
Delay time from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}} \uparrow$ to address	<43> $t_{\text{DWRA}}$		$0.5T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}$ high-level width	<44> $t_{\text{WWRH}}$		$T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}$ low-level width	<45> $t_{\text{WWRL}}$		$(1 + \text{WD} + \text{w})T - 10$		ns
Data output setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}} \uparrow$ )	<46> $t_{\text{SODWR}}$		$(1.5 + \text{WD} + \text{w})T - 10$		ns
Data output hold time (from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}} \uparrow$ )	<47> $t_{\text{HWROD}}$		$0.5T - 10$		ns

**Note** For first  $\overline{\text{WAIT}}$  sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

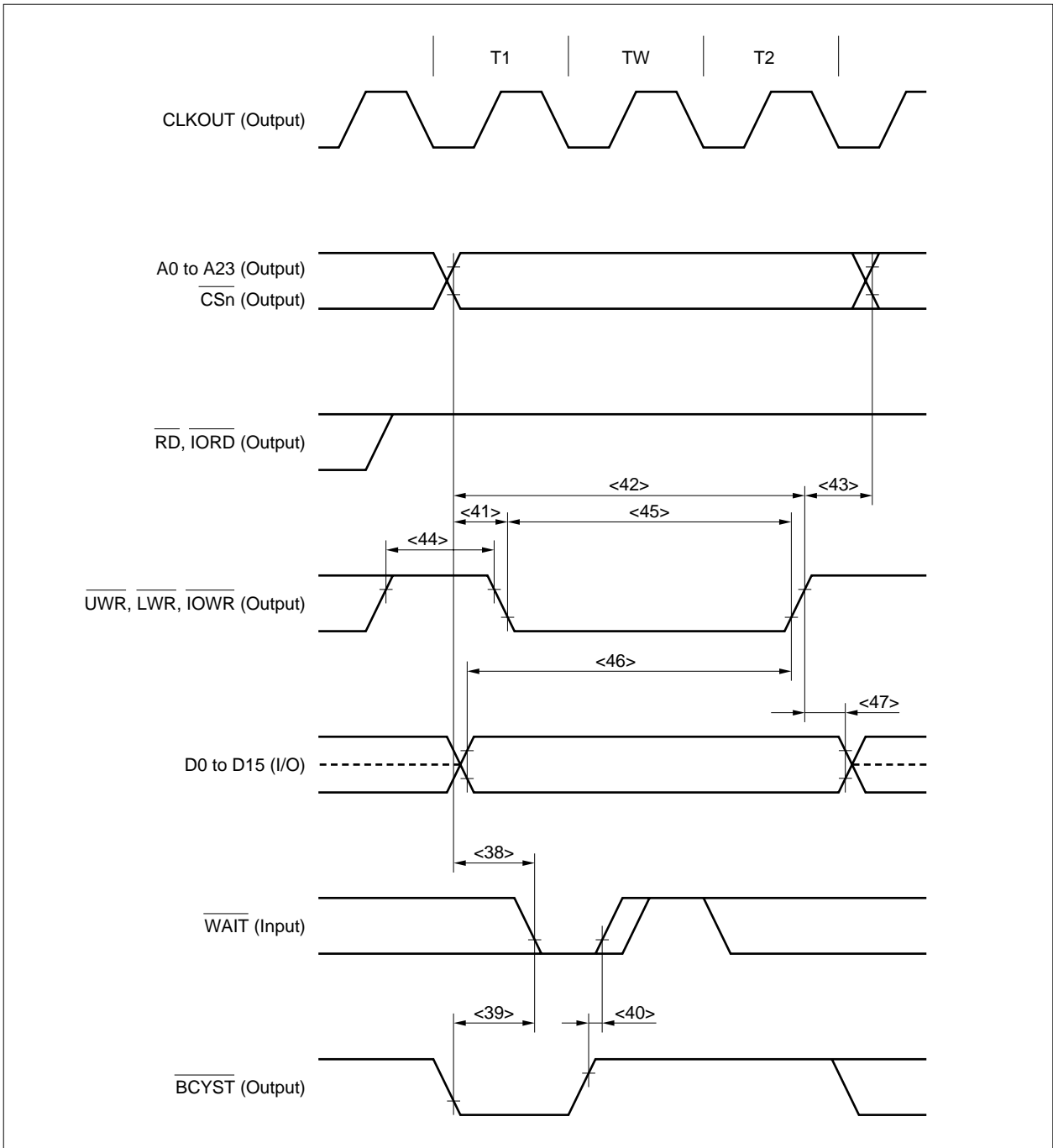
**Remarks** 1.  $T = t_{\text{CYK}}$

2.  $w$ : The number of waits due to  $\overline{\text{WAIT}}$ .

3.  $\text{WD}$ : The number of waits due to the DWC1 and DWC2 registers.

4.  $n = 0, 3$  to 5

(c) Write timing (SRAM, external ROM, or external I/O) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.
  2. The broken lines indicate high impedance.
  3. n = 0, 3 to 5

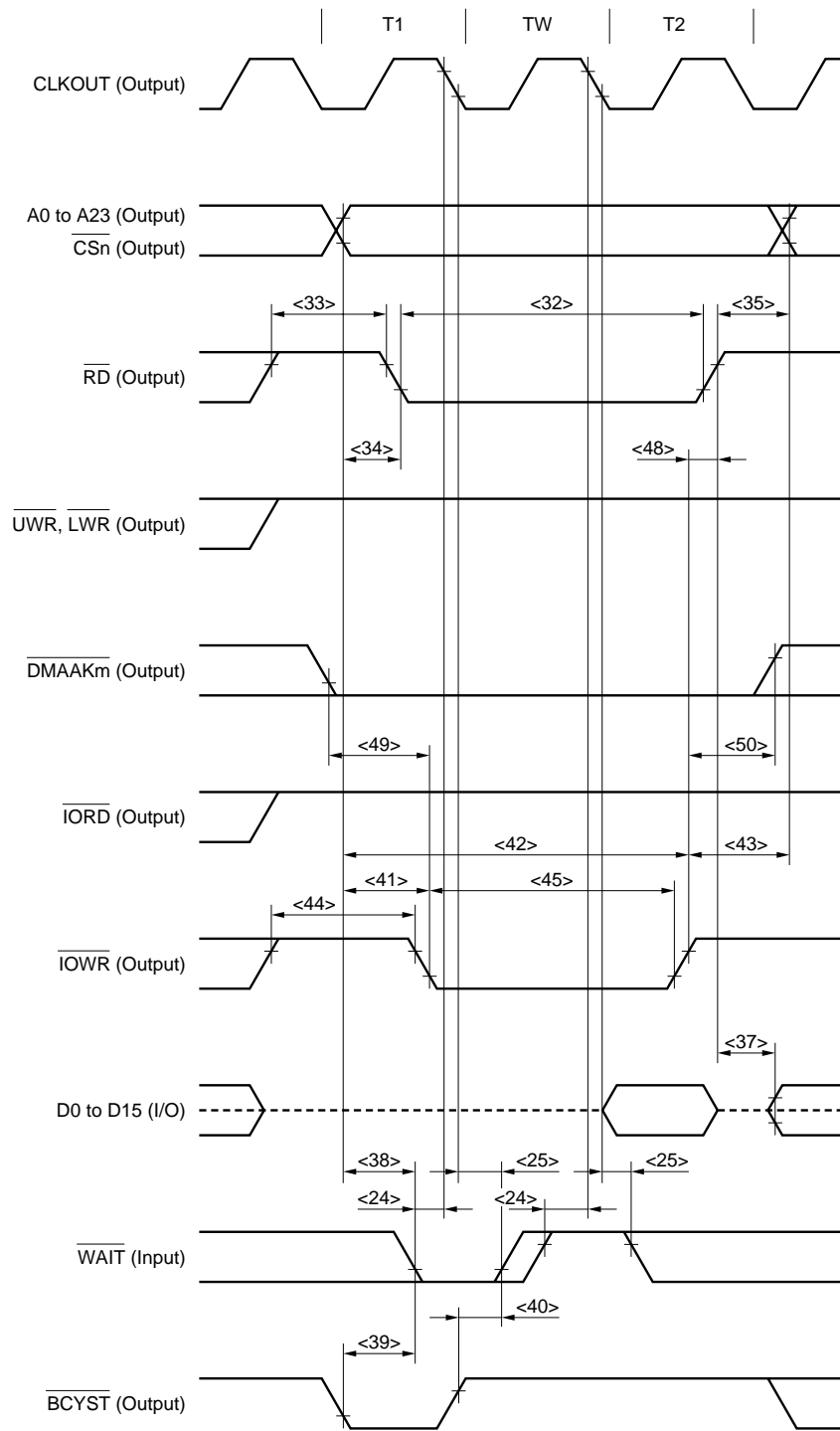
(d) DMA flyby transfer timing (SRAM → external I/O transfer) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	$t_{\text{SWK}}$	15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	$t_{\text{HKW}}$	2		ns
$\overline{\text{RD}}$ low-level width	<32>	$t_{\text{WRDL}}$	$(1 + w_D + w_F + w)T - 10$		ns
$\overline{\text{RD}}$ high-level width	<33>	$t_{\text{WRDH}}$	$T - 10$		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{RD}}$ ↓	<34>	$t_{\text{DARD}}$	$0.5T - 10$		ns
Delay time from $\overline{\text{RD}}$ ↑ to address	<35>	$t_{\text{DRDA}}$	$(0.5 + i)T - 10$		ns
Delay time from $\overline{\text{RD}}$ ↑ to data output	<37>	$t_{\text{DRDOD}}$	$(0.5 + i)T - 10$		ns
$\overline{\text{WAIT}}$ setup time (to address)	<38>	$t_{\text{SAW}}$	<b>Note</b>	$T - 25$	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}$ ↓)	<39>	$t_{\text{SBSW}}$	<b>Note</b>	$T - 25$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}$ ↑)	<40>	$t_{\text{HBSW}}$	<b>Note</b>	0	ns
Delay time from address to $\overline{\text{IOWR}}$ ↓	<41>	$t_{\text{DAWR}}$	$0.5T - 10$		ns
Address setup time (to $\overline{\text{IOWR}}$ ↑)	<42>	$t_{\text{SAWR}}$	$(1.5 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to address	<43>	$t_{\text{DWRA}}$	$0.5T - 10$		ns
$\overline{\text{IOWR}}$ high-level width	<44>	$t_{\text{WWRH}}$	$T - 10$		ns
$\overline{\text{IOWR}}$ low-level width	<45>	$t_{\text{WWRL}}$	$(1 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to $\overline{\text{RD}}$ ↑	<48>	$t_{\text{DWRRD}}$	$w_F = 0$	0	ns
			$w_F = 1$	$T - 10$	ns
Delay time from $\overline{\text{DMAAKm}}$ ↓ to $\overline{\text{IOWR}}$ ↓	<49>	$t_{\text{DDAWR}}$	$0.5T - 10$		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to $\overline{\text{DMAAKm}}$ ↑	<50>	$t_{\text{DWRDA}}$	$(0.5 + w_F)T - 10$		ns

**Note** For first  $\overline{\text{WAIT}}$  sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

- Remarks**
1.  $T = t_{\text{CYK}}$
  2.  $w$ : The number of waits due to  $\overline{\text{WAIT}}$ .
  3.  $w_D$ : The number of waits due to the DWC1 and DWC2 registers.
  4.  $w_F$ : The number of waits that are inserted for a source-side access during a DMA flyby transfer.
  5.  $i$ : The number of idle states that are inserted when a write cycle follows a read cycle.
  6.  $n = 0, 3$  to  $5, m = 0$  to  $3$

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and  $w_F = 0$ .
  2. The broken lines indicate high impedance.
  3.  $n = 0, 3$  to  $5$ ,  $m = 0$  to  $3$

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (1/2)

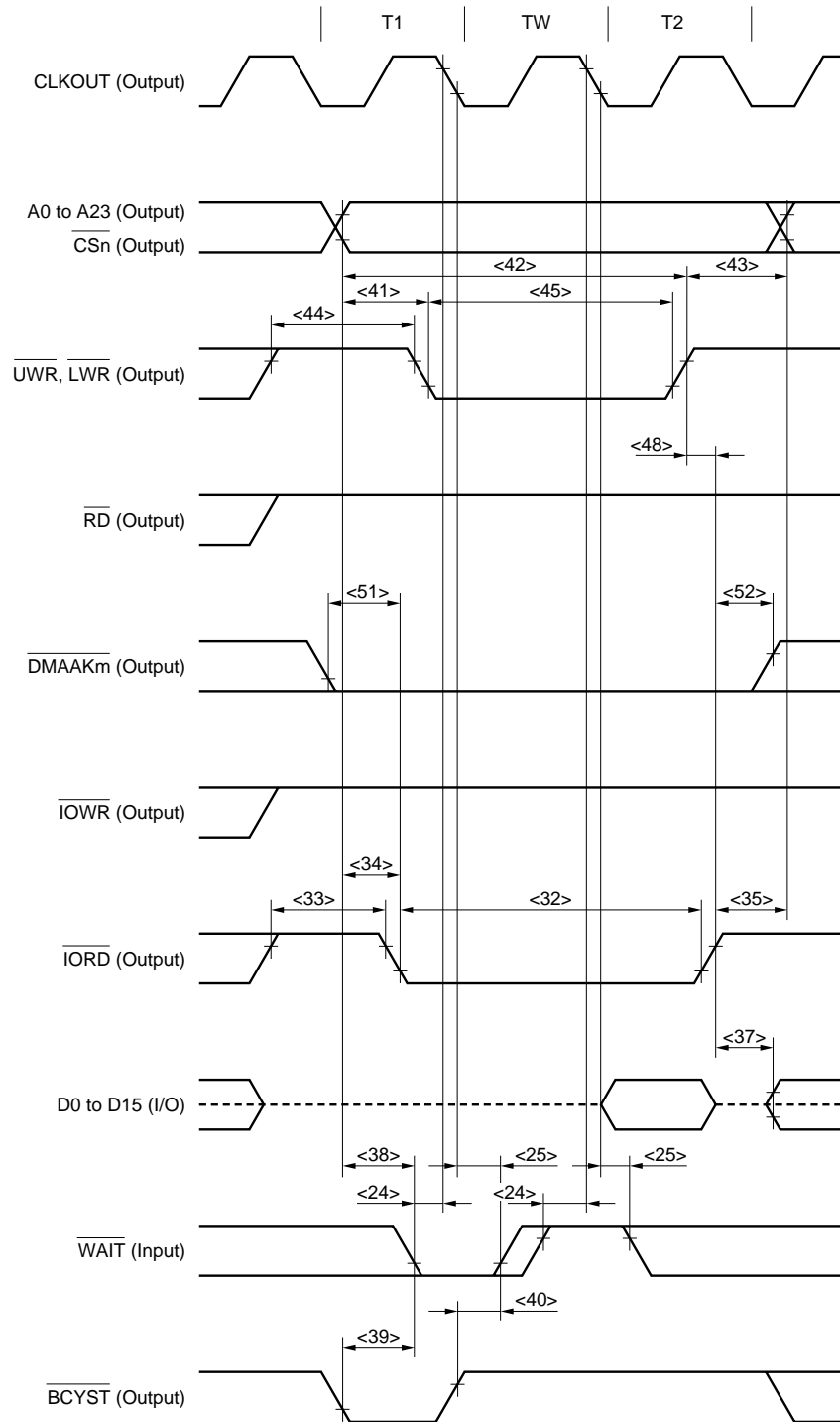
Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	$t_{\text{SWK}}$	15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	$t_{\text{HKW}}$	2		ns
$\overline{\text{IORD}}$ low-level width	<32>	$t_{\text{WRDL}}$	$(1 + w_D + w_F + w)T - 10$		ns
$\overline{\text{IORD}}$ high-level width	<33>	$t_{\text{WRDH}}$	$T - 10$		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{IORD}}$ ↓	<34>	$t_{\text{DARD}}$	$0.5T - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↑ to address	<35>	$t_{\text{DRDA}}$	$(0.5 + i)T - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↑ to data output	<37>	$t_{\text{DRDOD}}$	$(0.5 + i)T - 10$		ns
$\overline{\text{WAIT}}$ setup time (to address)	<38>	$t_{\text{SAW}}$	<b>Note</b>	$T - 25$	ns
$\overline{\text{WAIT}}$ setup time (to BCYST ↓)	<39>	$t_{\text{SBSW}}$	<b>Note</b>	$T - 25$	ns
$\overline{\text{WAIT}}$ hold time (from BCYST ↑)	<40>	$t_{\text{HBSW}}$	<b>Note</b>	0	ns
Delay time from address to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ ↓	<41>	$t_{\text{DAWR}}$	$0.5T - 10$		ns
Address setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ ↑)	<42>	$t_{\text{SAWR}}$	$(1.5 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ to address	<43>	$t_{\text{DWRA}}$	$0.5T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ high-level width	<44>	$t_{\text{WWRH}}$	$T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ low-level width	<45>	$t_{\text{WWRL}}$	$(1 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ ↑ to $\overline{\text{IORD}}$ ↑	<48>	$t_{\text{DWRRD}}$	$w_F = 0$	0	ns
			$w_F = 1$	$T - 10$	ns
Delay time from $\overline{\text{DMAAKm}}$ ↓ to $\overline{\text{IORD}}$ ↓	<51>	$t_{\text{DDARD}}$	$0.5T - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↑ to $\overline{\text{DMAAKm}}$ ↑	<52>	$t_{\text{DRDDA}}$	$0.5T - 10$		ns

**Note** For first  $\overline{\text{WAIT}}$  sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

- Remarks**
1.  $T = t_{\text{CYK}}$
  2.  $w$ : The number of waits due to  $\overline{\text{WAIT}}$ .
  3.  $w_D$ : The number of waits due to the DWC1 and DWC2 registers.
  4.  $w_F$ : The number of waits that are inserted for a source-side access during a DMA flyby transfer.
  5.  $i$ : The number of idle states that are inserted when a write cycle follows a read cycle.
  6.  $n = 0, 3$  to  $5$ ,  $m = 0$  to  $3$



(e) DMA flyby transfer timing (external I/O → SRAM transfer) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and  $w_F = 0$ .
  2. The broken lines indicate high impedance.
  3.  $n = 0, 3$  to  $5$ ,  $m = 0$  to  $3$

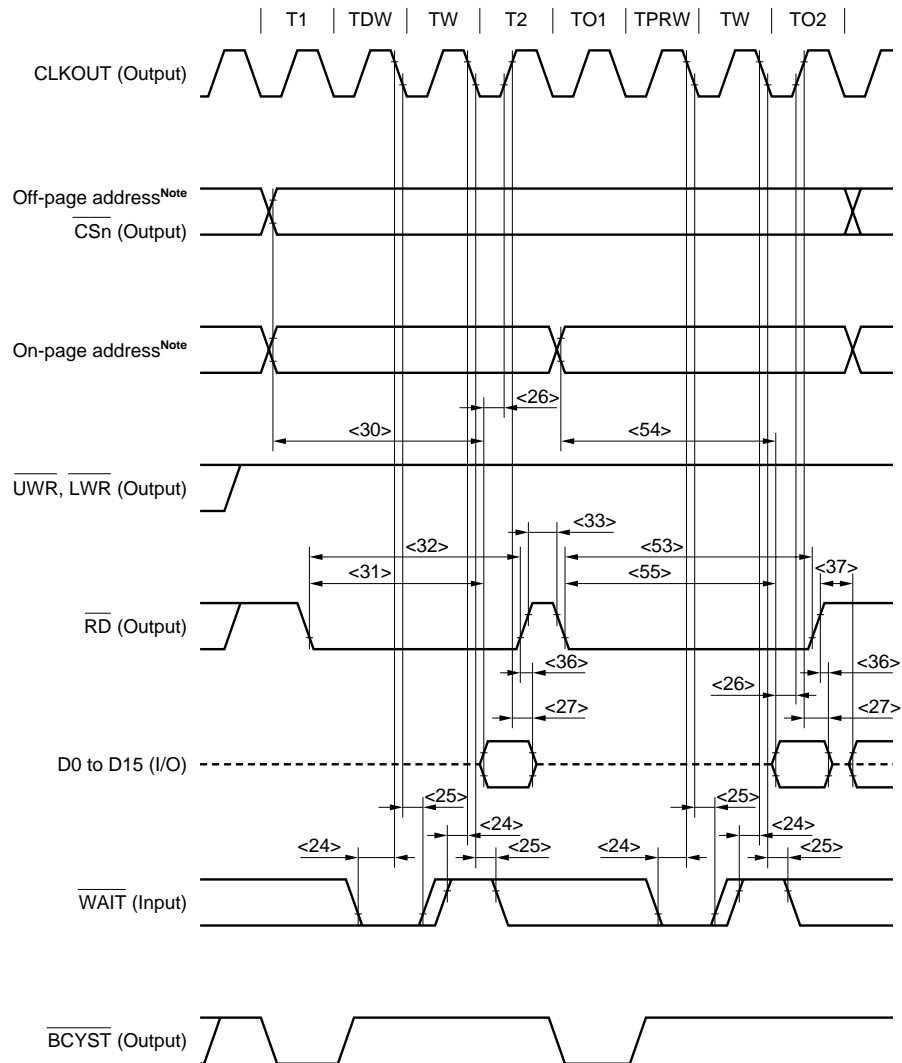
(5) Page ROM access timing (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24> $t_{\text{SWK}}$		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25> $t_{\text{HKW}}$		2		ns
Data input setup time (to CLKOUT ↑)	<26> $t_{\text{SKID}}$		18		ns
Data input hold time (from CLKOUT ↑)	<27> $t_{\text{HKID}}$		2		ns
Off-page data input setup time (to address)	<30> $t_{\text{SAID}}$			$(1.5 + w_D + w)T - 28$	ns
Off-page data input setup time (to $\overline{\text{RD}}$ )	<31> $t_{\text{SRDID}}$			$(1 + w_D + w)T - 32$	ns
Off-page $\overline{\text{RD}}$ low-level width	<32> $t_{\text{WRDL}}$		$(1 + w_D + w)T - 10$		ns
$\overline{\text{RD}}$ high-level width	<33> $t_{\text{WRDH}}$		$0.5T - 10$		ns
Data input hold time (from $\overline{\text{RD}}$ )	<36> $t_{\text{HRDID}}$		0		ns
Delay time from $\overline{\text{RD}}$ ↑ to data output	<37> $t_{\text{DRDOD}}$		$(0.5 + i)T - 10$		ns
On-page $\overline{\text{RD}}$ low-level width	<53> $t_{\text{WORDL}}$		$(1.5 + w_{\text{PR}} + w)T - 10$		ns
On-page data input setup time (to address)	<54> $t_{\text{SOAID}}$			$(1.5 + w_{\text{PR}} + w)T - 28$	ns
On-page data input setup time (to $\overline{\text{RD}}$ )	<55> $t_{\text{SORID}}$			$(1.5 + w_{\text{PR}} + w)T - 32$	ns

Remarks 1.  $T = t_{\text{CYK}}$

2.  $w$ : The number of waits due to  $\overline{\text{WAIT}}$ .
3.  $w_D$ : The number of waits due to the DWC1 and DWC2 registers.
4.  $w_{\text{PR}}$ : The number of waits due to the PRC register.
5.  $i$ : The number of idle states that are inserted when a write cycle follows a read cycle.
6. Maintain at least one of the data input hold times,  $t_{\text{HKID}}$  or  $t_{\text{HRDID}}$ .

(5) Page ROM access timing (2/2)



**Note** On-page and off-page addresses are as follows.

PRC Register			On-page Addresses	Off-page Addresses
MA5	MA4	MA3		
0	0	0	A0, A1	A2 to A23
0	0	1	A0 to A2	A3 to A23
0	1	1	A0 to A3	A4 to A23
1	1	1	A0 to A4	A5 to A23

- Remarks**
- This is the timing for the following case.  
 Number of waits due to the DWC1 and DWC2 registers (TDW): 1  
 Number of waits due to the PRC register (TPRW): 1
  - The broken lines indicate high impedance.
  - n = 0, 3 to 5

(6) DRAM access timing

(a) Read timing (high-speed page DRAM access, normal access: off-page) (1/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
WAIT setup time (to CLKOUT ↓)	<24>	t <sub>SWK</sub>	15		ns
WAIT hold time (from CLKOUT ↓)	<25>	t <sub>HKW</sub>	2		ns
Data input setup time (to CLKOUT ↑)	<26>	t <sub>SKID</sub>	18		ns
Data input hold time (from CLKOUT ↑)	<27>	t <sub>HKID</sub>	2		ns
Delay time from $\overline{OE}$ ↑ to data output	<37>	t <sub>DRDOD</sub>	$(0.5 + i)T - 10$		ns
Row address setup time	<56>	t <sub>ASR</sub>	$(0.5 + W_{RP})T - 10$		ns
Row address hold time	<57>	t <sub>RAH</sub>	$(0.5 + W_{RH})T - 10$		ns
Column address setup time	<58>	t <sub>ASC</sub>	$0.5T - 10$		ns
Column address hold time	<59>	t <sub>CAH</sub>	$(1.5 + W_{DA} + w)T - 10$		ns
Read/write cycle time	<60>	t <sub>RC</sub>	$(3 + W_{RP} + W_{RH} + W_{DA} + w)T - 10$		ns
$\overline{RAS}$ precharge time	<61>	t <sub>RP</sub>	$(0.5 + W_{RP})T - 10$		ns
$\overline{RAS}$ pulse time	<62>	t <sub>RAS</sub>	$(2.5 + W_{RH} + W_{DA} + w)T - 10$		ns
$\overline{RAS}$ hold time	<63>	t <sub>RSH</sub>	$(1.5 + W_{DA} + w)T - 10$		ns
Column address read time for $\overline{RAS}$	<64>	t <sub>RAL</sub>	$(2 + W_{DA} + w)T - 10$		ns
$\overline{CAS}$ pulse width	<65>	t <sub>CAS</sub>	$(1 + W_{DA} + w)T - 10$		ns
$\overline{CAS}$ - $\overline{RAS}$ precharge time	<66>	t <sub>CRP</sub>	$(1 + W_{RP})T - 10$		ns
$\overline{CAS}$ hold time	<67>	t <sub>CSH</sub>	$(2 + W_{RH} + W_{DA} + w)T - 10$		ns
$\overline{WE}$ setup time	<68>	t <sub>RCS</sub>	$(2 + W_{RP} + W_{RH})T - 10$		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)	<69>	t <sub>RRH</sub>	$0.5T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)	<70>	t <sub>RCH</sub>	$T - 10$		ns
$\overline{CAS}$ precharge time	<71>	t <sub>CPN</sub>	$(2 + W_{RP} + W_{RH})T - 10$		ns
Output enable access time	<72>	t <sub>OEA</sub>		$(2 + W_{RP} + W_{RH} + W_{DA} + w)T - 28$	ns
$\overline{RAS}$ access time	<73>	t <sub>RAC</sub>		$(2 + W_{RH} + W_{DA} + w)T - 28$	ns
Access time from column address	<74>	t <sub>AA</sub>		$(1.5 + W_{DA} + w)T - 28$	ns
$\overline{CAS}$ access time	<75>	t <sub>CAC</sub>		$(1 + W_{DA} + w)T - 28$	ns

Remarks 1. T = t<sub>cyk</sub>

2. w: The number of waits due to  $\overline{WAIT}$ .

3. W<sub>RP</sub>: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. W<sub>RH</sub>: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. W<sub>DA</sub>: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

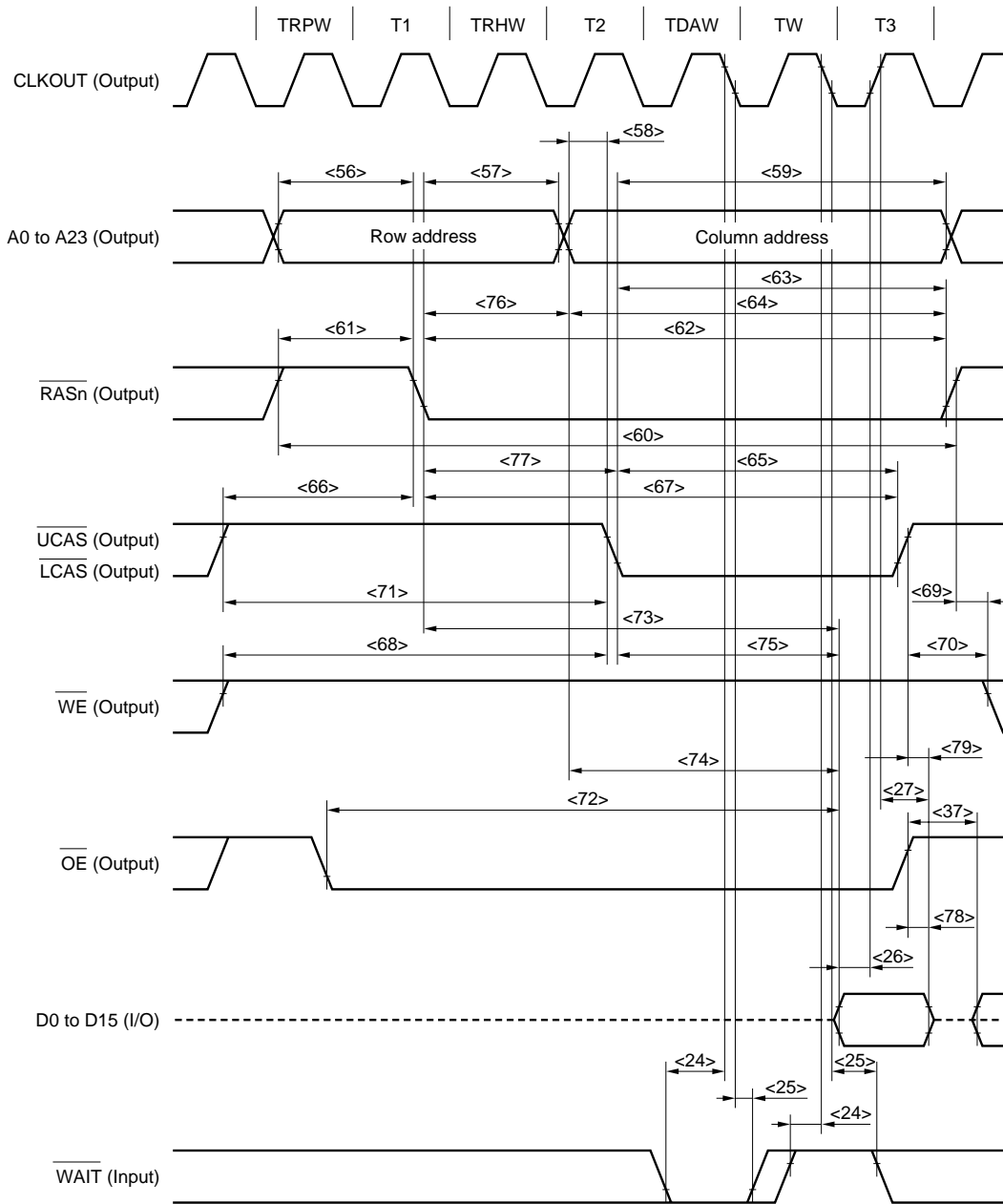
6. i: The number of idle states that are inserted when a write cycle follows a read cycle.

(a) Read timing (high-speed page DRAM access, normal access: off-page) (2/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{RAS}}$ column address delay time	<76> $t_{\text{RAD}}$		$(0.5 + W_{\text{RH}})T - 10$		ns
$\overline{\text{RAS}}$ - $\overline{\text{CAS}}$ delay time	<77> $t_{\text{RCD}}$		$(1 + W_{\text{RH}})T - 10$		ns
Output buffer turn-off delay time (from $\overline{\text{OE}} \uparrow$ )	<78> $t_{\text{OEZ}}$		0		ns
Output buffer turn-off delay time (from $\overline{\text{CAS}} \uparrow$ )	<79> $t_{\text{OFF}}$		0		ns

- Remarks**
1.  $T = t_{\text{CYK}}$
  2.  $W_{\text{RH}}$ : The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(a) Read timing (high-speed page DRAM access, normal access: off-page) (3/3)



- Remarks**
1. This is the timing for the following case ( $n = 0$  to  $3$ ,  $xx = 00$  to  $03$ ,  $10$  to  $13$ ).  
 Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1  
 Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1  
 Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
  2. The broken lines indicate high impedance.
  3.  $n = 3$  to  $5$

[MEMO]

(b) Read timing (high-speed page DRAM access: on-page) (1/2)

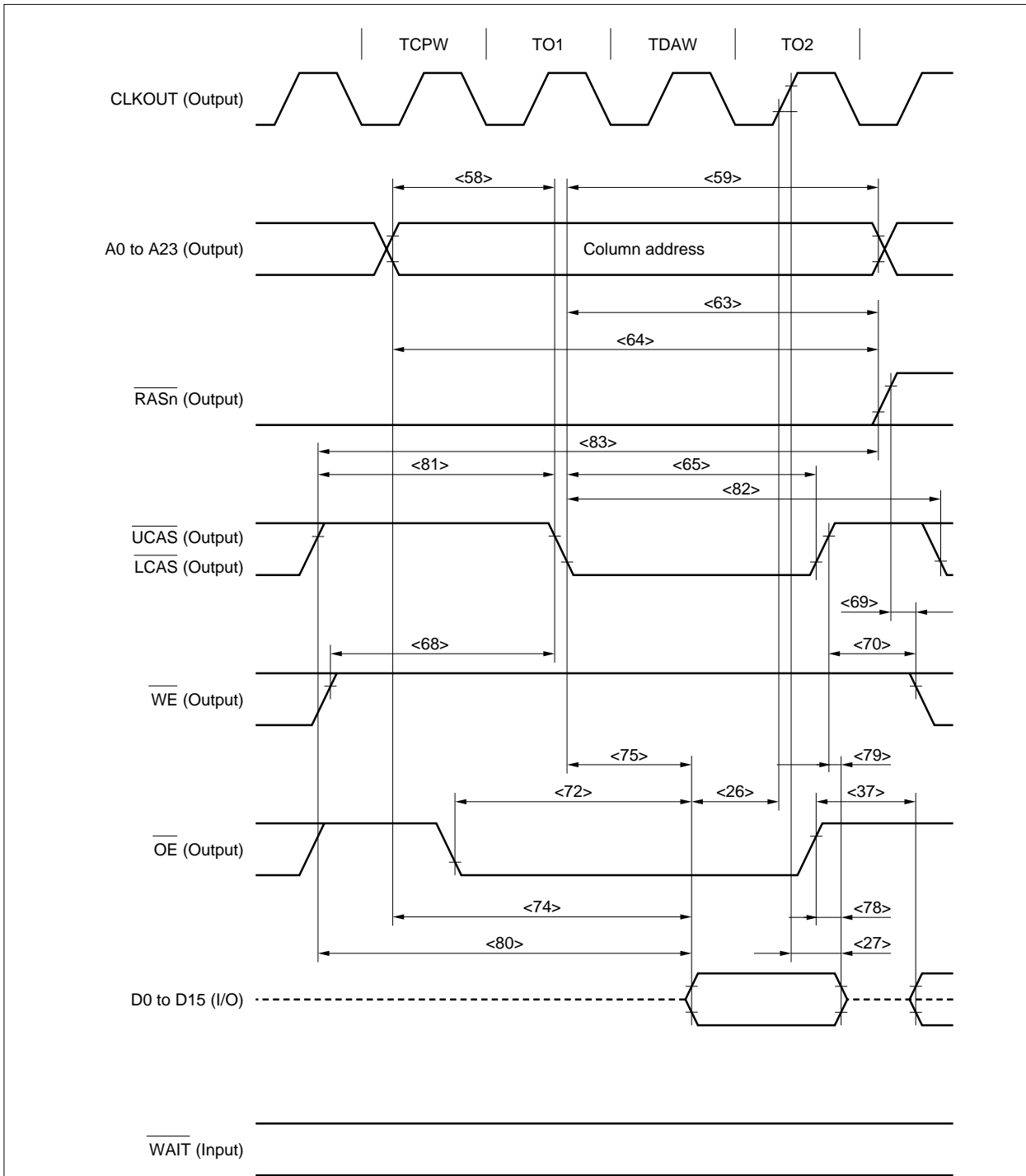
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)	<26>	t <sub>SKID</sub>	18		ns
Data input hold time (from CLKOUT ↑)	<27>	t <sub>HKID</sub>	2		ns
Delay time from $\overline{OE}$ ↑ to data output	<37>	t <sub>DRDOD</sub>	$(0.5 + i)T - 10$		ns
Column address setup time	<58>	t <sub>ASC</sub>	$(0.5 + W_{CP})T - 10$		ns
Column address hold time	<59>	t <sub>CAH</sub>	$(1.5 + W_{DA})T - 10$		ns
$\overline{RAS}$ hold time	<63>	t <sub>RSH</sub>	$(1.5 + W_{DA})T - 10$		ns
Column address read time for $\overline{RAS}$	<64>	t <sub>RAL</sub>	$(2 + W_{CP} + W_{DA})T - 10$		ns
$\overline{CAS}$ pulse width	<65>	t <sub>CAS</sub>	$(1 + W_{DA})T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<68>	t <sub>RCS</sub>	$(1 + W_{CP})T - 10$		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)	<69>	t <sub>RRH</sub>	$0.5T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)	<70>	t <sub>RCH</sub>	$T - 10$		ns
Output enable access time	<72>	t <sub>OEa</sub>		$(1 + W_{CP} + W_{DA})T - 28$	ns
Access time from column address	<74>	t <sub>AA</sub>		$(1.5 + W_{CP} + W_{DA})T - 28$	ns
$\overline{CAS}$ access time	<75>	t <sub>CAC</sub>		$(1 + W_{DA})T - 28$	ns
Output buffer turn-off delay time (from $\overline{OE}$ ↑)	<78>	t <sub>OEZ</sub>	0		ns
Output buffer turn-off delay time (from $\overline{CAS}$ ↑)	<79>	t <sub>OFF</sub>	0		ns
Access time from $\overline{CAS}$ precharge	<80>	t <sub>ACP</sub>		$(2 + W_{CP} + W_{DA})T - 28$	ns
$\overline{CAS}$ precharge time	<81>	t <sub>CP</sub>	$(1 + W_{CP})T - 10$		ns
High-speed page mode cycle time	<82>	t <sub>PC</sub>	$(2 + W_{CP} + W_{DA})T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83>	t <sub>RHCP</sub>	$(2.5 + W_{CP} + W_{DA})T - 10$		ns

**Remarks 1.** T = t<sub>cyk</sub>

2. w<sub>CP</sub>: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
3. w<sub>DA</sub>: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. i: The number of idle states that are inserted when a write cycle follows a read cycle.



(b) Read timing (high-speed page DRAM access: on-page) (2/2)



- Remarks**
- This is the timing for the following case ( $n = 0$  to  $3$ ,  $xx = 00$  to  $03$ ,  $10$  to  $13$ ).  
 Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1  
 Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
  - The broken lines indicate high impedance.
  - $n = 3$  to  $5$

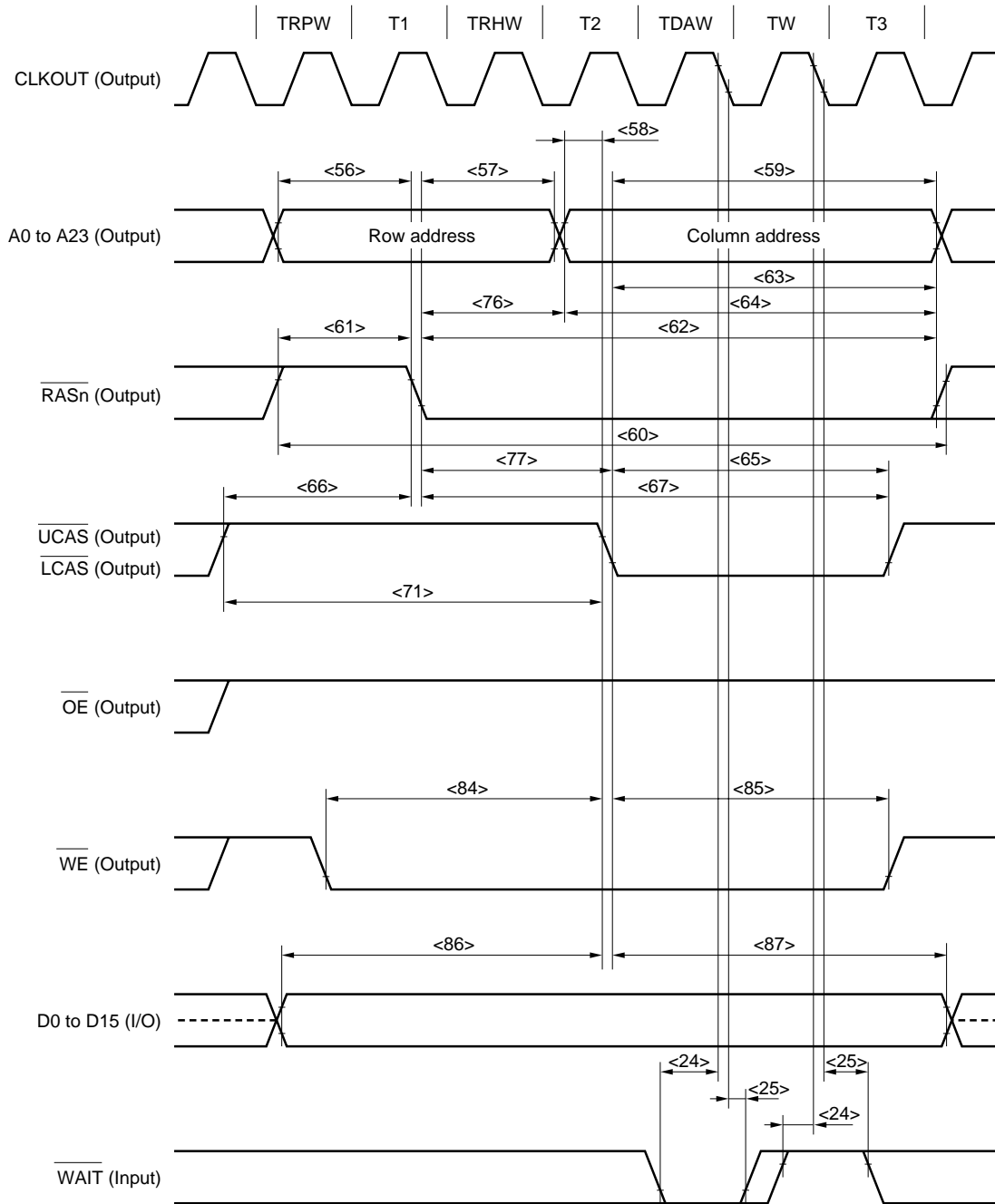
## (c) Write timing (high-speed page DRAM access, normal access: off-page) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	$t_{\text{SWK}}$	15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	$t_{\text{HKW}}$	2		ns
Row address setup time	<56>	$t_{\text{ASR}}$	$(0.5 + W_{\text{RP}})T - 10$		ns
Row address hold time	<57>	$t_{\text{RAH}}$	$(0.5 + W_{\text{RH}})T - 10$		ns
Column address setup time	<58>	$t_{\text{ASC}}$	$0.5T - 10$		ns
Column address hold time	<59>	$t_{\text{CAH}}$	$(1.5 + W_{\text{DA}} + w)T - 10$		ns
Read/write cycle time	<60>	$t_{\text{RC}}$	$(3 + W_{\text{RP}} + W_{\text{RH}} + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61>	$t_{\text{RP}}$	$(0.5 + W_{\text{RP}})T - 10$		ns
$\overline{\text{RAS}}$ pulse time	<62>	$t_{\text{RAS}}$	$(2.5 + W_{\text{RH}} + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63>	$t_{\text{RSH}}$	$(1.5 + W_{\text{DA}} + w)T - 10$		ns
Column address read time (from $\overline{\text{RAS}}$ ↑)	<64>	$t_{\text{RAL}}$	$(2 + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65>	$t_{\text{CAS}}$	$(1 + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{CAS}}$ -RAS precharge time	<66>	$t_{\text{CRP}}$	$(1 + W_{\text{RH}})T - 10$		ns
$\overline{\text{CAS}}$ hold time	<67>	$t_{\text{CSH}}$	$(2 + W_{\text{RH}} + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{CAS}}$ precharge time	<71>	$t_{\text{CPN}}$	$(2 + W_{\text{RP}} + W_{\text{RH}})T - 10$		ns
$\overline{\text{RAS}}$ column address delay time	<76>	$t_{\text{RAD}}$	$(0.5 + W_{\text{RH}})T - 10$		ns
RAS-CAS delay time	<77>	$t_{\text{RCD}}$	$(1 + W_{\text{RH}})T - 10$		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}$ ↓)	<84>	$t_{\text{WCS}}$	$(1 + W_{\text{RP}} + W_{\text{RH}})T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}$ ↓)	<85>	$t_{\text{WCH}}$	$(1 + W_{\text{DA}} + w)T - 10$		ns
Data setup time (to $\overline{\text{CAS}}$ ↓)	<86>	$t_{\text{DS}}$	$(1.5 + W_{\text{RP}} + W_{\text{RH}})T - 10$		ns
Data hold time (from $\overline{\text{CAS}}$ ↓)	<87>	$t_{\text{DH}}$	$(1.5 + W_{\text{DA}} + w)T - 10$		ns

**Remarks 1.**  $T = t_{\text{CYK}}$

2.  $w$ : The number of waits due to  $\overline{\text{WAIT}}$ .
3.  $W_{\text{RP}}$ : The number of waits due to the RPCxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).
4.  $W_{\text{RH}}$ : The number of waits due to the RHCxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).
5.  $W_{\text{DA}}$ : The number of waits due to the DACxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).

(c) Write timing (high-speed page DRAM access, normal access: off-page) (2/2)



- Remarks**
- This is the timing for the following case ( $n = 0$  to  $3$ ,  $xx = 00$  to  $03$ ,  $10$  to  $13$ ).
    - Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
    - Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
    - Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
  - The broken lines indicate high impedance.
  - $n = 3$  to  $5$

## (d) Write timing (high-speed page DRAM access: on-page) (1/2)

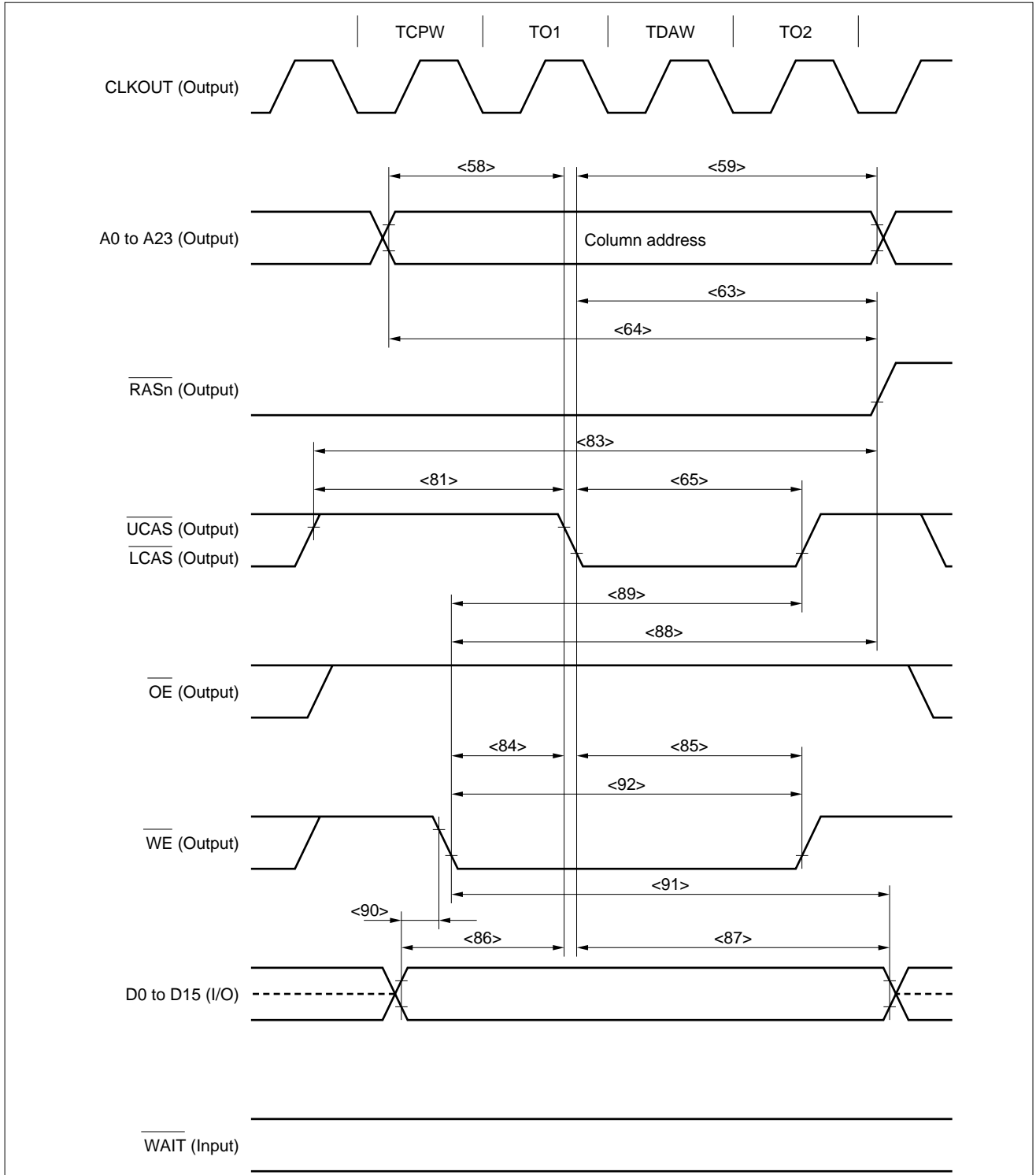
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Column address setup time	<58>	t <sub>ASC</sub>		$(0.5 + WCP)T - 10$		ns
Column address hold time	<59>	t <sub>CAH</sub>		$(1.5 + WDA)T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63>	t <sub>RSH</sub>		$(1.5 + WDA)T - 10$		ns
Column address read time (from $\overline{\text{RAS}} \uparrow$ )	<64>	t <sub>RAL</sub>		$(2 + WCP + WDA)T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65>	t <sub>CAS</sub>		$(1 + WDA)T - 10$		ns
$\overline{\text{CAS}}$ precharge time	<81>	t <sub>CP</sub>		$(1 + WCP)T - 10$		ns
$\overline{\text{RAS}}$ hold time for $\overline{\text{CAS}}$ precharge	<83>	t <sub>RHCP</sub>		$(2.5 + WCP + WDA)T - 10$		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}} \downarrow$ )	<84>	t <sub>WCS</sub>	WCP ≥ 1	WCP T - 10		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}} \downarrow$ )	<85>	t <sub>WCH</sub>		$(1 + WDA)T - 10$		ns
Data setup time (to $\overline{\text{CAS}} \downarrow$ )	<86>	t <sub>DS</sub>		$(0.5 + WCP)T - 10$		ns
Data hold time (from $\overline{\text{CAS}} \downarrow$ )	<87>	t <sub>DH</sub>		$(1.5 + WDA)T - 10$		ns
$\overline{\text{WE}}$ read time (from $\overline{\text{RAS}} \uparrow$ )	<88>	t <sub>RWL</sub>	WCP = 0	$(1.5 + WDA)T - 10$		ns
$\overline{\text{WE}}$ read time (from $\overline{\text{CAS}} \uparrow$ )	<89>	t <sub>CWL</sub>	WCP = 0	$(1 + WDA)T - 10$		ns
Data setup time (to $\overline{\text{WE}} \downarrow$ )	<90>	t <sub>DSWE</sub>	WCP = 0	0.5T - 10		ns
Data hold time (from $\overline{\text{WE}} \downarrow$ )	<91>	t <sub>DHWE</sub>	WCP = 0	$(1.5 + WDA)T - 10$		ns
$\overline{\text{WE}}$ pulse width	<92>	t <sub>WP</sub>	WCP = 0	$(1 + WDA)T - 10$		ns

**Remarks 1.** T = t<sub>cyk</sub>

**2.** w<sub>CP</sub>: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

**3.** w<sub>DA</sub>: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(d) Write timing (high-speed page DRAM access: on-page) (2/2)



- Remarks**
1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).  
 Number of waits due to the CPCxx bit of the DRCn register (TCPW) : 1  
 Number of waits due to the DACxx bit of the DRCn register (TDAW) : 1
  2. The broken lines indicate high impedance.
  3. n = 3 to 5

(e) Read timing (EDO DRAM) (1/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)	<26>	t <sub>SKID</sub>	18		ns
Data input hold time (from CLKOUT ↑)	<27>	t <sub>HKID</sub>	2		ns
Delay time from $\overline{OE}$ ↑ to data output	<37>	t <sub>DRDOD</sub>	$(0.5 + i)T - 10$		ns
Row address setup time	<56>	t <sub>ASR</sub>	$(0.5 + WRP)T - 10$		ns
Row address hold time	<57>	t <sub>RAH</sub>	$(0.5 + WRH)T - 10$		ns
Column address setup time	<58>	t <sub>ASC</sub>	$0.5T - 10$		ns
Column address hold time	<59>	t <sub>CAH</sub>	$(0.5 + WDA)T - 10$		ns
$\overline{RAS}$ precharge time	<61>	t <sub>RP</sub>	$(0.5 + WRP)T - 10$		ns
Column address read time (from $\overline{RAS}$ ↑)	<64>	t <sub>RAL</sub>	$(2 + WCP + WDA)T - 10$		ns
$\overline{CAS}$ - $\overline{RAS}$ precharge time	<66>	t <sub>CRP</sub>	$(1 + WRP)T - 10$		ns
$\overline{CAS}$ hold time	<67>	t <sub>CSH</sub>	$(1.5 + WRH + WDA)T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<68>	t <sub>RCS</sub>	$(2 + WRP + WRH)T - 10$		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)	<69>	t <sub>RRH</sub>	$0.5T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)	<70>	t <sub>RCH</sub>	$1.5T - 10$		ns
$\overline{RAS}$ access time	<73>	t <sub>RAC</sub>		$(2 + WRH + WDA)T - 28$	ns
Access time from column address	<74>	t <sub>AA</sub>		$(1.5 + WDA)T - 28$	ns
$\overline{CAS}$ access time	<75>	t <sub>CAC</sub>		$(1 + WDA)T - 28$	ns
Delay time from $\overline{RAS}$ to column address	<76>	t <sub>RAD</sub>	$(0.5 + WRH)T - 10$		ns
$\overline{RAS}$ - $\overline{CAS}$ delay time	<77>	t <sub>RCD</sub>	$(1 + WRH)T - 10$		ns
Output buffer turn-off delay time (from $\overline{OE}$ )	<78>	t <sub>OEZ</sub>	0		ns
Access time from $\overline{CAS}$ precharge	<80>	t <sub>ACP</sub>		$(1.5 + WCP + WDA)T - 28$	ns
$\overline{CAS}$ precharge time	<81>	t <sub>CP</sub>	$(0.5 + WCP)T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83>	t <sub>RHCP</sub>	$(2 + WCP + WDA)T - 10$		ns
Read cycle time	<93>	t <sub>HPC</sub>	$(1 + WDA + WCP)T - 10$		ns
$\overline{RAS}$ pulse width	<94>	t <sub>RASP</sub>	$(2.5 + WRH + WDA)T - 10$		ns
$\overline{CAS}$ pulse width	<95>	t <sub>HCAS</sub>	$(0.5 + WDA)T - 10$		ns
$\overline{CAS}$ hold time from $\overline{OE}$	Off-page	<96>	t <sub>och1</sub>	$(2 + WRH + WDA)T - 10$	ns
	On-page	<97>	t <sub>och2</sub>	$(0.5 + WDA)T - 10$	ns
Data input hold time (from $\overline{CAS}$ ↓)	<98>	t <sub>DHC</sub>	0		ns

Remarks 1. T = t<sub>cyk</sub>

2. WRP: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
3. WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. WDA: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. WCP: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
6. i: The number of idle states that are inserted when a write cycle follows a read cycle.

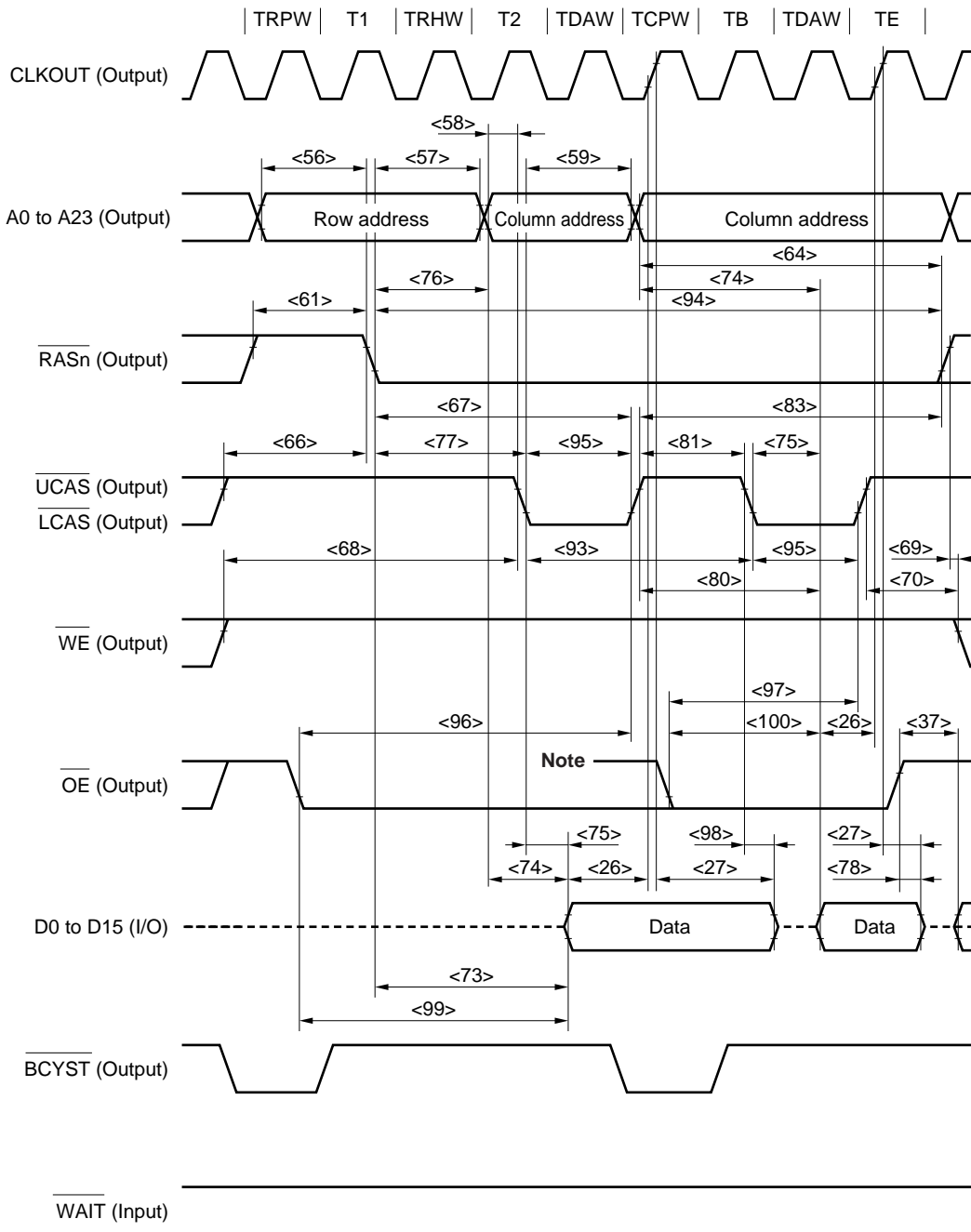
(e) Read timing (EDO DRAM) (2/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Output enable access time	Off-page	<99>	t <sub>OE1</sub>			$(2 + W_{RP} + W_{RH} + W_{DA})T - 28$	ns
	On-page	<100>	t <sub>OE2</sub>			$(1 + W_{CP} + W_{DA})T - 28$	ns

**Remarks** 1. T = t<sub>CYK</sub>

2. W<sub>RP</sub>: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
3. W<sub>RH</sub>: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. W<sub>DA</sub>: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. W<sub>CP</sub>: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(e) Read timing (EDO DRAM) (3/3)



**Note** For on-page access from another cycle during the RASn low-level signal.

- Remarks**
- This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
    - Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
    - Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
    - Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
    - Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
  - The broken lines indicate high impedance.
  - n = 3 to 5



[MEMO]

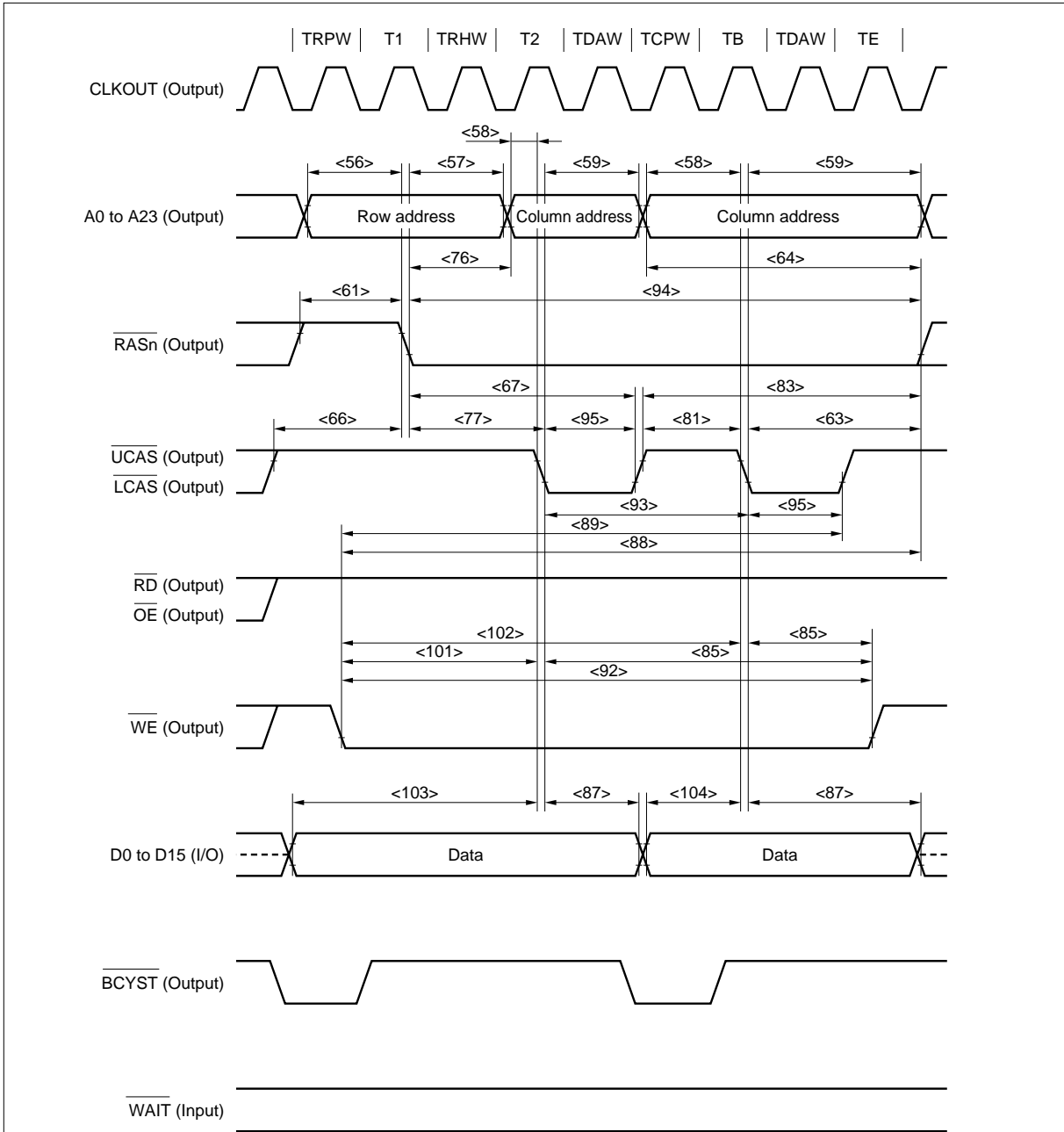
(f) Write timing (EDO DRAM) (1/2)

Parameter		Symbol	Condition	MIN.	MAX.	Unit
Row address setup time		<56>	t <sub>ASR</sub>		(0.5 + W <sub>RP</sub> )T – 10	ns
Row address hold time		<57>	t <sub>RAH</sub>		(0.5 + W <sub>RH</sub> )T – 10	ns
Column address setup time		<58>	t <sub>ASC</sub>		0.5T – 10	ns
Column address hold time		<59>	t <sub>CAH</sub>		(0.5 + W <sub>DA</sub> )T – 10	ns
RAS precharge time		<61>	t <sub>RP</sub>		(0.5 + W <sub>RP</sub> )T – 10	ns
RAS hold time		<63>	t <sub>RSH</sub>		(1.5 + W <sub>DA</sub> )T – 10	ns
Column address read time (from RAS ↑)		<64>	t <sub>RAL</sub>		(2 + W <sub>CP</sub> + W <sub>DA</sub> )T – 10	ns
CAS-RAS precharge time		<66>	t <sub>CRP</sub>		(1 + W <sub>RP</sub> )T – 10	ns
CAS hold time		<67>	t <sub>CSH</sub>		(1.5 + W <sub>RH</sub> + W <sub>DA</sub> )T – 10	ns
Delay time from RAS to column address		<76>	t <sub>RAD</sub>		(0.5 + W <sub>RH</sub> )T – 10	ns
RAS-CAS delay time		<77>	t <sub>RCD</sub>		(1 + W <sub>RH</sub> )T – 10	ns
CAS precharge time		<81>	t <sub>CP</sub>		(0.5 + W <sub>CP</sub> )T – 10	ns
RAS hold time for CAS precharge		<83>	t <sub>RHCP</sub>		(2 + W <sub>CP</sub> + W <sub>DA</sub> )T – 10	ns
WE hold time (from CAS ↓)		<85>	t <sub>WCH</sub>		(1 + W <sub>DA</sub> )T – 10	ns
Data hold time (from CAS ↓)		<87>	t <sub>DH</sub>		(0.5 + W <sub>DA</sub> )T – 10	ns
WE read time (from RAS ↑)	On-page	<88>	t <sub>RWL</sub>	W <sub>CP</sub> = 0	(1.5 + W <sub>DA</sub> )T – 10	ns
WE read time (from CAS ↑)	On-page	<89>	t <sub>CWL</sub>	W <sub>CP</sub> = 0	(0.5 + W <sub>DA</sub> )T – 10	ns
WE pulse width	On-page	<92>	t <sub>WP</sub>	W <sub>CP</sub> = 0	(1 + W <sub>DA</sub> )T – 10	ns
Write cycle time		<93>	t <sub>HPC</sub>		(1 + W <sub>DA</sub> + W <sub>CP</sub> )T – 10	ns
RAS pulse width		<94>	t <sub>RASP</sub>		(2.5 + W <sub>RH</sub> + W <sub>DA</sub> )T – 10	ns
CAS pulse width		<95>	t <sub>HCAS</sub>		(0.5 + W <sub>DA</sub> )T – 10	ns
WE setup time (to CAS ↓)	Off-page	<101>	t <sub>WCS1</sub>		(1 + W <sub>RP</sub> + W <sub>RH</sub> )T – 10	ns
	On-page	<102>	t <sub>WCS2</sub>	W <sub>CP</sub> ≥ 1	W <sub>CP</sub> T – 10	ns
Data setup time (to CAS ↓)	Off-page	<103>	t <sub>DS1</sub>		(1.5 + W <sub>RP</sub> + W <sub>RH</sub> )T – 10	ns
	On-page	<104>	t <sub>DS2</sub>		(0.5 + W <sub>CP</sub> )T – 10	ns

Remarks 1. T = t<sub>CYK</sub>

2. W<sub>RP</sub>: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
3. W<sub>RH</sub>: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. W<sub>DA</sub>: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. W<sub>CP</sub>: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(f) Write timing (EDO DRAM) (2/2)



- Remarks**
- This is the timing for the following case ( $n = 0$  to  $3$ ,  $xx = 00$  to  $03$ ,  $10$  to  $13$ ).
    - Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
    - Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
    - Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
    - Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
  - The broken lines indicate high impedance.
  - $n = 3$  to  $5$

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (1/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	$t_{\text{SWK}}$	15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	$t_{\text{HKW}}$	2		ns
Delay time from $\overline{\text{OE}} \uparrow$ to data output	<37>	$t_{\text{DRDOD}}$	$(0.5 + i)T - 10$		ns
Delay time from address to $\overline{\text{IOWR}} \downarrow$	<41>	$t_{\text{DAWR}}$	$(0.5 + \text{WRP})T - 10$		ns
Address setup time (to $\overline{\text{IOWR}} \uparrow$ )	<42>	$t_{\text{SAWR}}$	$(2 + \text{WRP} + \text{WRH} + \text{WDA} + w)T - 10$		ns
Delay time from $\overline{\text{IOWR}} \uparrow$ to address	<43>	$t_{\text{DWRA}}$	$0.5T - 10$		ns
Delay time from $\overline{\text{IOWR}} \uparrow$ to $\overline{\text{RD}} \uparrow$	<48>	$t_{\text{DWRD}}$	$\text{WF} = 0$	0	ns
			$\text{WF} = 1$	$T - 10$	ns
$\overline{\text{IOWR}}$ low-level width	<50>	$t_{\text{WWRL}}$	$(2 + \text{WRH} + \text{WDA} + w)T - 10$		ns
Row address setup time	<56>	$t_{\text{ASR}}$	$(0.5 + \text{WRP})T - 10$		ns
Row address hold time	<57>	$t_{\text{RAH}}$	$(0.5 + \text{WRH})T - 10$		ns
Column address setup time	<58>	$t_{\text{ASC}}$	$0.5T - 10$		ns
Column address hold time	<59>	$t_{\text{CAH}}$	$(1.5 + \text{WDA} + \text{WF} + w)T - 10$		ns
Read/write cycle time	<60>	$t_{\text{RC}}$	$(3 + \text{WRP} + \text{WRH} + \text{WDA} + \text{WF} + w)T - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61>	$t_{\text{RP}}$	$(0.5 + \text{WRP})T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63>	$t_{\text{RSH}}$	$(1.5 + \text{WDA} + \text{WF} + w)T - 10$		ns
Column address read time for $\overline{\text{RAS}}$	<64>	$t_{\text{RAL}}$	$(2 + \text{WCP} + \text{WDA} + \text{WF} + w)T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65>	$t_{\text{CAS}}$	$(1 + \text{WDA} + \text{WF} + w)T - 10$		ns
$\overline{\text{CAS}}$ - $\overline{\text{RAS}}$ precharge time	<66>	$t_{\text{CRP}}$	$(1 + \text{WRP})T - 10$		ns
$\overline{\text{CAS}}$ hold time	<67>	$t_{\text{CSH}}$	$(2 + \text{WRH} + \text{WDA} + \text{WF} + w)T - 10$		ns

- Remarks**
1.  $T = t_{\text{CYK}}$
  2.  $w$ : The number of waits due to  $\overline{\text{WAIT}}$ .
  3.  $\text{WRP}$ : The number of waits due to the  $\text{RPCxx}$  bit of the  $\text{DRCn}$  register ( $n = 0$  to  $3$ ,  $\text{xx} = 00$  to  $03$ ,  $10$  to  $13$ ).
  4.  $\text{WRH}$ : The number of waits due to the  $\text{RHCxx}$  bit of the  $\text{DRCn}$  register ( $n = 0$  to  $3$ ,  $\text{xx} = 00$  to  $03$ ,  $10$  to  $13$ ).
  5.  $\text{WDA}$ : The number of waits due to the  $\text{DACxx}$  bit of the  $\text{DRCn}$  register ( $n = 0$  to  $3$ ,  $\text{xx} = 00$  to  $03$ ,  $10$  to  $13$ ).
  6.  $\text{WCP}$ : The number of waits due to the  $\text{CPCxx}$  bit of the  $\text{DRCn}$  register ( $n = 0$  to  $3$ ,  $\text{xx} = 00$  to  $03$ ,  $10$  to  $13$ ).
  7.  $\text{WF}$ : The number of waits that are inserted for a source-side access during a DMA flyby transfer.
  8.  $i$ : The number of idle states that are inserted when a write cycle follows a read cycle.

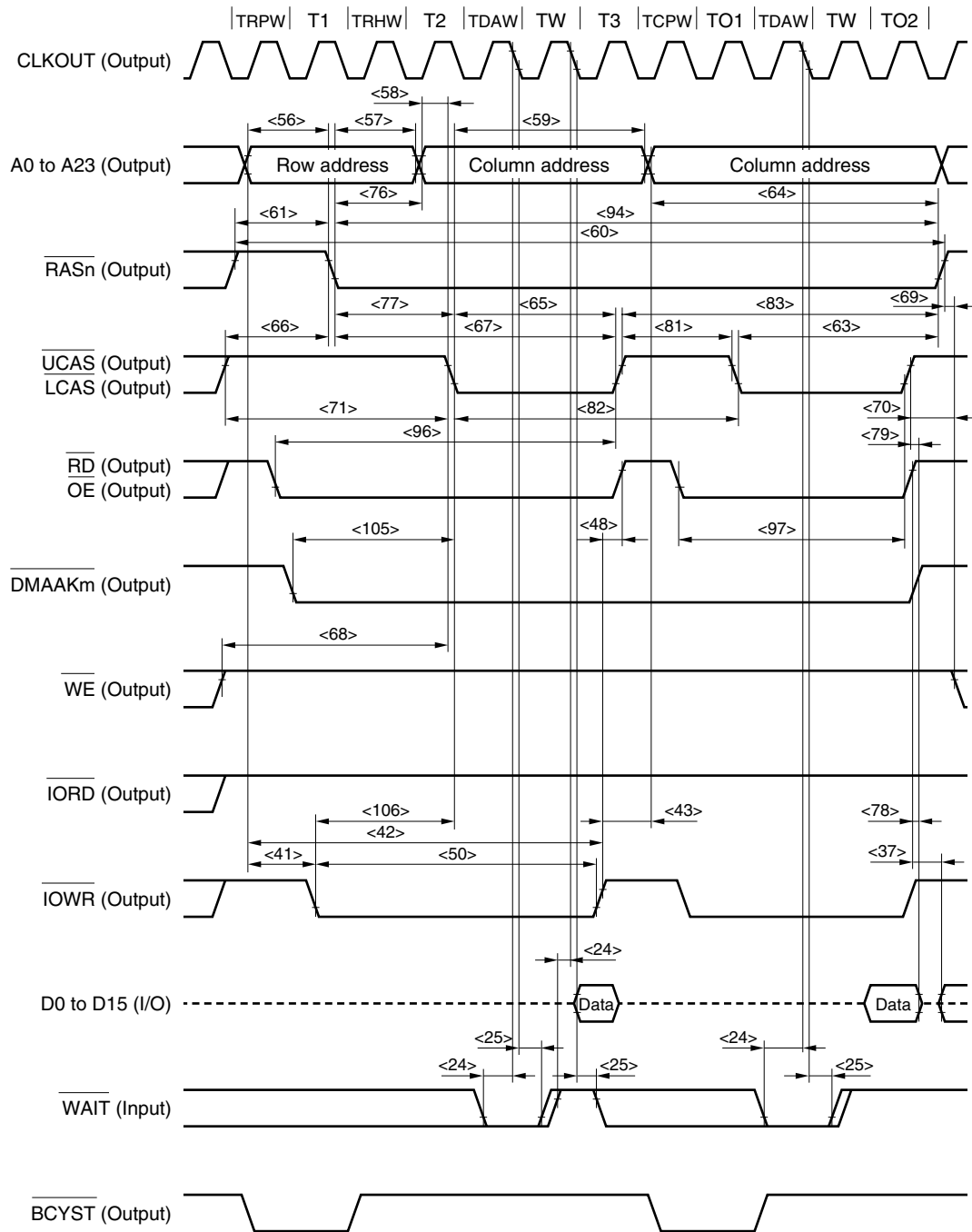
(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (2/3)

Parameter		Symbol	Condition	MIN.	MAX.	Unit
$\overline{WE}$ setup time (to $\overline{CAS} \downarrow$ )		<68>	tRCS		$(2 + WRP + WRH)T - 10$	ns
$\overline{WE}$ hold time (from $\overline{RAS} \uparrow$ )		<69>	tRRH		$0.5T - 10$	ns
$\overline{WE}$ hold time (from $\overline{CAS} \uparrow$ )		<70>	tRCH		$1.5T - 10$	ns
$\overline{CAS}$ precharge time		<71>	tCPN		$(2 + WRP + WRH)T - 10$	ns
Delay time from $\overline{RAS}$ to column address		<76>	tRAD		$(0.5 + WRH)T - 10$	ns
$\overline{RAS}$ - $\overline{CAS}$ delay time		<77>	tRCD		$(1 + WRH)T - 10$	ns
Output buffer turn-off delay time (from $\overline{OE} \uparrow$ )		<78>	tOEZ		0	ns
Output buffer turn-off delay time (from $\overline{CAS} \uparrow$ )		<79>	tOFF		0	ns
$\overline{CAS}$ precharge time		<81>	tCP		$(0.5 + WCP)T - 10$	ns
High-speed page mode cycle time		<82>	tPC		$(2 + WCP + WDA + WF + W)T - 10$	ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	tRHCP		$(2.5 + WCP + WDA + WF + W)T - 10$	ns
$\overline{RAS}$ pulse width		<94>	tRASP		$(2.5 + WRH + WDA + WF + W)T - 10$	ns
$\overline{CAS}$ hold time from $\overline{OE}$ (from $\overline{CAS} \uparrow$ )	Off-page	<96>	tOCH1		$(2.5 + WRP + WRH + WDA + WF + W)T - 10$	ns
	On-page	<97>	tOCH2		$(1.5 + WCP + WDA + WF + W)T - 10$	ns
Delay time from $\overline{DMAAKm} \downarrow$ to $\overline{CAS} \downarrow$		<105>	tDDACS		$(1.5 + WRH)T - 10$	ns
Delay time from $\overline{IOWR} \downarrow$ to $\overline{CAS} \downarrow$		<106>	tDRDCS		$(1 + WRH)T - 10$	ns

**Remarks** 1.  $T = t_{CYK}$

2.  $w$ : The number of waits due to  $\overline{WAIT}$ .
3.  $WCP$ : The number of waits due to the CPCxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).
4.  $WDA$ : The number of waits due to the DACxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).
5.  $WRH$ : The number of waits due to the RHCxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).
6.  $WRP$ : The number of waits due to the RPCxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).
7.  $WF$ : The number of waits that are inserted for a source-side access during a DMA flyby transfer.
8.  $m = 0$  to 3

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (3/3)



- Remarks**
1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).  
 Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1  
 Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1  
 Number of waits due to the DACxx bit of the DRCn register (TDAW): 1  
 Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1  
 Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0
  2. The broken lines indicate high impedance.
  3. n = 3 to 5, m = 0 to 3

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (1/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	t <sub>SWK</sub>	15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	t <sub>HKW</sub>	2		ns
$\overline{\text{IORD}}$ low-level width	<32>	t <sub>WRDL</sub>	$(2 + \text{WRH} + \text{WDA} + \text{WF} + \text{w})\text{T} - 10$		ns
$\overline{\text{IORD}}$ high-level width	<33>	t <sub>WRDH</sub>	$\text{T} - 10$		ns
Delay time from address to $\overline{\text{IORD}}$ ↑	<34>	t <sub>DARD</sub>	$0.5\text{T} - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↑ to address	<35>	t <sub>DRDA</sub>	$(0.5 + i)\text{T} - 10$		ns
Row address setup time	<56>	t <sub>ASR</sub>	$(0.5 + \text{WRP})\text{T} - 10$		ns
Row address hold time	<57>	t <sub>RAH</sub>	$(0.5 + \text{WRH})\text{T} - 10$		ns
Column address setup time	<58>	t <sub>ASC</sub>	$0.5\text{T} - 10$		ns
Column address hold time	<59>	t <sub>CAH</sub>	$(1.5 + \text{WDA} + \text{WF})\text{T} - 10$		ns
Read/write cycle time	<60>	t <sub>RC</sub>	$(3 + \text{WRP} + \text{WRH} + \text{WDA} + \text{WF} + \text{w})\text{T} - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61>	t <sub>RP</sub>	$(0.5 + \text{WRP})\text{T} - 10$		ns
$\overline{\text{RAS}}$ hold time	<63>	t <sub>RSH</sub>	$(1.5 + \text{WDA} + \text{WF})\text{T} - 10$		ns
Column address read time for $\overline{\text{RAS}}$	<64>	t <sub>RAL</sub>	$(2 + \text{WCP} + \text{WDA} + \text{WF} + \text{w})\text{T} - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65>	t <sub>CAS</sub>	$(1 + \text{WDA} + \text{WF})\text{T} - 10$		ns
$\overline{\text{CAS}}\text{-}\overline{\text{RAS}}$ precharge time	<66>	t <sub>CRP</sub>	$(1 + \text{WRP})\text{T} - 10$		ns
$\overline{\text{CAS}}$ hold time	<67>	t <sub>CSH</sub>	$(2 + \text{WRH} + \text{WDA} + \text{WF} + \text{w})\text{T} - 10$		ns
$\overline{\text{CAS}}$ precharge time	<71>	t <sub>CPN</sub>	$(2 + \text{WRP} + \text{WRH} + \text{w})\text{T} - 10$		ns
Delay time from $\overline{\text{RAS}}$ to column address	<76>	t <sub>RAD</sub>	$(0.5 + \text{WRH})\text{T} - 10$		ns
$\overline{\text{RAS}}\text{-}\overline{\text{CAS}}$ delay time	<77>	t <sub>RCD</sub>	$(1 + \text{WRH} + \text{w})\text{T} - 10$		ns
$\overline{\text{CAS}}$ precharge time	<81>	t <sub>CP</sub>	$(0.5 + \text{WCP} + \text{w})\text{T} - 10$		ns
High-speed page mode cycle time	<82>	t <sub>PC</sub>	$(2 + \text{WCP} + \text{WDA} + \text{WF} + \text{w})\text{T} - 10$		ns
$\overline{\text{RAS}}$ hold time for $\overline{\text{CAS}}$ precharge	<83>	t <sub>RHCP</sub>	$(2.5 + \text{WCP} + \text{WDA} + \text{w})\text{T} - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}$ ↓)	<85>	t <sub>WCH</sub>	$(1 + \text{WDA})\text{T} - 10$		ns
$\overline{\text{WE}}$ read time (from $\overline{\text{RAS}}$ ↑)	<88>	t <sub>RWL</sub>	WCP = 0 $(1.5 + \text{WDA} + \text{w})\text{T} - 10$		ns

**Remarks** 1. T = t<sub>CYK</sub>

2. w: The number of waits due to  $\overline{\text{WAIT}}$ .
3. WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. WDA: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. WRP: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
6. WCP: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
7. wf: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
8. i: The number of idle states that are inserted when a write cycle follows a read cycle.

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (2/3)

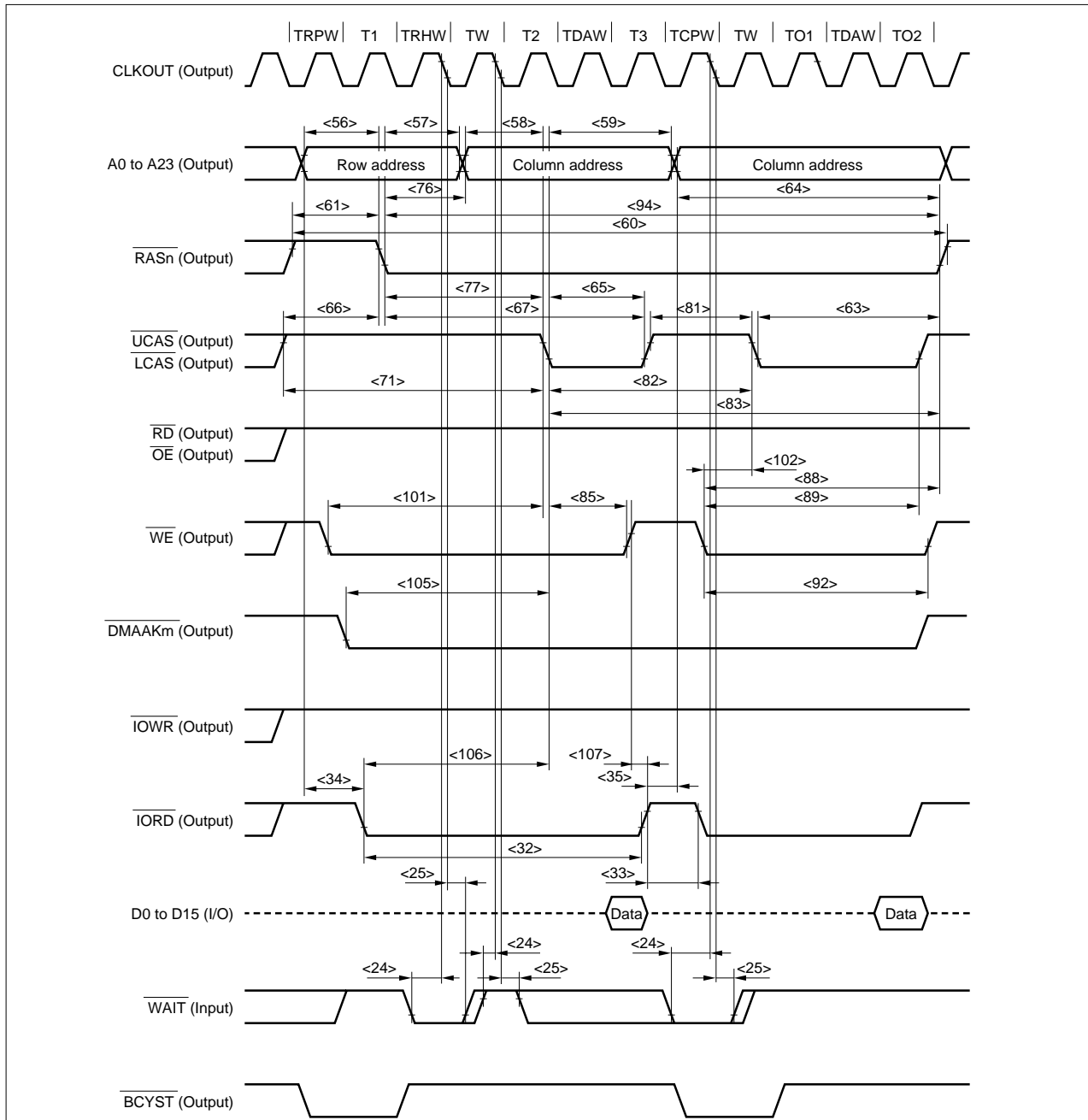
Parameter		Symbol	Condition	MIN.	MAX.	Unit
$\overline{WE}$ read time (from $\overline{CAS} \uparrow$ )		<89>	$t_{CWL}$	$W_{CP} = 0$	$(1 + W_{DA} + w)T - 10$	ns
$\overline{WE}$ pulse width		<92>	$t_{WP}$	$W_{CP} = 0$	$(1 + W_{DA} + w)T - 10$	ns
$\overline{RAS}$ pulse width		<94>	$t_{RASP}$		$(2.5 + W_{RH} + W_{DA} + W_F + w)T - 10$	ns
$\overline{WE}$ setup time (to $\overline{CAS} \downarrow$ )	Off-page	<101>	$t_{WCS1}$	$W_{CP} = 0$	$(1 + W_{RH} + W_{RP} + w)T - 10$	ns
	On-page	<102>	$t_{WCS2}$	$W_{CP} \geq 1$	$W_{CP}T - 10$	ns
Delay time from $\overline{DMAAKm} \downarrow$ to $\overline{CAS} \downarrow$		<105>	$t_{DDACS}$		$(1.5 + W_{RH} + w)T - 10$	ns
Delay time from $\overline{IORD} \downarrow$ to $\overline{CAS} \downarrow$		<106>	$t_{DRDCS}$		$(1 + W_{RH} + w)T - 10$	ns
Delay time from $\overline{WE} \uparrow$ to $\overline{IORD} \uparrow$		<107>	$t_{DWERD}$	$W_F = 0$	0	ns
				$W_F = 1$	$T - 10$	ns

**Remarks** 1.  $T = t_{CYK}$

2.  $w$ : The number of waits due to  $\overline{WAIT}$ .
3.  $W_{RH}$ : The number of waits due to the RHCxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).
4.  $W_{DA}$ : The number of waits due to the DACxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).
5.  $W_{RP}$ : The number of waits due to the RPCxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).
6.  $W_{CP}$ : The number of waits due to the CPCxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13).
7.  $W_F$ : The number of waits that are inserted for a source-side access during a DMA flyby transfer.
8.  $m = 0$  to 3



(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (3/3)



- Remarks**
1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).  
 Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1  
 Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1  
 Number of waits due to the DACxx bit of the DRCn register (TDAW): 1  
 Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1  
 Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0
  2. The broken lines indicate high impedance.
  3. n = 3 to 5, m = 0 to 3

(i) CBR refresh timing

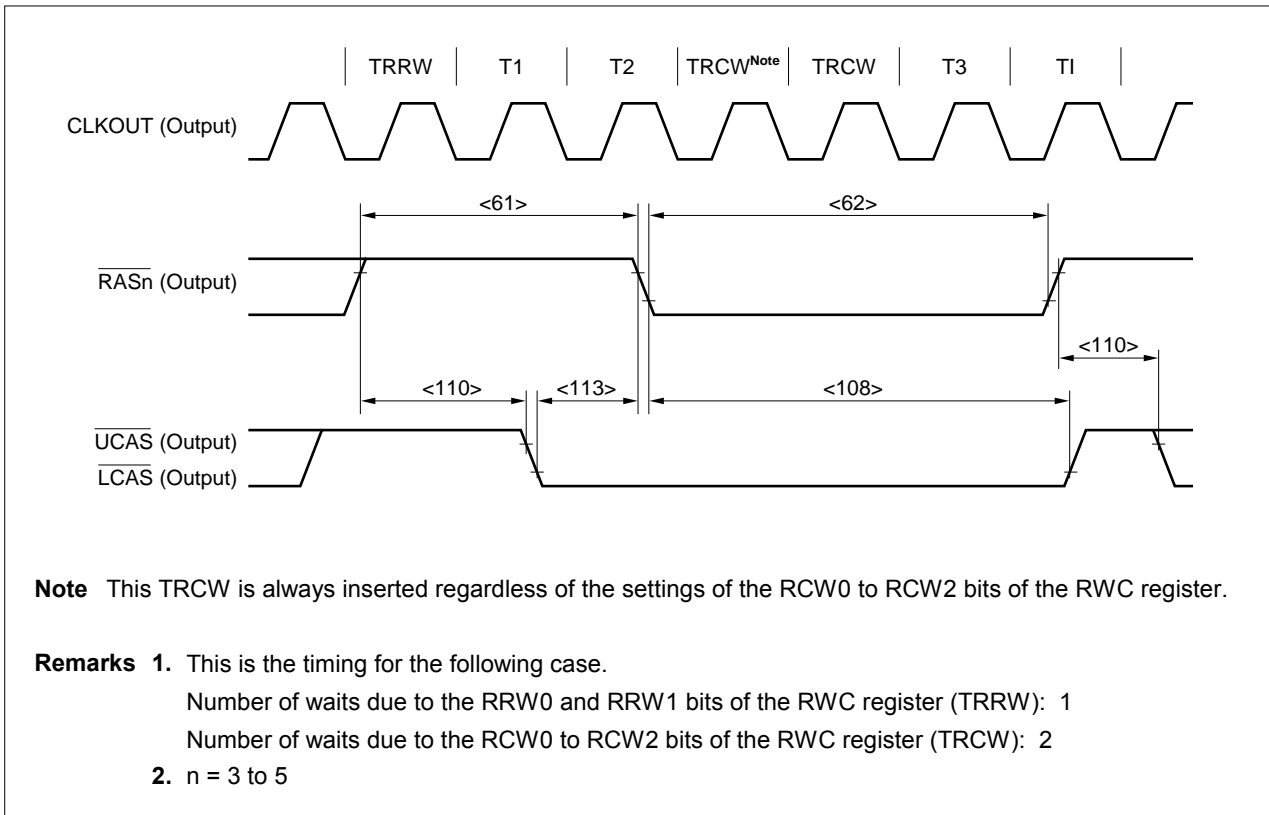
Parameter	Symbol	Condition	MIN.	MAX.	Unit
RAS precharge time	<61>	$t_{RP}$	$(1.5 + W_{RRW})T - 10$		ns
RAS pulse width	<62>	$t_{RAS}$	$(1.5 + W_{RCW}^{Note})T - 10$		ns
CAS hold time	<108>	$t_{CHR}$	$(1.5 + W_{RCW}^{Note})T - 10$		ns
RAS precharge CAS hold time	<110>	$t_{RPC}$	$(0.5 + W_{RRW})T - 10$		ns
CAS setup time	<113>	$t_{CSR}$	$T - 10$		ns

**Note** At least one clock cycle is inserted by default for  $w_{RCW}$  regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

**Remarks 1.**  $T = t_{CYK}$

**2.**  $w_{RRW}$ : The number of waits due to the RRW0 and RRW1 bits of the RWC register.

**3.**  $w_{RCW}$ : The number of waits due to the RCW0 to RCW2 bits of the RWC register.



**Note** This TRCW is always inserted regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

**Remarks 1.** This is the timing for the following case.

Number of waits due to the RRW0 and RRW1 bits of the RWC register ( $T_{RRW}$ ): 1

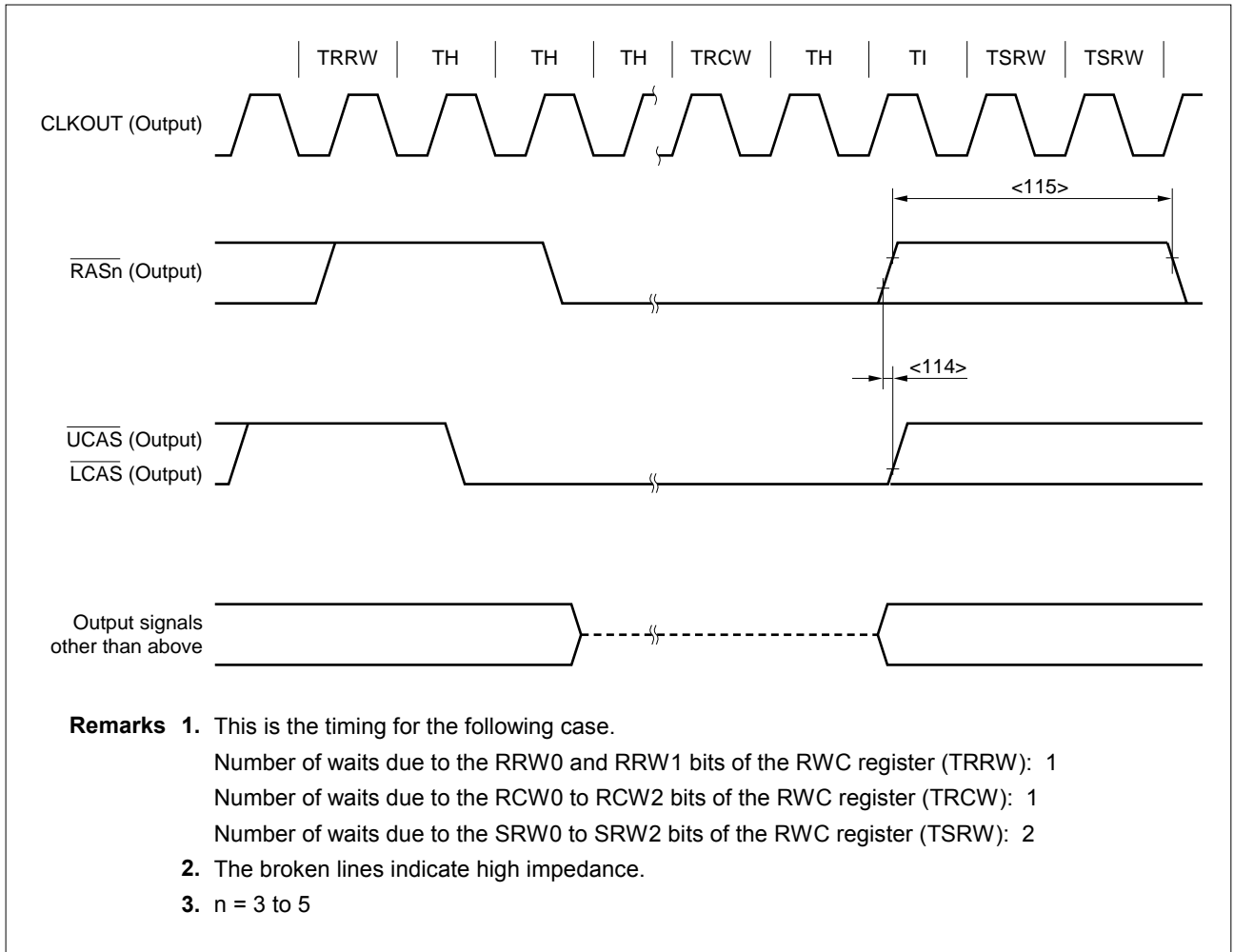
Number of waits due to the RCW0 to RCW2 bits of the RWC register ( $T_{RCW}$ ): 2

**2.**  $n = 3$  to  $5$

(j) CBR self-refresh timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
CAS hold time	<114>	t <sub>CHS</sub>	-5		ns
RAS precharge time	<115>	t <sub>RPS</sub>	(1 + 2 <sub>WSRW</sub> )T - 10		ns

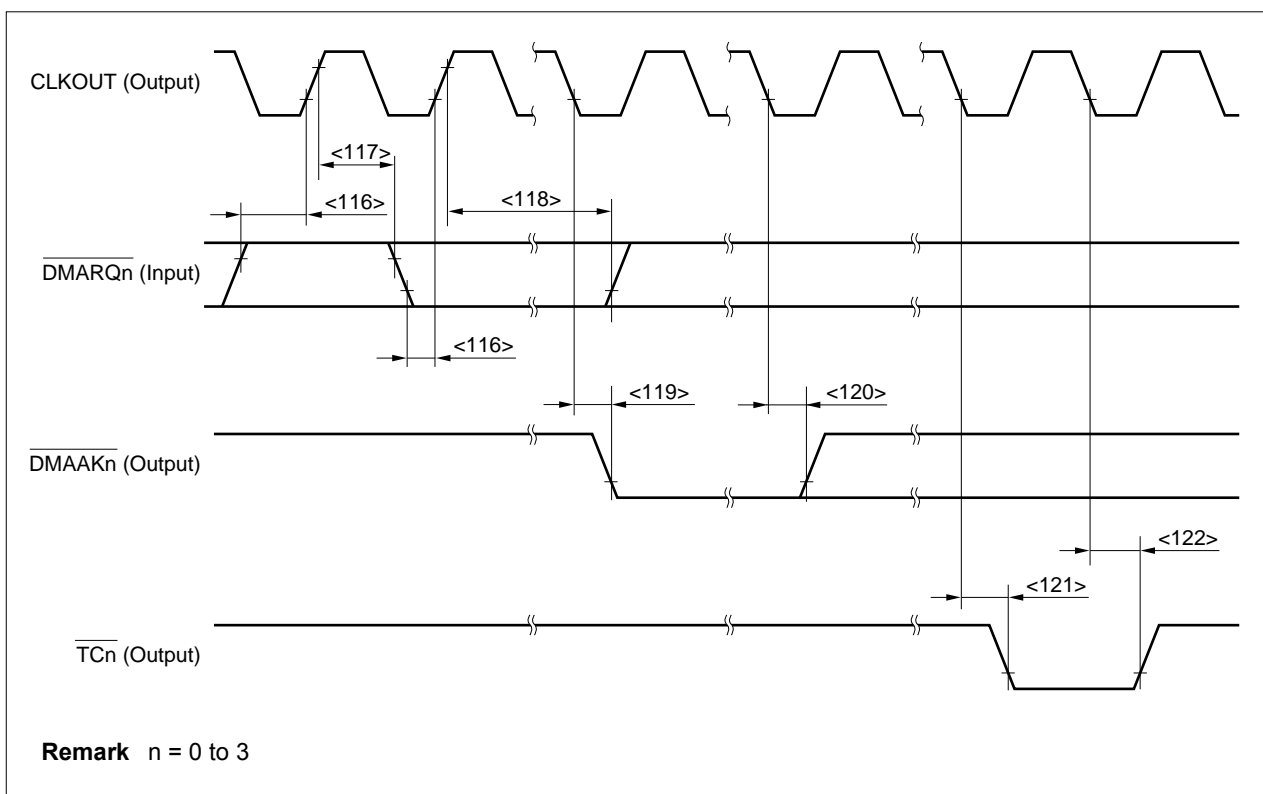
- Remarks**
1. T = t<sub>cyk</sub>
  2. <sub>WSRW</sub>: The number of waits due to the SRW0 to SRW2 bits of the RWC register.



(7) DMAC timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{DMARQn}}$ setup time (to CLKOUT ↑)	<116> $t_{\text{SDRK}}$		15		ns
$\overline{\text{DMARQn}}$ hold time (from CLKOUT ↑)	<117> $t_{\text{HKDR1}}$		2		ns
	<118> $t_{\text{HKDR2}}$	Until $\overline{\text{DMAAKn}} \downarrow$			ns
$\overline{\text{DMAAKn}}$ output delay time (from CLKOUT ↓)	<119> $t_{\text{DKDA}}$		2	10	ns
$\overline{\text{DMAAKn}}$ output hold time (from CLKOUT ↓)	<120> $t_{\text{HKDA}}$		2	10	ns
$\overline{\text{TCn}}$ output delay time (from CLKOUT ↓)	<121> $t_{\text{DKTC}}$		2	10	ns
$\overline{\text{TCn}}$ output hold time (from CLKOUT ↓)	<122> $t_{\text{HKTC}}$		2	10	ns

**Remark** n = 0 to 3



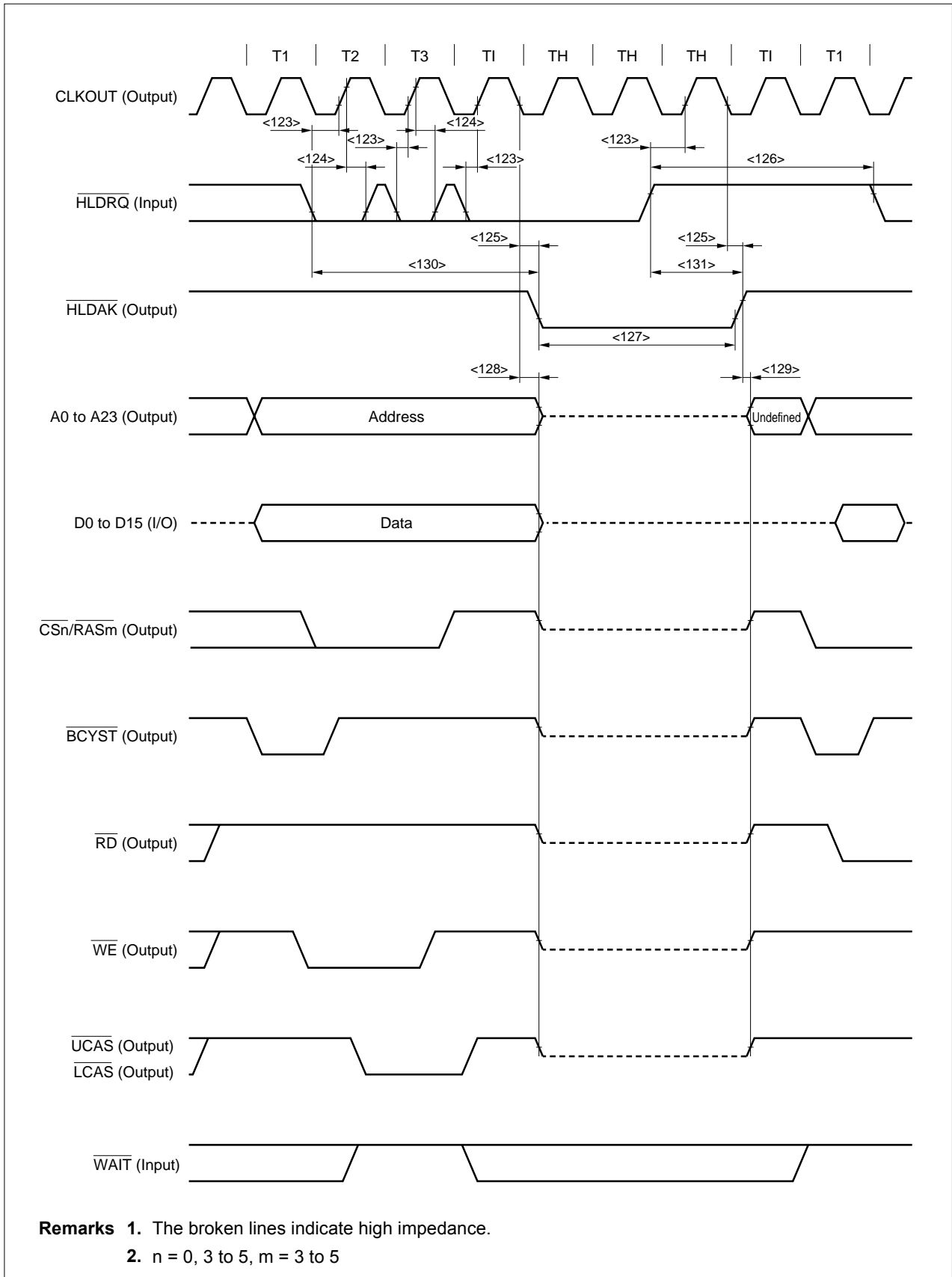
[MEMO]

(8) Bus hold timing (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT ↑)	<123> $t_{\text{SHRK}}$		15		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT ↑)	<124> $t_{\text{HKHR}}$		2		ns
Delay time from CLKOUT ↓ to $\overline{\text{HLDAK}}$	<125> $t_{\text{DKHA}}$		2	10	ns
$\overline{\text{HLDRQ}}$ high-level width	<126> $t_{\text{WHQH}}$		T + 17		ns
$\overline{\text{HLDAK}}$ low-level width	<127> $t_{\text{WHAL}}$		T - 8		ns
Delay time from CLKOUT ↓ to bus float	<128> $t_{\text{DKCF}}$			10	ns
Delay time from $\overline{\text{HLDAK}}$ ↑ to bus output	<129> $t_{\text{DHAC}}$		0		ns
Delay time from $\overline{\text{HLDRQ}}$ ↓ to $\overline{\text{HLDAK}}$ ↓	<130> $t_{\text{DHQA1}}$		2.5T		ns
Delay time from $\overline{\text{HLDRQ}}$ ↑ to $\overline{\text{HLDAK}}$ ↑	<131> $t_{\text{DHQA2}}$		0.5T	1.5T	ns

**Remark** T = t<sub>cyk</sub>

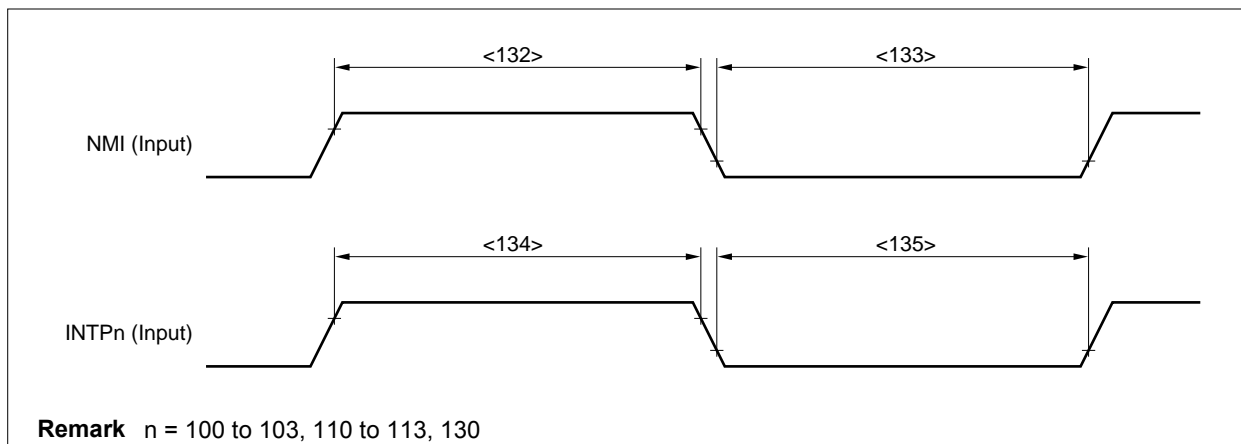
(8) Bus hold timing (2/2)



(9) Interrupt timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
NMI high-level width	<132> $t_{WNIH}$		500		ns
NMI low-level width	<133> $t_{WNIL}$		500		ns
INTPn high-level width	<134> $t_{WITh}$		$4T + 10$		ns
INTPn low-level width	<135> $t_{WITL}$		$4T + 10$		ns

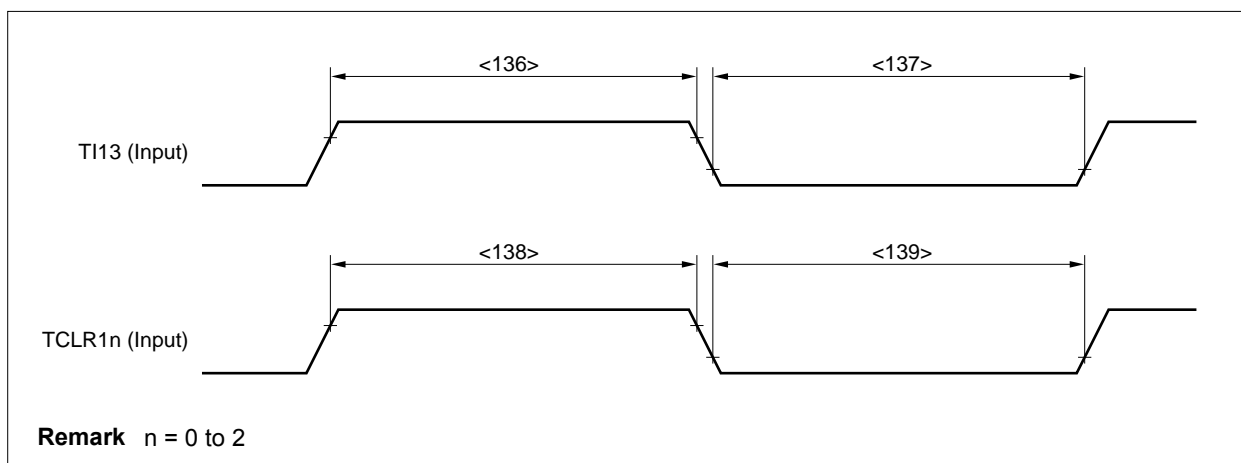
- Remarks** 1. n = 100 to 103, 110 to 113, 130  
 2. T = t<sub>cyk</sub>



(10) RPU timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
TI13 high-level width	<136> $t_{WTIH}$		$3T + 18$		ns
TI13 low-level width	<137> $t_{WTIL}$		$3T + 18$		ns
TCLR1n high-level width	<138> $t_{WTCH}$		$3T + 18$		ns
TCLR1n low-level width	<139> $t_{WTCL}$		$3T + 18$		ns

- Remarks** 1. n = 0 to 2  
 2. T = t<sub>cyk</sub>

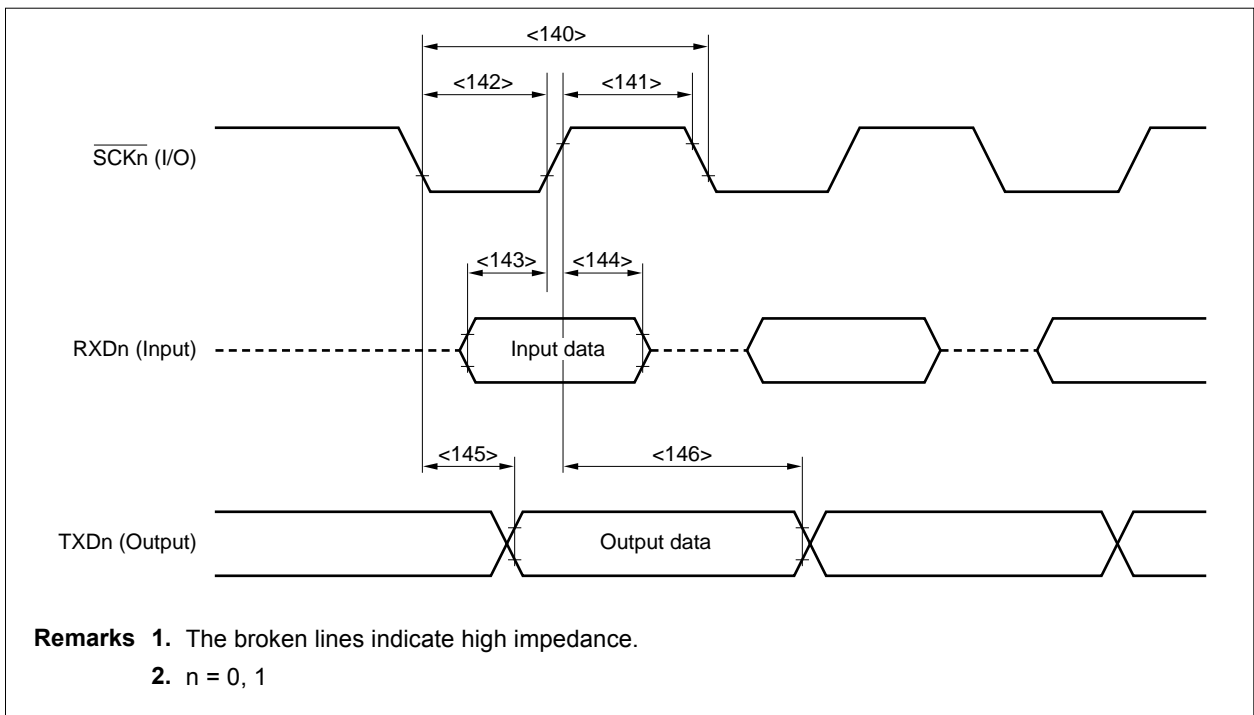




(11) UART0, UART1 timing (clock-synchronized or master mode only)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle	<140>	$t_{\text{CYSK0}}$	250		ns
$\overline{\text{SCKn}}$ high-level width	<141>	$t_{\text{WSK0H}}$	$0.5t_{\text{CYSK0}} - 20$		ns
$\overline{\text{SCKn}}$ low-level width	<142>	$t_{\text{WSK0L}}$	$0.5t_{\text{CYSK0}} - 20$		ns
RxDn setup time (to $\overline{\text{SCKn}} \uparrow$ )	<143>	$t_{\text{SRXSK}}$	30		ns
RxDn hold time (from $\overline{\text{SCKn}} \uparrow$ )	<144>	$t_{\text{HSKRX}}$	0		ns
TxDn output delay time (from $\overline{\text{SCKn}} \downarrow$ )	<145>	$t_{\text{DSKTX}}$		20	ns
TxDn output hold time (from $\overline{\text{SCKn}} \uparrow$ )	<146>	$t_{\text{HSKTX}}$	$0.5t_{\text{CYSK0}} - 5$		ns

Remark n = 0, 1



(12) CSI0, CSI1 timing

(a) Master mode

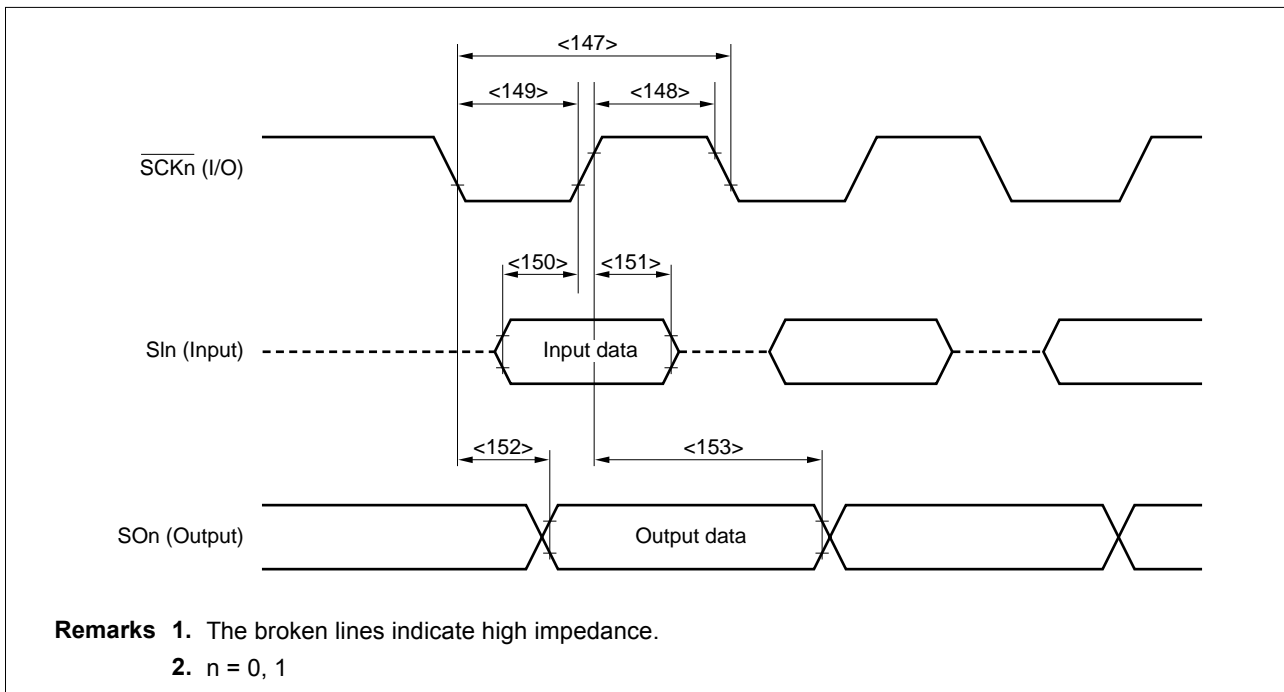
Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<147> $t_{CYSK1}$	Output	100		ns
$\overline{SCKn}$ high-level width	<148> $t_{WSK1H}$	Output	$0.5t_{CYSK1} - 20$		ns
$\overline{SCKn}$ low-level width	<149> $t_{WSK1L}$	Output	$0.5t_{CYSK1} - 20$		ns
SIn setup time (to $\overline{SCKn} \uparrow$ )	<150> $t_{SSISK}$		30		ns
SIn hold time (from $\overline{SCKn} \uparrow$ )	<151> $t_{HSKSI}$		0		ns
SOn output delay time (from $\overline{SCKn} \downarrow$ )	<152> $t_{DSKSO}$			20	ns
SOn output hold time (from $\overline{SCKn} \uparrow$ )	<153> $t_{HSKSO}$		$0.5t_{CYSK1} - 5$		ns

Remark n = 0, 1

(b) Slave mode

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<147> $t_{CYSK1}$	Input	100		ns
$\overline{SCKn}$ high-level width	<148> $t_{WSK1H}$	Input	30		ns
$\overline{SCKn}$ low-level width	<149> $t_{WSK1L}$	Input	30		ns
SIn setup time (to $\overline{SCKn} \uparrow$ )	<150> $t_{SSISK}$		10		ns
SIn hold time (from $\overline{SCKn} \uparrow$ )	<151> $t_{HSKSI}$		10		ns
SOn output delay time (from $\overline{SCKn} \downarrow$ )	<152> $t_{DSKSO}$			30	ns
SOn output hold time (from $\overline{SCKn} \uparrow$ )	<153> $t_{HSKSO}$		$t_{WSK1H}$		ns

Remark n = 0, 1



Remarks 1. The broken lines indicate high impedance.  
2. n = 0, 1

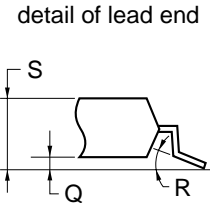
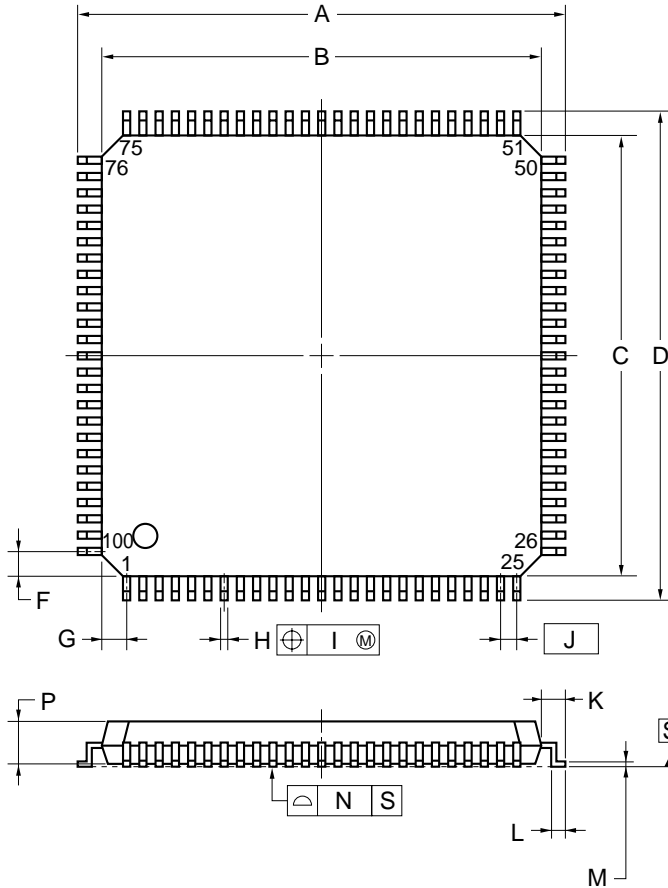
**A/D Converter Characteristics** ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = CV_{DD} = 3.0$  to  $3.6$  V,  $HV_{DD} = 5.0$  V  $\pm 10\%$ ,  $V_{SS} = 0$  V,  $HV_{DD} - 0.5$  V  $\leq AV_{DD} \leq HV_{DD}$ , output pin load capacitance:  $C_L = 50$  pF)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	–		10			bit
Overall error	–				$\pm 4$	LSB
Quantization error	–				$\pm 1/2$	LSB
Conversion time	$t_{CONV}$		5		10	$\mu\text{s}$
Sampling time	$t_{SAMP}$		Conversion clock <sup>Note</sup> /6			ns
Zero scale error	–				$\pm 4$	LSB
Scale error	–				$\pm 4$	LSB
Linearity error	–				$\pm 3$	LSB
Analog input voltage	$V_{IAN}$		-0.3		$AV_{REF} + 0.3$	V
Analog input resistance	$R_{AN}$			2		$M\Omega$
$AV_{REF}$ input voltage	$AV_{REF}$	$AV_{REF} = AV_{DD}$	4.5		5.5	V
$AV_{REF}$ input current	$AI_{REF}$				2.0	mA
$AV_{DD}$ current	$AI_{DD}$				6	mA

**Note** Conversion clock is the number of clocks set by the ADM1 register.

4. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	0.22 <sup>+0.05</sup> <sub>-0.04</sub>
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	0.17 <sup>+0.03</sup> <sub>-0.07</sub>
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	3° <sup>+7°</sup> <sub>-3°</sub>
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

## 5. RECOMMENDED SOLDERING CONDITIONS

TBD

## NOTES FOR CMOS DEVICES

**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Reference materials** Electrical Characteristics for Microcomputer (U15170J<sup>Note</sup>)

**Note** This document number is that of Japanese version.

**The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.**

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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