12-ns DG611 Switch Family Combines Benefits of CMOS and DMOS Technologies

The DG611, DG612, and DG613 are extremely low-power, high-speed analog switches designed to optimize circuit performance in high-speed switching applications. Each of these devices integrates low-power CMOS drivers with high-speed DMOS FETs. The resulting switches boast some remarkable features: high speed, low power, low on-resistance, low leakage, low charge injection and low channel capacitance, all on the same device.

By combining both CMOS and DMOS technologies on a single chip, the DG61X family avoids the tradeoffs inherent in other high-speed analog switches, such as high power consumption, high on-resistance, and high channel capacitance. The DG61X family is likewise superior to DMOS FETs, which are fast but highly sensitive to electrostatic discharge, as well as requiring external drivers built with a number of external discrete components.

This application note describes the new DG61X devices in detail and provides a series of application hints which will help you take full advantage of this fast new family in your designs.

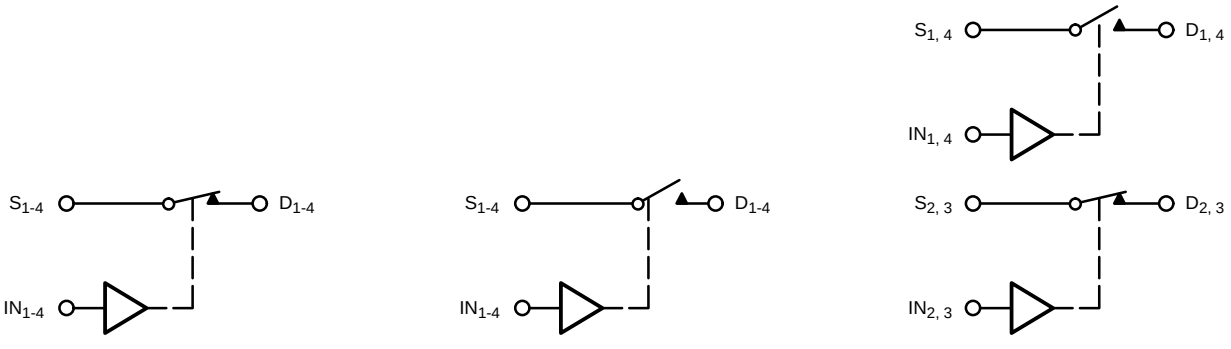
Circuit Description

Each device has four independently controlled switches. The DG611 and DG612 respond to opposite control logic. The DG611 has a normally closed (NC) function while the DG612 is a normally open (NO) device.

The DG613 offers a complementary function. It contains two NO and two NC switches. This versatile device can be configured as two single-pole single-throw (SPDT), one double-pole double-throw (DPDT), a “T” switch, two “L” switches, and so forth.

As illustrated in Figure 2, each analog switch channel consists of an input stage, followed by a level translator, a driver stage, and an n-channel MOSFET.

The input stage is a CMOS inverter powered from V_L. V_L is the logic power supply voltage (normally +5 V). As with any classic CMOS inverter, control input pin impedance is very high and essentially equivalent to the logic input pin capacitance (approximately 5 pF). This pin does not draw current (except for leakage) when in a steady state. To change states it is necessary to charge or discharge this input capacitance, which requires a short current pulse from the control logic gate.



All Switches Shown for Logic “0” Inputs.

FIGURE 1. Functional Diagrams (Typical Switch)

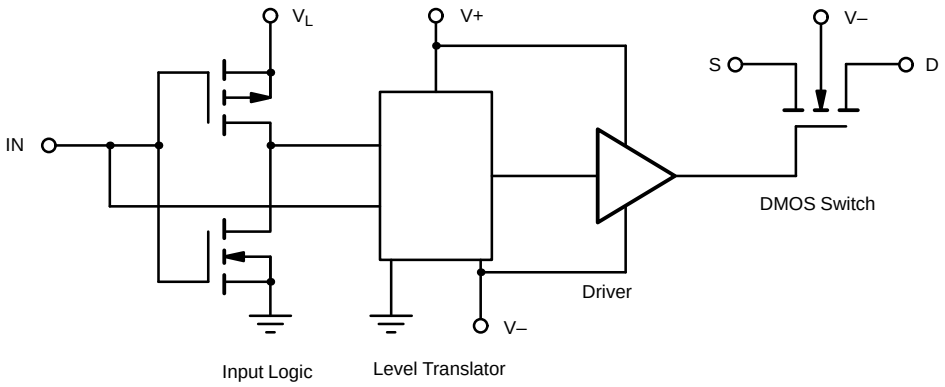


FIGURE 2. Typical Channel Block Diagram

The level translator provides level shifting of the 0 to 5 V logic input to the V+ to V– voltage excursions needed to control the MOSFET switch.

The driver stage acts as a buffer and provides current amplification to quickly charge/discharge the MOSFET gate, thus quickly turning the switch ON or OFF.

The switching element is an n-channel double-diffused enhancement-mode MOSFET. DMOS FETs achieve very low inter-electrode capacitance and high speed, thanks to their lateral construction. To turn the switch ON, a voltage equal to V+ is applied to the FET's gate. This enhances the channel into conduction.

The source and Drain terminals can stand up to 16 V with respect to the substrate voltage (V–).

ESD protection diode pairs are connected from each logic input, source, and drain pin to the V+ and V- power supply rails.

Optimized Characteristics

The DG611 family was designed to optimize the parameters which are most important in high-speed applications.

Switching Speed

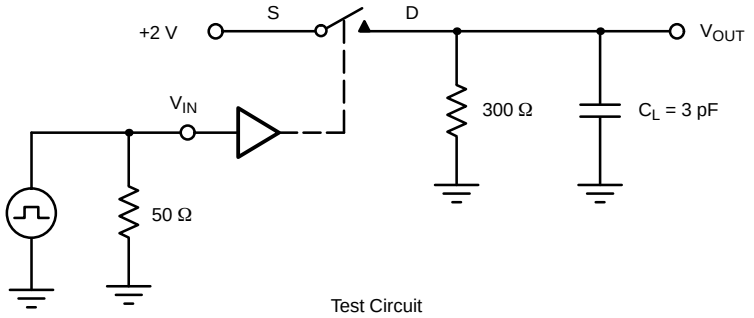
Discrete DMOS FETs such as the SD210 or SD5000 are well known for their fast switching speeds. In fact, both specify a $t_{d(on)}$ of 1 ns max. The DG611 family combines fast DMOS switching elements with a low-power CMOS driver. These devices are so fast that measuring their speed at final test becomes a challenge. ATE limitations (lead inductances/capacitances, generator's rise and fall times) conspire to slow things down. This is why the t_{ON}/t_{OFF} specifications on the data sheet are so loose (35 ns max).

A typical device in a typical application is much faster than the data-sheet specifications would indicate. A bench test circuit reduced test fixture parasitics, while a low capacitance (3 pF) FET probe was used to monitor the output voltage. Figure 3 shows that before the output starts to change there was a propagation delay through the driver of about 8 ns. Once the FET starts to turn on, the output voltage rises very fast. The rise time was approximately 2 ns. Total t_{ON} (50% Vin to 90% Vout) was approximately 12 ns. Similarly at turn-off the driver's propagation delay appeared to be about 8 ns, the fall time was about 5 ns. t_{OFF} (50% V_{IN} to 90% V_{OUT}) was about 7 ns.

Reduced Switching Transients

By adding two dynamic compensation capacitors to the output driver stage, charge injection glitches have been virtually eliminated. For comparison purposes, Figure 4 illustrates the typical charge injection characteristics for two Vishay Siliconix' high-speed analog switches: DG271 and DG611. Note how flat the DG611 characteristic is. This guarantees low charge injection regardless of analog signal voltage.

Charge injection causes switching glitches both at turn-on and at turn-off times. To evaluate and compare the switching glitches produced by the DG611, the test circuit of Figure 5 was built. A 4-Vp-p triangular bipolar wave form was fed to the switch input. On this wave form we wanted to cut some 0-V notches as commanded by a pulse train. 100-ns pulses were used to interrupt signal flow twice in every period letting the output voltage to fall to 0 V.



Test Circuit

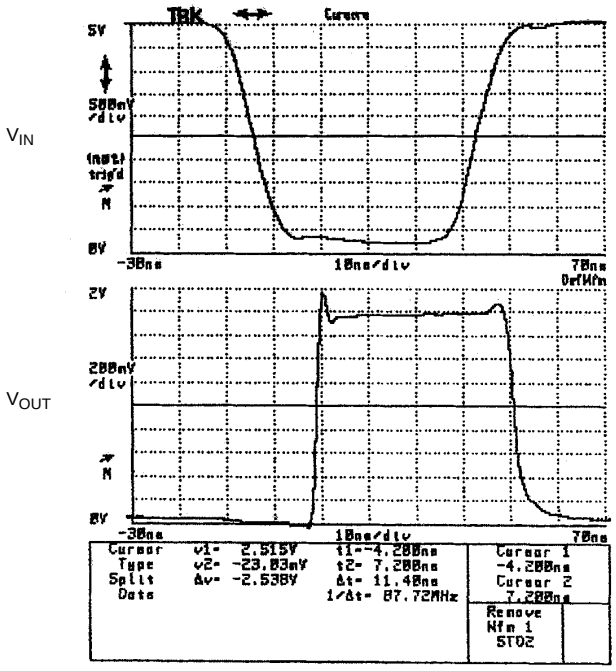


FIGURE 3. Bench Test Switching Times Are Faster Than Data Sheet Limits

As seen in Figure 6, there were significant differences between the DG271 and the DG611 output wave forms. First, the DG611 considerably reduced switching glitches. Some spikes went from 1 V to 0.2 V, a fivefold improvement. Second, the faster DG611 reduced output delays and produced more consistent notch widths.

For general purpose switches, it is customary to assume that all charge injection is due to capacitive coupling from the output driver into the analog channel. At the low Qinj levels achieved by the DG61X family, even the spurious capacitance (due to pin proximity from the logic control pin to the adjacent drain pin) will contribute a significant amount of charge. For this reason, it is possible to get minimal glitches by applying the input signal to the drain pin and using the source pin for the output.

On-Resistance

A low on-resistance switch reduces measurement errors and helps to achieve fast settling times in test equipment and data acquisition systems. It is also useful in reducing insertion loss when switching RF or video signals. The DG611 family specifies a typical $r_{DS(on)}$ of 18 Ω. This is one of the lowest values among high-speed analog switches. In order to reduce parasitic capacitances, the DG611 uses an n-channel enhancement mode MOSFET for the switch element. Consequently, its on-resistance increases as the channel voltage increases. Eventually, as V_S approaches V+ the n-channel MOSFET loses its enhancement voltage (V+) -V_S and turns off.

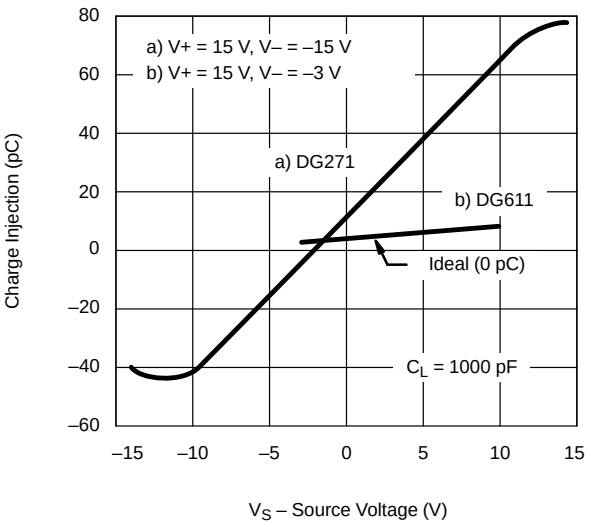


FIGURE 4. The DG611 Charge Injection Characteristic Shows a Dramatic Improvement Over That of the DG271

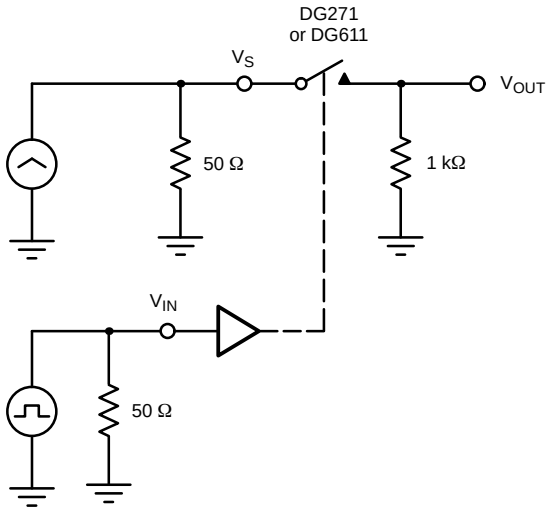
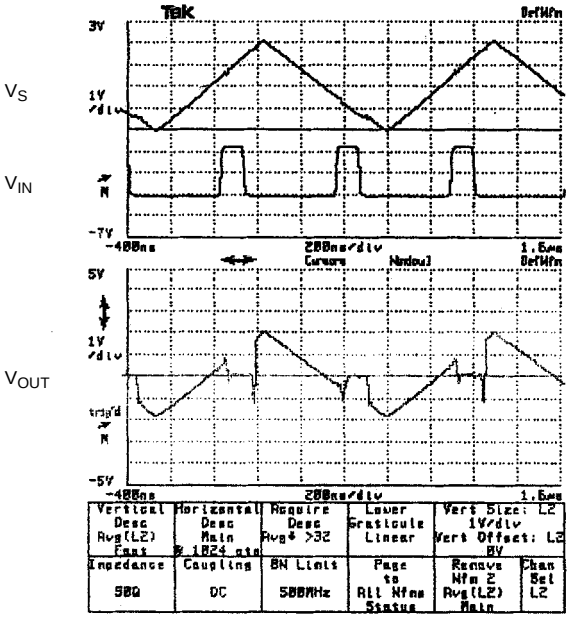
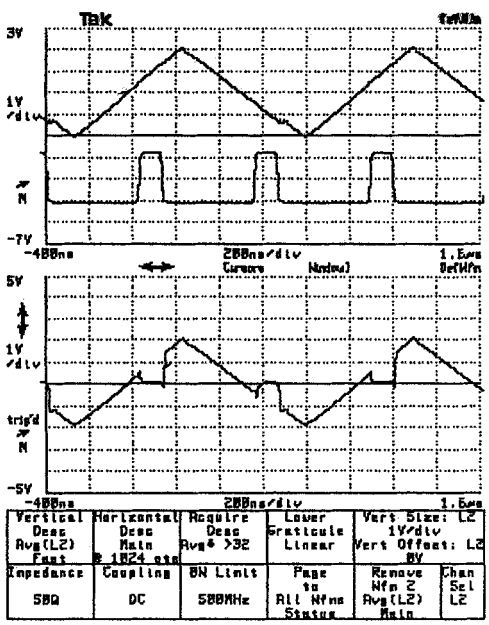


FIGURE 5. Switching Spikes Evaluation Circuit



a) Using DG271



a) Using DG611

FIGURE 6. The DG611 Significantly Improves the Output Wave Form

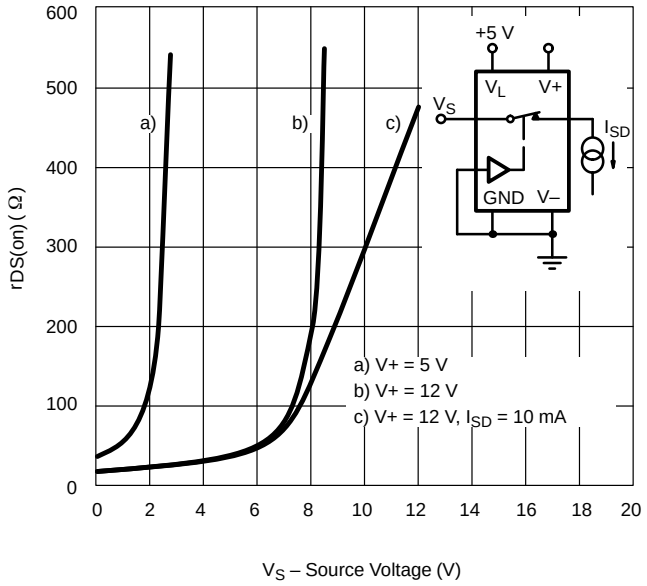


FIGURE 7. Typical $r_{DS(on)}$ Characteristics

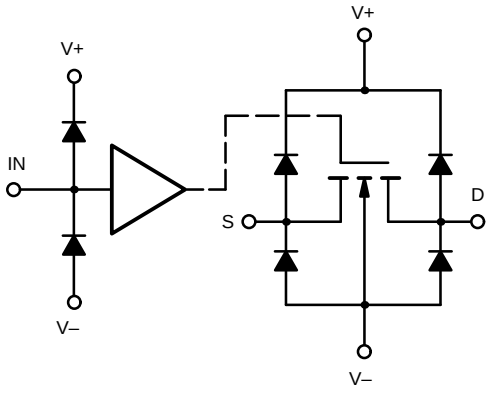


FIGURE 8. ESD Protection Diodes are Located at all Control and Switch Pins

Figure 7 illustrates typical on-resistance curves. Curve (a) represents single 5-V operation. Assuming a maximum acceptable $r_{DS(on)}$ value of 200 Ω, the usable analog signal range goes from 0 V to slightly over 2 V. Curve (b) shows operation with V+ = 12 V. Now the usable signal range has increased to 8 V. If you want to operate in the flat, low-resistance part of the curve, you may want to limit your analog signal to no more than 6 V. Curve (c) was generated using a –10-mA I_D current. Note that when V_S = 12 V, it still shows an $r_{DS(on)}$ = 480 Ω. To sink 10 mA, V_D has gone down to 7.2 V, and this creates a partial channel enhancement.

ESDS (ESD Sensitivity)

By incorporating a CMOS driver in front of the DMOS FET, direct access to the DMOS gate has been eliminated. By itself, this goes a long way to reduce ESD sensitivity. Additional ESD protection diodes have been added to the source and drain pins. Nevertheless, to maintain high speed, a compromise between ESD protection, speed, on-resistance, and on-capacitance had to be reached. This means that the protection diodes are relatively small and protect only up to about 500 V. To prevent damage from high-energy electrostatic fields, anti-static handling precautions must be observed at all times.

Applications

Following is a collection of practical application hints and design ideas intended to help you design with the DG61X family.

High-Speed 8-Channel Analog Multiplexer

If you are designing a high-speed data acquisition system, then you will need a very fast analog multiplexer. A fast multiplexer like the DG408 specifies a typical transition time of 160 ns. By using the DG611 to make the multiplexer shown in Figure 9, you will achieve transition times in the 30-ns range, a sixfold speed improvement. This added speed will allow you to achieve sampling rates in excess of 3 MHz, as demonstrated below.

For an 8-channel multiplexer the maximum sampling rate is given by:

$$f_S = \frac{1}{8 \times (t_{SETTLING} + t_{TRANS})} \quad (1)$$

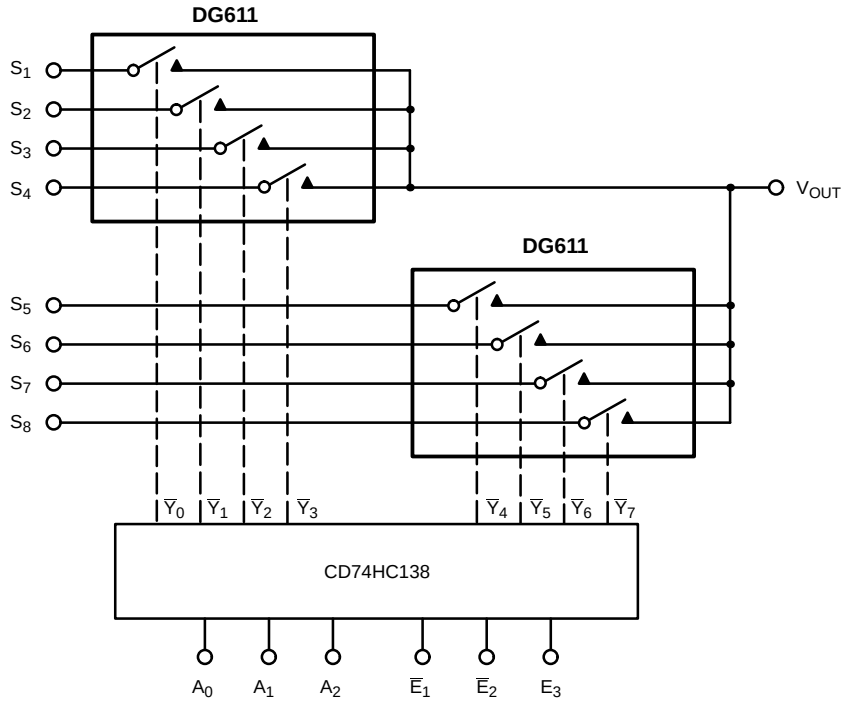
where $t_{SETTLING} = N \times r_{DS(on)} \times C_{(on)}$ (2)

for an accuracy of 0.01% (12 bits) N = 9.

For small signals, let us assume that typical $r_{DS(on)}$ = 18 Ω

The output node capacitance is given by:

$C_{(on)} = 1\ C_{D(on)} + 7\ C_{D(off)} = 10\ pF + 7 \times 2\ pF = 24\ pF$



Inputs						On Switch
Enable			Address			
E_3	$\overline{E}_2$	$\overline{E}_1$	A_2	A_1	A_0	
X	X	H	X	X	X	None
L	X	X	X	X	X	None
X	H	X	X	X	X	None
H	L	L	L	L	L	1
H	L	L	L	L	H	2
H	L	L	L	H	L	3
H	L	L	L	H	H	4
H	L	L	H	L	L	5
H	L	L	H	L	H	6
H	L	L	H	H	L	7
H	L	L	H	H	H	8

H = High Level, L = Low Level
X = Don't Care

FIGURE 9. High-Speed 8-Channel Multiplexer Capable of 3-MHz Sampling Rates

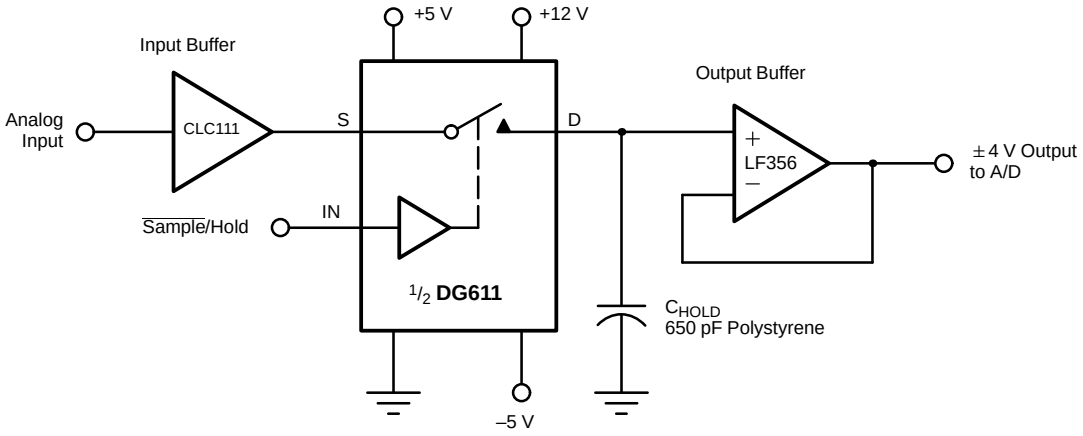


FIGURE 10. High-Speed Open-Loop Sample-and-Hold

Replacing into equation (1):

$$f_S = \frac{1}{8(9 \times 18\ \Omega \times 24\ pF + 30\ ns)} = 3.7\ MHz$$

An added benefit of this circuit is its improvement of overall accuracy by isolating the analog and (usually noisy) digital grounds. This is because the DG611 CMOS input stage has a high noise immunity, allowing for differences of up to ±1 V between the analog and digital grounds.

Sample-and-Hold Circuits

Data acquisition systems use sample-and-holds to "freeze" fast changing analog signals so they can be presented to an A/D converter for digitization. Accurately acquiring and holding the signal amplitude is critical to system performance. Figure 10 shows a basic open-loop sample-and-hold circuit. When the switch opens, a sample is stored on the hold capacitor.

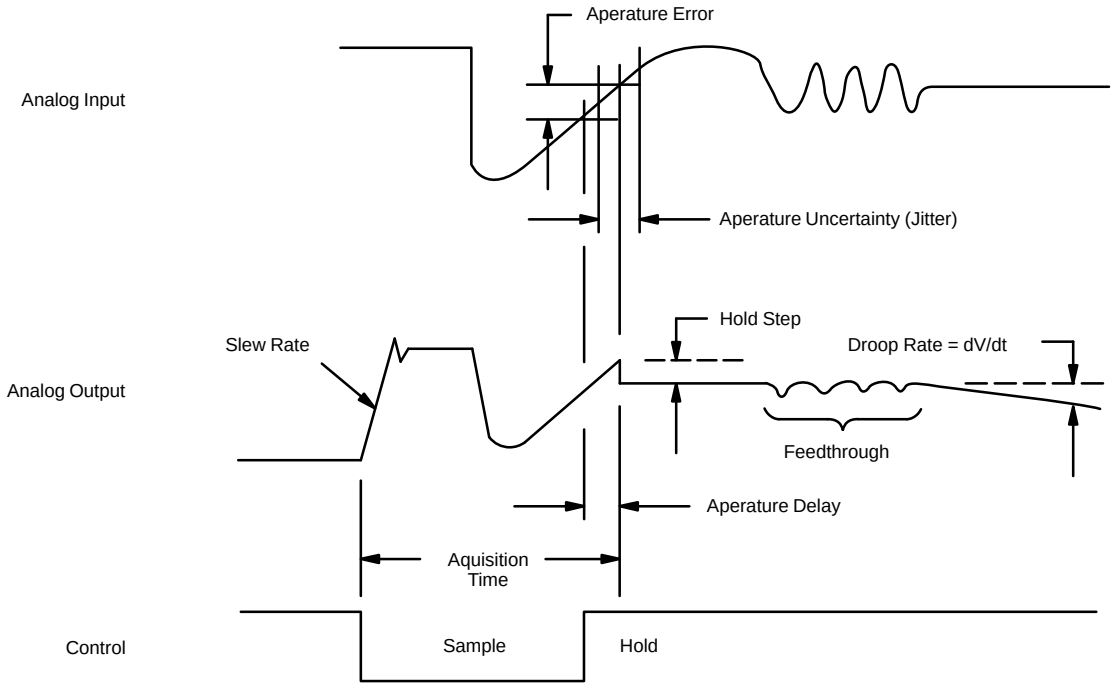


FIGURE 11. Error Sources in Sample-and-Hold Circuits

Because of non-ideal component characteristics, there are many sources of error in a sample-and-hold circuit. Figure 11 illustrates the most important ones. Table 1 lists these error sources and shows how the DG611 characteristics reduce those errors and improve overall circuit performance.

Figure 12 shows a closed loop sample-and-hold circuit. When SW1 and SW2 are closed, the output buffer is forced to track the analog input with a high degree of accuracy. SW3 improves acquisition time by letting the input buffer follow the input signal even during the hold periods. This circuit achieves high speed and high accuracy.

Programmable Low-Pass Filter

Many active filter implementations can be made programmable by using analog switches to select different component values into the circuit. Figure 13 illustrates a low-pass filter where a single DG613 is used to change the corner frequencies from 300 kHz to 400 kHz by selecting one of two resistor pairs. Keeping the input and feedback resistor values equal maintains unity gain. The DG613s low parasitic capacitances improve frequency response and permit operation at higher frequencies.

Switched-Capacitor Filters

Switched-capacitor filters (SCFs) offer high accuracy and excellent temperature stability. In addition, their cutoff frequencies are programmable over a wide range by simply changing the clock frequency.

Highly efficient audio frequency SCFs have been commercially available for several years, but since their sampling clocks need to be 25 to 100 times the signal frequency, they have been limited to applications in the 30- to 50-kHz range.

TABLE 1

Error Source	DG611 Parameter	Benefit
Acquisition Time	$r_{DS(on)}$ = 18 Ω $t_{(on)}$ = 12 ns	Faster sampling,settling times
Aperature Delay	$t_{(off)}$ = 8 ns	Minimal turn-off delay
Aperature Uncertainty	$t_{(off)}$ = 8 ns	Consistent propagation delay
Hold Step	ΔQ = 3 pC	Minimal switching glitches
Feed Through	Off Isolation = 74 dB @ 5 MHz	Low capacitive coupling
Droop Rate	$I_{D(off)}$ = 0.25 nA	Guaranteed low leakages

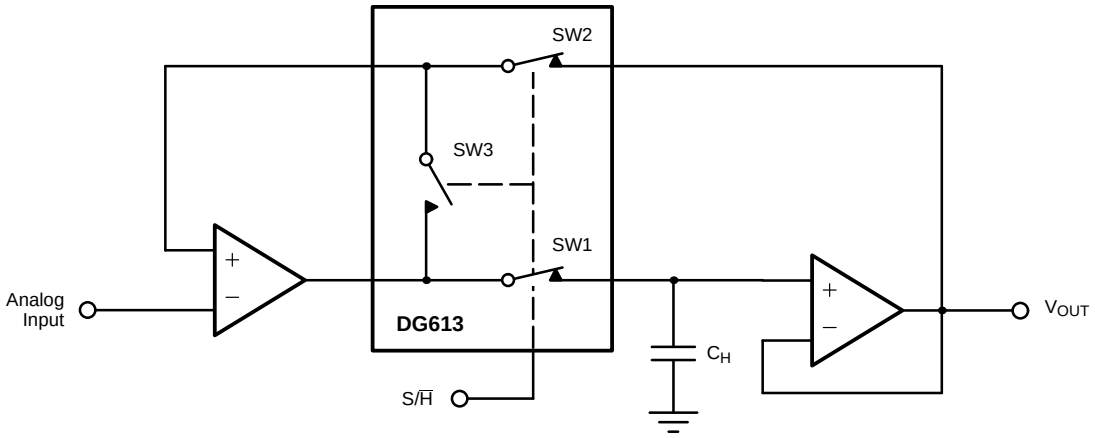


FIGURE 12. Fast and Accurate Closed-Loop Sample-and-Hold

Thanks to its high speed, low $r_{DS(on)}$ and low capacitances, the DG611 family makes it possible to implement SCFs with cutoff frequencies in the 1-MHz range. These higher frequencies are suitable for applications in the radio IF range (400-500 kHz). Using high-speed Op Amps and chip resistors it is possible to implement these SCFs in small hybrids.

The advantage of an RF SCF is that the filter's characteristics can be digitally controlled to adapt to the instantaneous bandwidth of the desired signal.

Figure 14(a) illustrates a simple low pass filter and its frequency response 14(b). Figure 14(c) is an SCF implementation that uses an inverting switched-capacitor integrator approach.

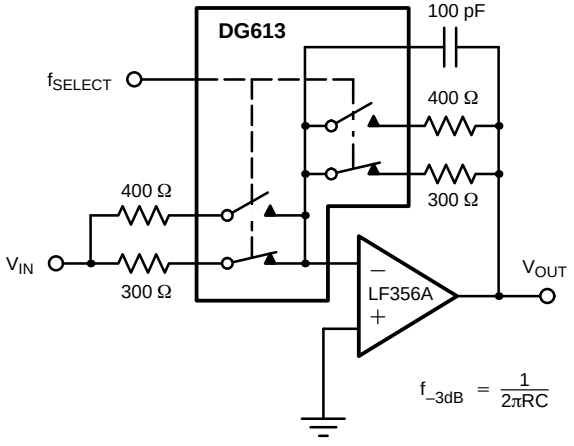


FIGURE 13. Programmable Low-Pass Filter

Video Overlaying

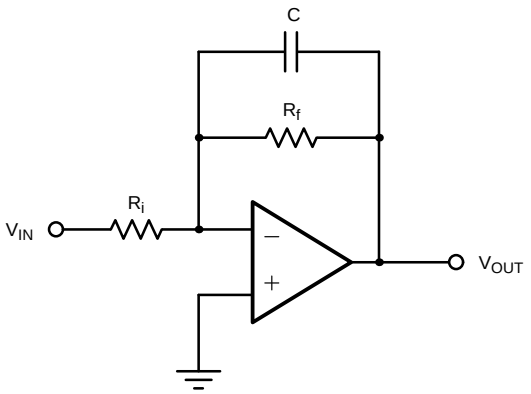
An inexpensive NTSC video titler can be implemented by superimposing the output of a character generator on a standard composite video background. A high-speed switch like the DG613 is used to select certain pixel groups from one of the two available sources during each horizontal line sweep. The same principle can be used to combine two video signals into a single image (i.e. blue background.) Both video sources must be sync-locked.

An advantage of the DG61X family is that its low charge injection eliminates switching noise that could appear as halos or shadows around the superimposed image. It is worth noting that if you disregard the propagation delay in the driver stages, the effective switching transition time from one video signal to the other is well below 5 ns!

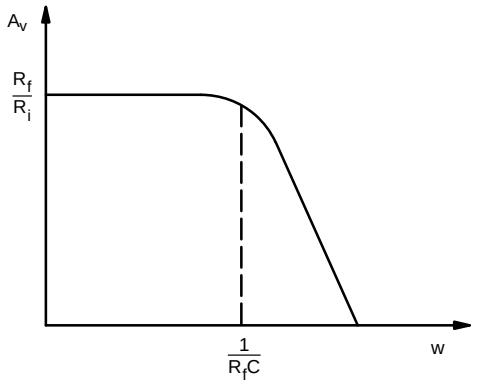
Figure 15 illustrates a basic pixel-rate switch circuit. Each incoming signal arrives to its own 75-Ω termination resistor. The DG613 is configured for a single-pole double-throw function and selects one of the two signals at a time. The CLC410 amplifier drives a 75-Ω back- terminated output line.

A back-terminated line provides impedance matching and eliminates any reflections caused by possible impedance disturbances on the transmission line. Connectors, transitions from coax cable to PC board traces, and transitions from board traces to IC package lead will cause slight impedance mismatches.

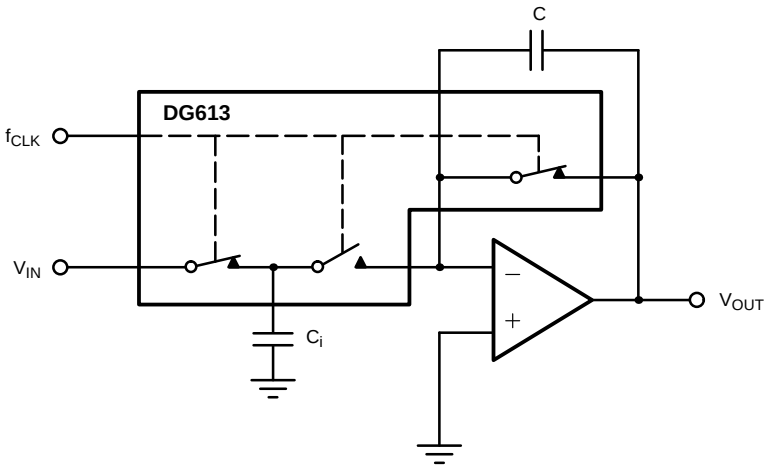
The output amplifier must have a gain of 2 (6 dB) since the back-termination resistor will introduce a 6-dB loss.



a) Active Low Pass Filter



b) Frequency Response



c) SCF Implementation

$$R_i = \frac{1}{C_i \times f_{CLK}} \qquad R_f = \frac{1}{C \times f_{CLK}}$$

FIGURE 14. Low Pass Switched-Capacitor Filter

Video DC Restoration

Sending video signals over long cable runs often causes dc offsets and may add power-line hum. When this is the case, a back porch clamp (or dc restorer) is used to return the waveform to its proper dc reference level. The same principle is used for picture brightness adjustments.

GaAs Driver

The DG611 family is capable of switching RF signals up into the UHF frequencies. The DG613 is ideal for switching RF in the GHz region when, as shown in Figure 15, it is used to drive GaAs FET switches. This circuit benefits from the DG613s high speed, low capacitances, and low power characteristics.

DAC Deglitcher

All DACs produce output glitches when the digital input data changes. The worst spikes occur when the MSB changes state, and at one-fourth and three-fourths of full scale. A deglitcher circuit as shown in Figure 18 acts as a track-and-hold and removes the output glitches. The DG611 is ideal because of its low charge injection and high speed.

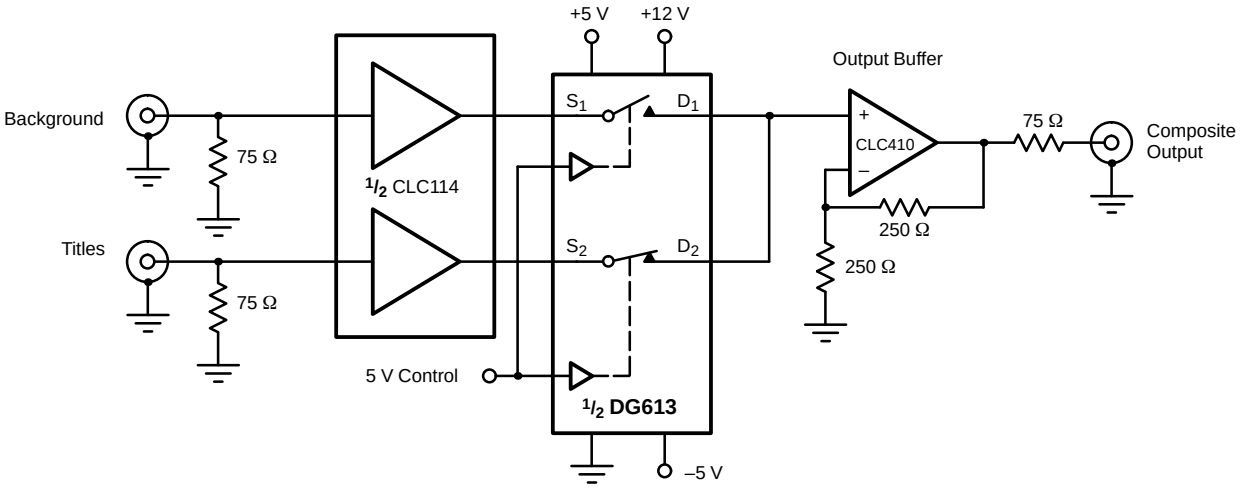


FIGURE 15. Pixel-Rate Switch Creates Video Overlays

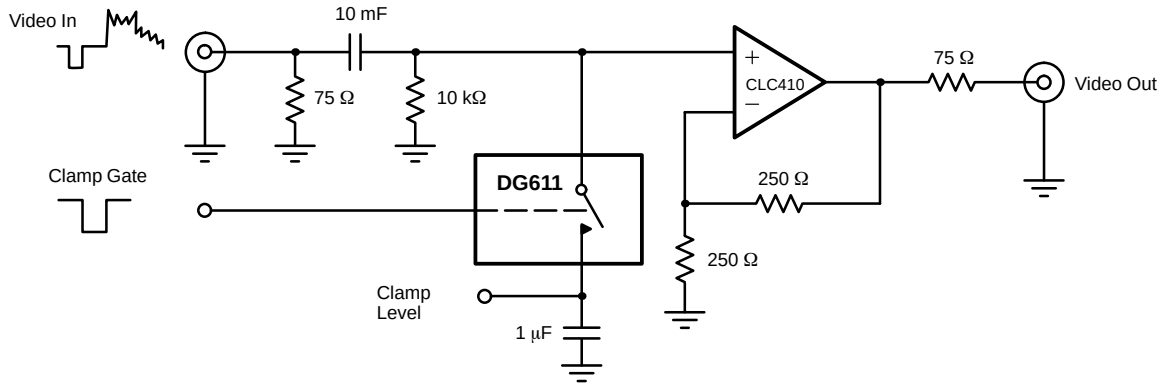


FIGURE 16. Fast Switch Restores Back Porch to Proper dc Level

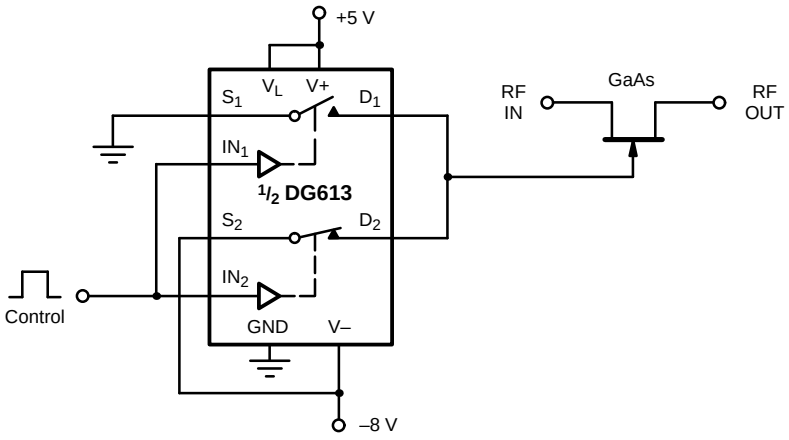
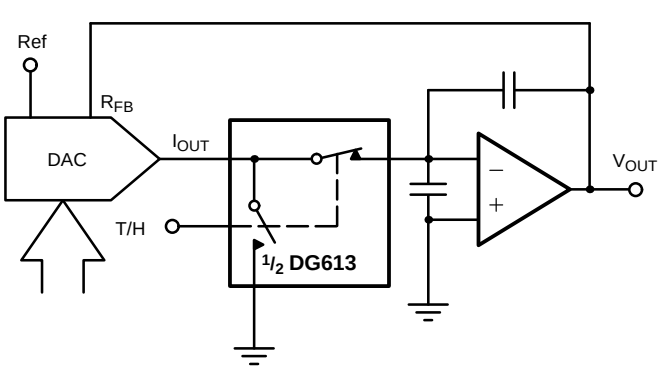


FIGURE 17. High-Speed GaAs FET Driver Saves Power



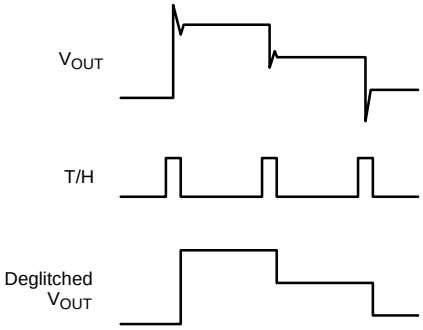
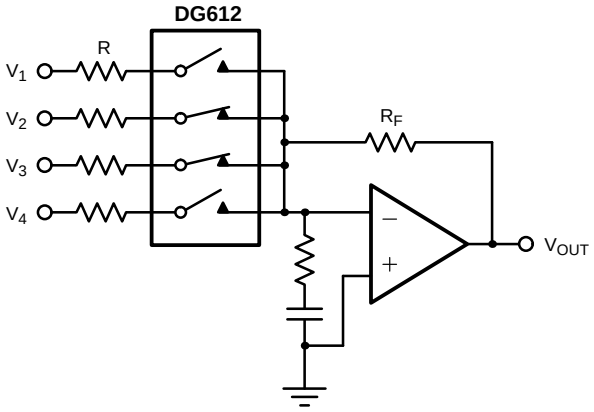


FIGURE 18. DAC Deglitcher



$$V_{OUT} = -\frac{R_F}{R}(V_1 + ... + V_4)$$

FIGURE 19. Low Distortion Audio Mixer Eliminates Switching Noise

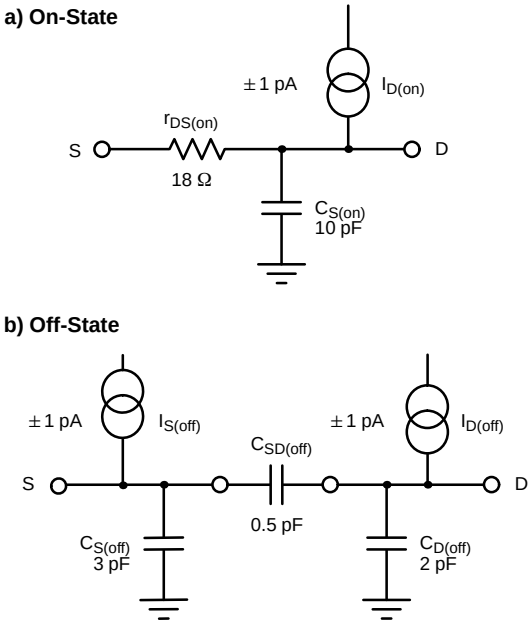


FIGURE 20. Static Switch Models

Audio Mixer

Switching audio inputs at the summing junction of an op amp eliminates audio distortion due to on-resistance modulation. This is because when turned on, the analog switch channel stays at a constant 0 V. Unfortunately, any charge injection present during switching at the high impedance Op Amp input gets amplified and can cause large output spikes. These switching spikes usually cause clicking and/or popping noises. Thanks to its low charge injection properties, the DG61X family virtually eliminates this type of switching noise. A small snubber network connected across the op amp inputs further reduces any high-speed glitches.

Switch Models

The following static models are useful for analyzing circuit performance when the switch is fully on or fully off. For the dynamic parameters such as switching times and charge injection it is better to refer to the typical characteristic curves provided in the data sheet.

The on-state model shown in Figure 20 uses typical parameter values for room temperature. The channel-on capacitance ($C_{D(on)}$) and channel-on leakage ($I_{D(on)}$) are placed on the output side to simulate the worst case possible. In reality, both parameters are distributed along the channel. If you would like to refine the model you may want to divide these lumped parameters into two or three fractions.

Single-Supply Operation

Disk drives and other computer peripherals may only have +12-V and +5-V power supplies or even just a single +5-V power supply. It is perfectly possible to operate the DG611 with the power-supply configurations shown in Figure 21. In case (c) the logic has to be 12-V CMOS. In (b), the switch on-resistance will be high and the analog dynamic range will be reduced to about 0 to 2 V, due to the limited channel enhancement voltage available. (See Figure 7.)

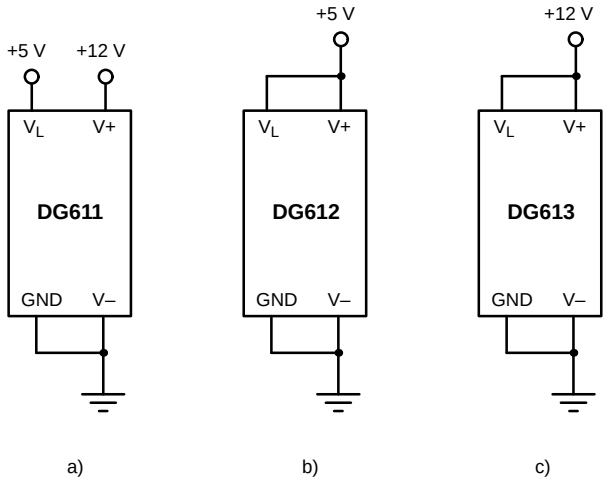


FIGURE 21. Unipolar Supply Configurations

Conclusion

By integrating fast DMOS FETs with high-speed CMOS drivers, the DG611 family of monolithic analog switches improves reliability and reduces part count. These fast analog switches simultaneously establish new records for high speed, low charge injection, and low power. These significant performance achievements bring considerable benefits to many dynamic switching applications.

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