

74LVC2G86

Dual 2-input exclusive-OR gate

Rev. 03 — 7 February 2005

Product data sheet

1. General description

The 74LVC2G86 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off} . The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC2G86 provides the dual 2-input exclusive-OR gate.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- Inputs accept voltages up to 5 V
- Direct interface with TTL levels
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low-power consumption
- Latch-up performance exceeds 250 mA
- ESD protection:
 - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

PHILIPS

3. Quick reference data

Table 1: Quick reference data

$GND = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL} , t_{PLH}	propagation delay inputs nA, nB to outputs nY	$V_{CC} = 1.8\text{ V}$; $C_L = 30\text{ pF}$; $R_L = 1\text{ k}\Omega$	-	3.8	-	ns
		$V_{CC} = 2.5\text{ V}$; $C_L = 30\text{ pF}$; $R_L = 500\text{ }\Omega$	-	2.5	-	ns
		$V_{CC} = 2.7\text{ V}$; $C_L = 50\text{ pF}$; $R_L = 500\text{ }\Omega$	-	3.0	-	ns
		$V_{CC} = 3.3\text{ V}$; $C_L = 50\text{ pF}$; $R_L = 500\text{ }\Omega$	-	2.3	-	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 50\text{ pF}$; $R_L = 500\text{ }\Omega$	-	1.9	-	ns
C_I	input capacitance		-	2.5	-	pF
C_{PD}	power dissipation capacitance per gate	$V_{CC} = 3.3\text{ V}$	[1] [2]	15.8	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of switching inputs;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[2] The condition is $V_I = GND$ to V_{CC} .

4. Ordering information

Table 2: Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G86DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G86DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G86GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $1 \times 1.95 \times 0.5\text{ mm}$	SOT833-1

5. Marking

Table 3: Marking

Type number	Marking code
74LVC2G86DP	V86
74LVC2G86DC	V86
74LVC2G86GT	V86

6. Functional diagram

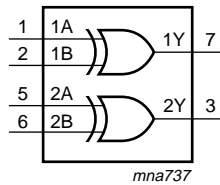


Fig 1. Logic symbol

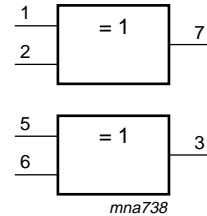


Fig 2. IEC logic symbol

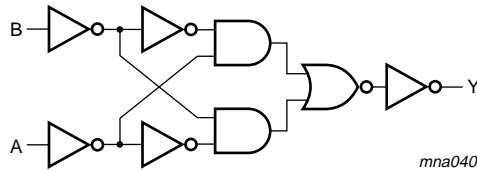


Fig 3. Logic diagram (one driver)

7. Pinning information

7.1 Pinning

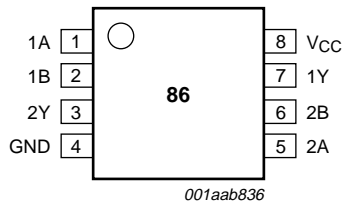


Fig 4. Pin configuration TSSOP8 and VSSOP8

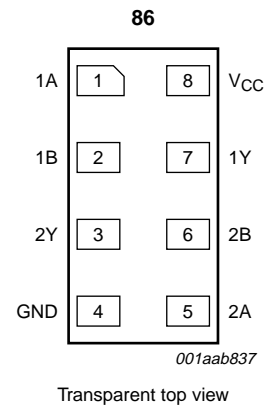


Fig 5. Pin configuration XSON8

7.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
1A	1	1 data input A
1B	2	1 data input B
2Y	3	2 data output Y
GND	4	ground (0 V)
2A	5	2 data input A
2B	6	2 data input B
1Y	7	1 data output Y
V _{CC}	8	supply voltage

8. Functional description

8.1 Function table

Table 5: Function table [\[1\]](#)

Input		Output
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage		[1] -0.5	+6.5	V
V_O	output voltage	Active mode	[1] -0.5	$V_{CC} + 0.5$	V
		Power-down mode	[1][2] -0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V	-	-50	mA
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
I_O	output source or sink current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	± 100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

10. Recommended operating conditions

Table 7: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 1.65$ V to 2.7 V	0	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	0	-	10	ns/V

11. Static characteristics

Table 8: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$ [1]						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\text{ }\mu\text{A}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}$; $V_{CC} = 1.65\text{ V}$	-	0.07	0.45	V
		$I_O = 8\text{ mA}$; $V_{CC} = 2.3\text{ V}$	-	0.12	0.3	V
		$I_O = 12\text{ mA}$; $V_{CC} = 2.7\text{ V}$	-	0.17	0.4	V
		$I_O = 24\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	0.33	0.55	V
		$I_O = 32\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.39	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\text{ }\mu\text{A}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}$; $V_{CC} = 1.65\text{ V}$	1.2	1.54	-	V
		$I_O = -8\text{ mA}$; $V_{CC} = 2.3\text{ V}$	1.9	2.15	-	V
		$I_O = -12\text{ mA}$; $V_{CC} = 2.7\text{ V}$	2.2	2.50	-	V
		$I_O = -24\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.3	2.62	-	V
		$I_O = -32\text{ mA}$; $V_{CC} = 4.5\text{ V}$	3.8	4.11	-	V
I_{LI}	input leakage current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 5.5\text{ V}$	-	± 0.1	± 5	μA
I_{off}	power-off leakage current	V_I or $V_O = 5.5\text{ V}$; $V_{CC} = 0\text{ V}$	-	± 0.1	± 10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 5.5\text{ V}$	-	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$; $V_{CC} = 2.3\text{ V to }5.5\text{ V}$	-	5	500	μA
C_I	input capacitance		-	2.5	-	pF
$T_{amb} = -40\text{ °C to }+125\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V

Table 8: Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.80	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	0.95	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.7	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	1.9	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.0	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.4	-	-	V
I _{LI}	input leakage current	V _I = 5.5 V or GND; V _{CC} = 5.5 V	-	-	±20	μA
I _{off}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	-	±20	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	40	μA
ΔI _{CC}	additional quiescent supply current per pin	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	-	5000	μA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

12. Dynamic characteristics

Table 9: Dynamic characteristicsGND = 0 V; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb} = -40 °C to +85 °C [1]						
t _{PHL} , t _{PLH}	propagation delay inputs nA, nB to outputs nY	see Figure 6				
		V _{CC} = 1.65 V to 1.95 V	1.4	3.8	9.9	ns
		V _{CC} = 2.3 V to 2.7 V	0.8	2.5	5.7	ns
		V _{CC} = 2.7 V	0.8	3.0	5.7	ns
		V _{CC} = 3.0 V to 3.6 V	0.8	2.3	4.7	ns
		V _{CC} = 4.5 V to 5.5 V	0.6	1.9	3.6	ns
C _{PD}	power dissipation capacitance per gate	V _{CC} = 3.3 V	[2] [3] -	15.8	-	pF

Table 9: Dynamic characteristics ...continued
 GND = 0 V; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
t _{PHL} , t _{PLH}	propagation delay inputs nA, nB to outputs nY	see Figure 6				
		V _{CC} = 1.65 V to 1.95 V	1.4	3.8	12.4	ns
		V _{CC} = 2.3 V to 2.7 V	0.8	2.5	7.2	ns
		V _{CC} = 2.7 V	0.8	3.0	7.2	ns
		V _{CC} = 3.0 V to 3.6 V	0.8	2.3	5.9	ns
		V _{CC} = 4.5 V to 5.5 V	0.6	1.9	4.5	ns

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in Volts;
 N = number of switching inputs;
 Σ(C_L × V_{CC}² × f_o) = sum of outputs.
- [3] The condition is V_I = GND to V_{CC}.

13. Waveforms

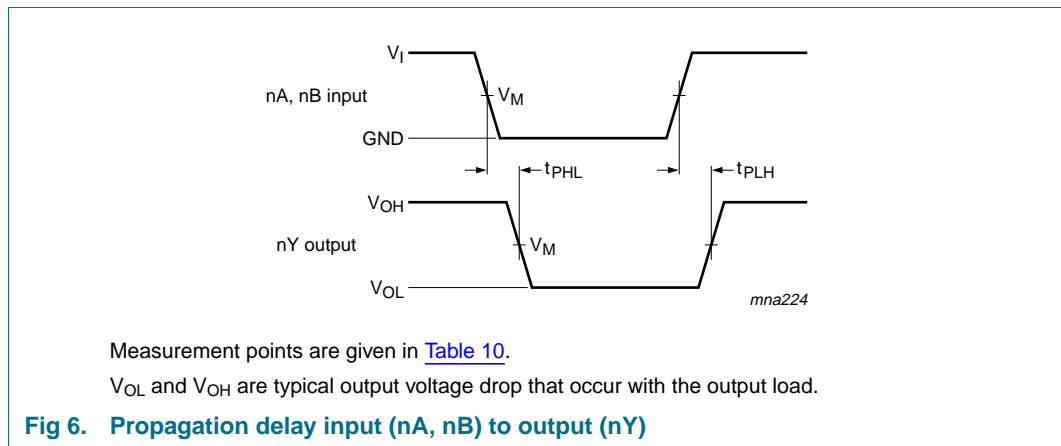


Table 10: Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
1.65 V to 1.95 V	0.5 × V _{CC}	0.5 × V _{CC}
2.3 V to 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V _{CC}	0.5 × V _{CC}

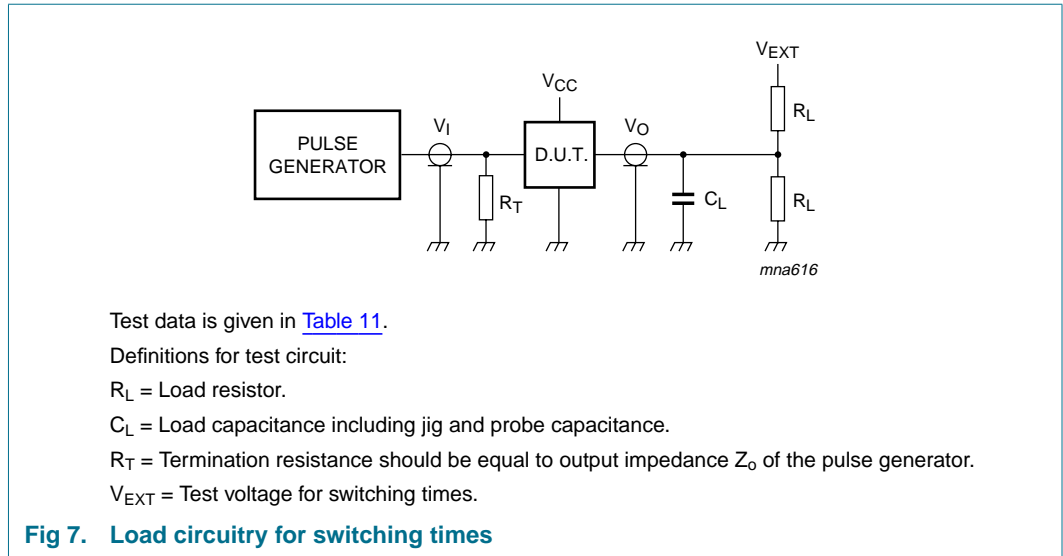


Table 11: Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

14. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

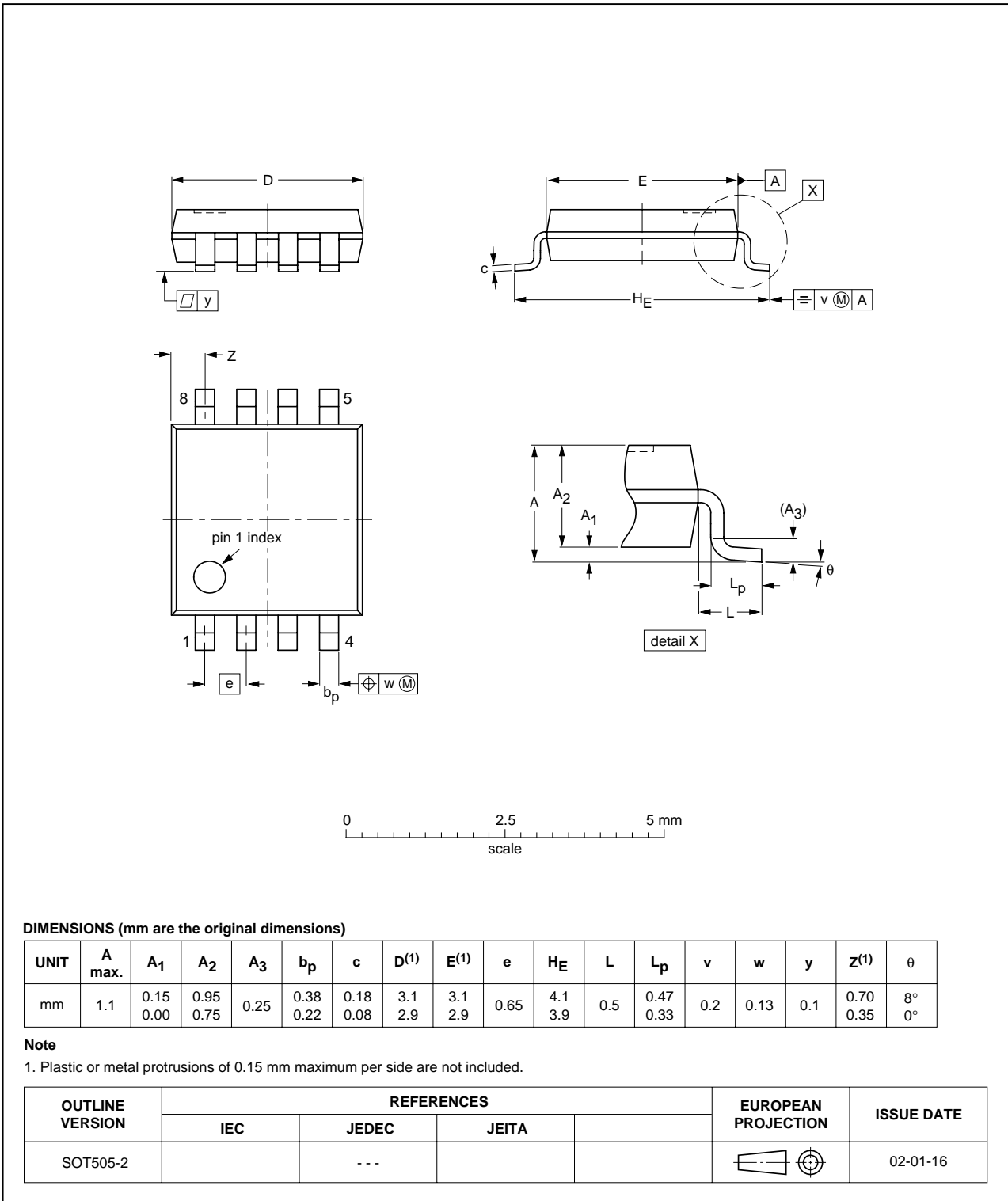


Fig 8. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

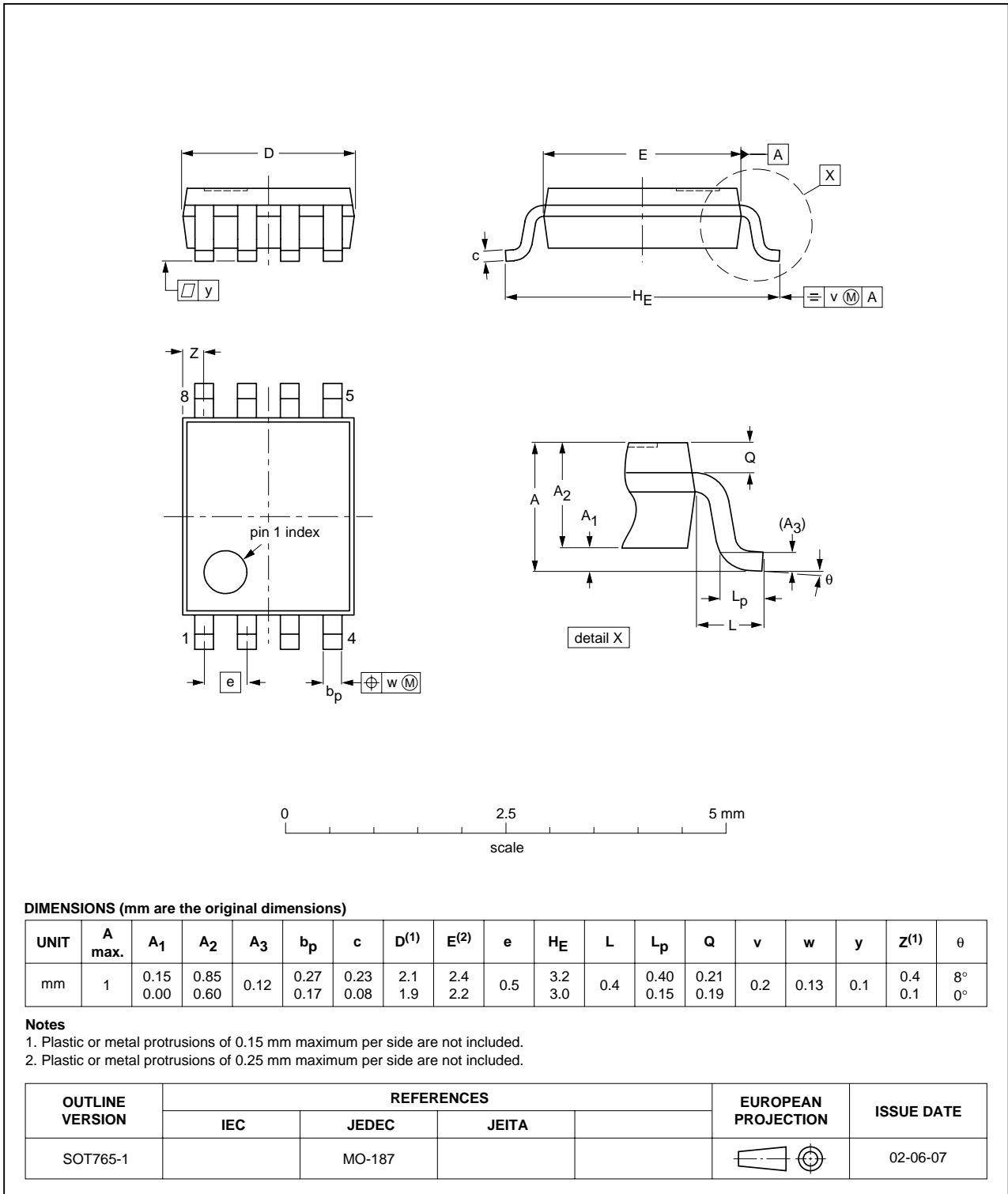


Fig 9. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

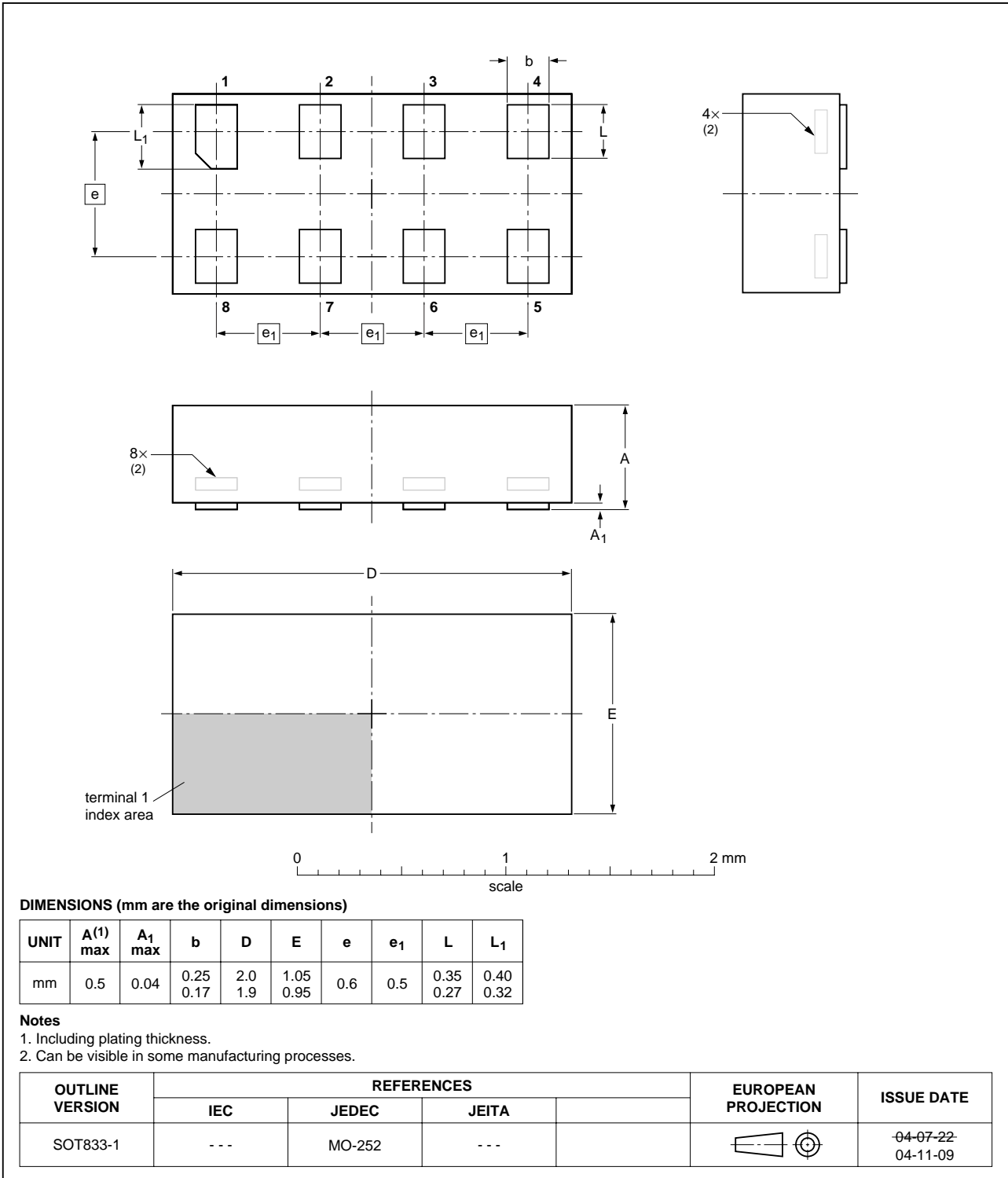


Fig 10. Package outline SOT833-1 (XSON8)

15. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVC2G86_3	20050207	Product data sheet	-	9397 750 14506	74LVC2G86_2
Modifications:					
					<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors• Added: type number 74LVC2G86DC (VSSOP8 package)• Table 2: Changed type number 74LVC2GM into 74LVC2GT
74LVC2G86_2	20041018	Product specification	-	9397 750 13786	74LVC2G86_1
74LVC2G86_1	20030825	Product specification	-	9397 750 11851	-

16. Data sheet status

Level	Data sheet status ^[1]	Product status ^[2] ^[3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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