Flash-ROM Module 8MByte (2Mx32Bit), 72Pin-SIMM, 3.3V Design
Part No. HMF2M32M4VGL

GENERAL DESCRIPTION

The HMF2M32M4VGL is a high-speed flash read only memory (FROM) module containing 2,097,152 words organized in a x32bit configuration. The module consists of four 2M x 8bit FROM mounted on a 72 -pin, single-sided, FR4-printed circuit board.
Commands are written to the command register using standard microprocessor write timings.
Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.
Four chip enable inputs, (/WE0, /WE1, /WE2, /WE3) are used to enable the module's 8 bits independently. Output enable (/OE) and write enable (/WE) can set the memory input and output.
When FROM module is disable condition the module is becoming power standby mode, system designer can get low -power design. All module components may be powered from a single + 3.3V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- Access time : 70, 80, 90, 120ns
- High-density 8MByte design
- High-reliability, low-power design
- Single + 3.3V ± 0.3V power supply
- Easy memory expansion
- All inputs and outputs are TTL-compatible
- FR4-PCB design
- Low profile 72-pin SIMM
- Minimum 1,000,000 write/erase cycle
- Sectors erase architecture
- Sector group protection
- Temporary sector group unprotection

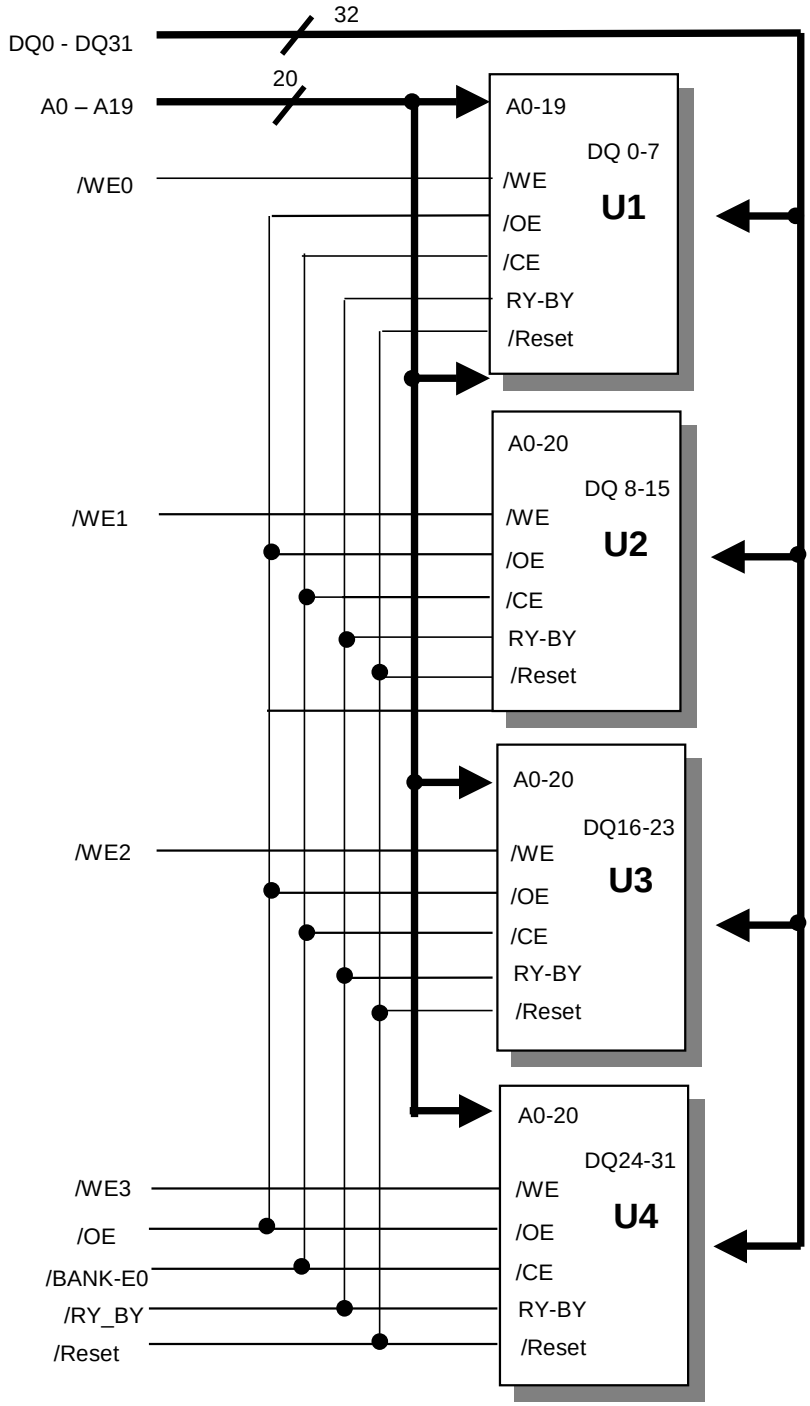
OPTIONS MARKING

- Timing
  - 70ns access -70
  - 80ns access -80
  - 90ns access -90
  - 120ns access -120
- Packages
  - 72-pin SIMM M

PIN ASSIGNMENT

PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vss	25	DQ17	49	/BANKE0
2	NC	26	DQ18	50	A3
3	DQ0	27	DQ19	51	A4
4	DQ1	28	DQ20	52	A5
5	DQ2	29	DQ21	53	A6
6	DQ3	30	Vcc	54	A7
7	DQ4	31	DQ22	55	A8
8	DQ5	32	DQ23	56	A9
9	DQ6	33	/WE2	57	A10
10	Vcc	34	NC	58	A11
11	DQ7	35	DQ24	59	Vcc
12	/WE0	36	DQ25	60	A12
13	/RY_BY	37	DQ26	61	A13
14	DQ8	38	DQ27	62	A14
15	DQ9	39	Vss	63	A15
16	DQ10	40	DQ28	64	A16
17	DQ11	41	DQ29	65	A17
18	DQ12	42	DQ30	66	A18
19	DQ13	43	DQ31	67	A19
20	DQ14	44	/WE3	68	A20
21	DQ15	45	NC	69	A0
22	/WE1	46	/RESET	70	A1
23	NC	47	A2	71	NC
24	DQ16	48	/OE	72	Vss

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	/RESET	DQ (/BYTE=L)	POWER
STANDBY	X	H	X	Vcc±0.3V	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
READ	L	L	H	H	D_{OUT}	ACTIVE
WRITE or ERASE	X	L	L	H	D_{IN}	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	$V_{IN,OUT}$	-0.5V to Vcc+0.5V
Voltage with respect to ground Vcc	V_{CC}	-0.5V to +4.0V
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	-55°C to +125°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
Vcc for ± 10% device Supply Voltages	Vcc	2.7V		3.6V
Ground	V_{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS ($0^oC \leq T_A \leq 70\ ^oC$)

PARAMETER	TEST CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT
Input Load Current	Vcc=Vcc max, V_{IN}= Vss to Vcc		I_{L1}			±1.0	µA
A9 Input Loda Current	Vcc=Vcc max, ; A9=12.5 V		I_{L1T}			35	µA
Output Leakage Current	Vcc=Vcc max, V_{OUT}= Vss to Vcc		I_{L0}			±1.0	µA
Vcc Active Read Current (1)	/CE= V_{IL}, /OE= V_{IH}, Byte Mode	5MHz	I_{CC1}		9	16	µA
		1MHz			2	4	
	/CE= V_{IL}, /OE= V_{IH}, Word Mode	5MHz			9	16	
		1MHz			2	4	
Vcc Active Write Current (Note2,3,4)	/CE = V_{IL}, /OE=V_{IH}		I_{CC2}		20	30	mA
Vcc Standby Current(Note2)	/CE, /RESET=Vcc±0.3V		I_{CC3}		0.2	5	mA

Vcc Standby Current During Reset(Note2)	/RESET=Vss±0.3V	I_{CC4}		0.2	5	mA
Automatic Sleep Mode(Note2,5)	V_{IH}= Vcc ±0.3V; V_{IL}= Vss ±0.3V;	V_{CC5}		0.2	5	V
Input Low Voltage		V_{IL}	-0.5		0.8	V
Input High Voltage		V_{IH}	0.7×Vcc		**Vcc+0.3**	V
Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3V	V_{ID}	11.5		12.5	V
Output Low Voltage	I_{OL} = 4.0mA, Vcc =Vcc min	V_{OL}			0.45	V
Output High Voltage	I_{OH} = -2.0mA, Vcc =Vcc min	0.85×Vcc				V
	I_{OH} = -100µA, Vcc =Vcc min	Vcc-0.4				
Low Vcc Lock-Out Voltage(Note 4)		V_{LKO}	2.3		2.5	V

Notes

1. The Icc Current listed is typically less than 2 ma/MHz,with /OE at $V_{IH.}$ Typical Vcc is 3.0V.
2. Maximum Icc Specifications are tested with Vcc=Vccmax.
3. Icc active while Embedded Erase of Embedded Program is in progress.

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	0.7	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time		25		sec	
Byte Programming Time	-	9	300	µs	Excludes system-level overhead
Chip Programming Time	-	18	54	sec	

TSOP CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes : Test conditions T_A = 25°C, f=1.0 MHz.

AC CHARACTERISTICS

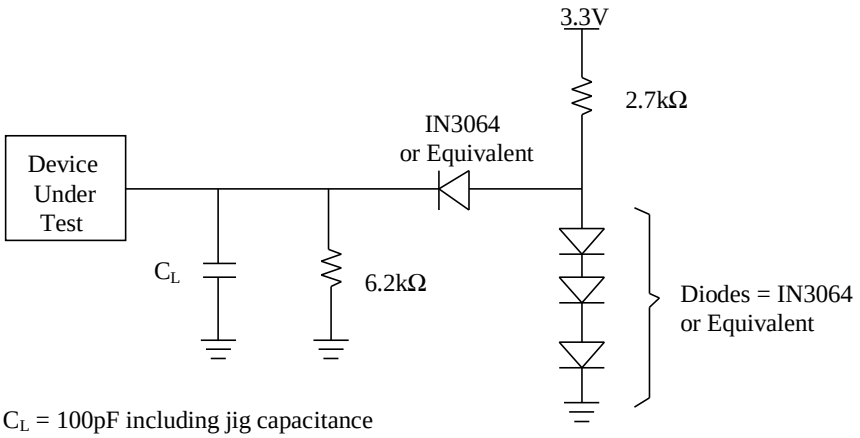
u Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION		TEST SETUP		Speed Options				UNIT
JEDEC	STANDARD					-70R	-80	-90	-120	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	80	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		/CE = V_{IL} /OE = V_{IL}	Max	70	80	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		/OE = V_{IL}	Max	70	80	90	120	ns
t_{GLQV}	t_{OE}	Chip Enable to Output Delay			Max	30	30	35	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z			Max	25	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z			Max	25	25	30	30	ns
		Output Enable Hold Time(Note 1)	Read		Min	0				ns
			Toggle and /Data Polling		Min	10				
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First			Min	0				ns

Notes :
1. Not 100% tested.
2. See Figure 5 and Table 10 for test specifications.

TEST SPECIFICATIONS

TEST CONDITION	70R, 80	90, 120	UNIT
Output load	1TTL gate		
Output load capacitance,C_L (Including jig capacitance)	30	100	pF
Input rise and fall times	5		ns
Input pulse levels	0.0-3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V



Note : C_L = 100pF including jig capacitance

u Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION			Speed Options				UNIT
JEDEC	STANDARD				70R	80	90	120	
t_{AVAV}	t_{WC}	Write Cycle Time		Min	70	80	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OES}	Output Enable Setup Time		Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min	0				ns
t_{ELWL}	t_{CS}	/CE Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	/CE Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Byte	Typ	9				µs
			Word	Typ	11				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)		Typ	0.7				sec
	t_{VCS}	Vcc set up time		Min	50				µs
	t_{RB}	Recovery Time from RY//BY		Min	0				ns
	t_{BUSY}	Program/Erase Valid to RY//BY Delay		Min	90				ns

Notes :

1. Not 100% tested.
2. See the “Erase and Programming Performance” section for more information.

u Erase/Program Operations

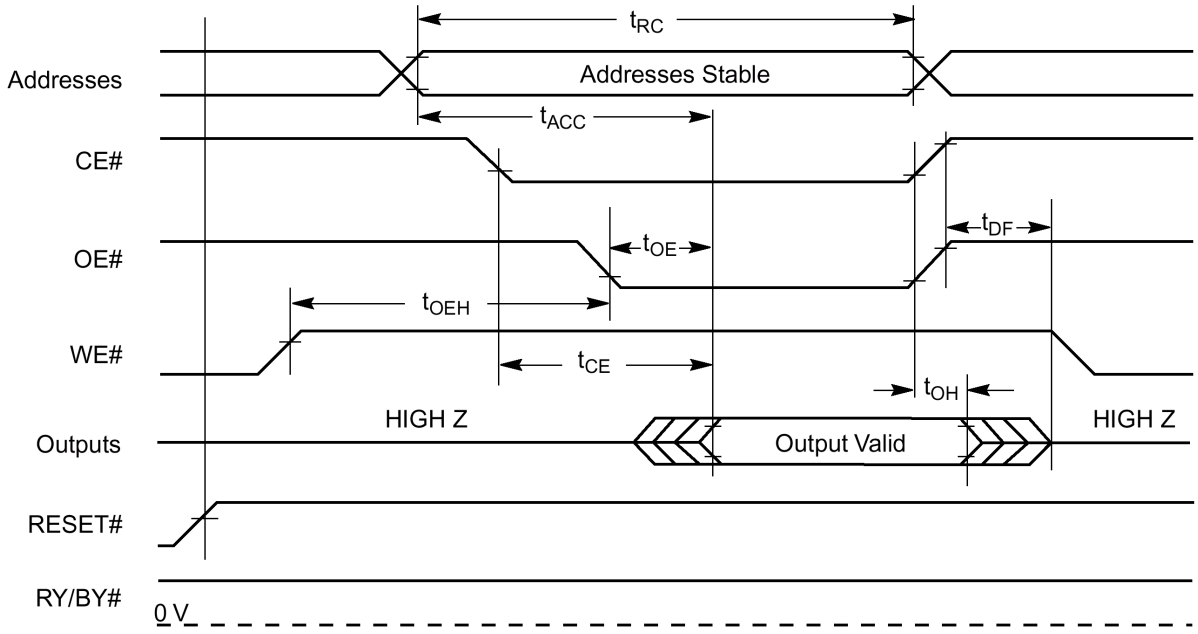
Alternate /CE Controlled Writes

PARAMETER SYMBOLS		DESCRIPTION			Speed Options				UNIT
JEDEC	STANDARD				-70R	-80	-90	120	
t_{AVAV}	t_{WC}	Write Cycle Time		Min	70	80	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	35	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OES}	Output Enable Setup Time		Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min	0				ns
t_{WLEL}	t_{WS}	/WE Setup Time		Min	0				ns
t_{EHEH}	t_{WH}	/WE Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	/CE Pulse Width		Min	35	35	35	50	ns
T_{EHEL}	t_{CPH}	/CE Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming	Byte	Typ	9				µs
		Operation	Word	Typ	11				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation		Typ	0.7				sec

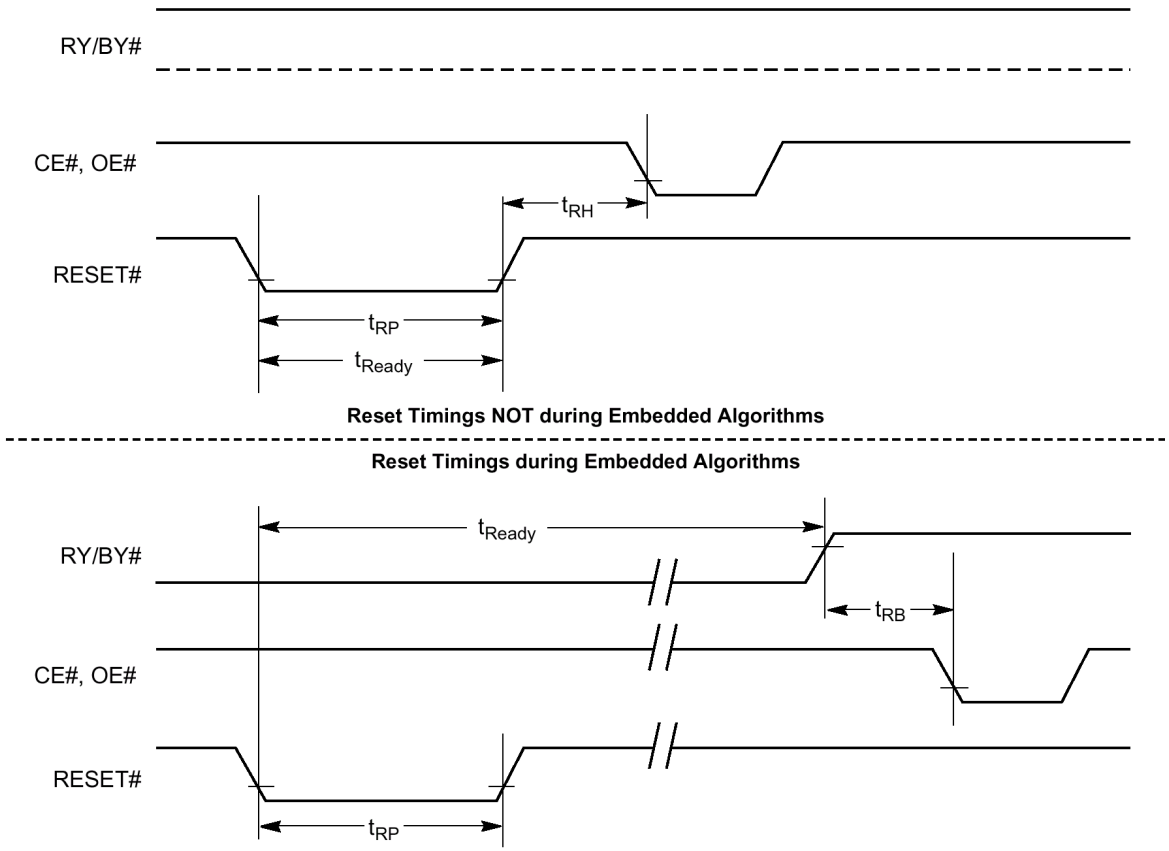
Notes :

1. Not 100% tested.
2. See the “Erase and Programming Performance”section for more information.

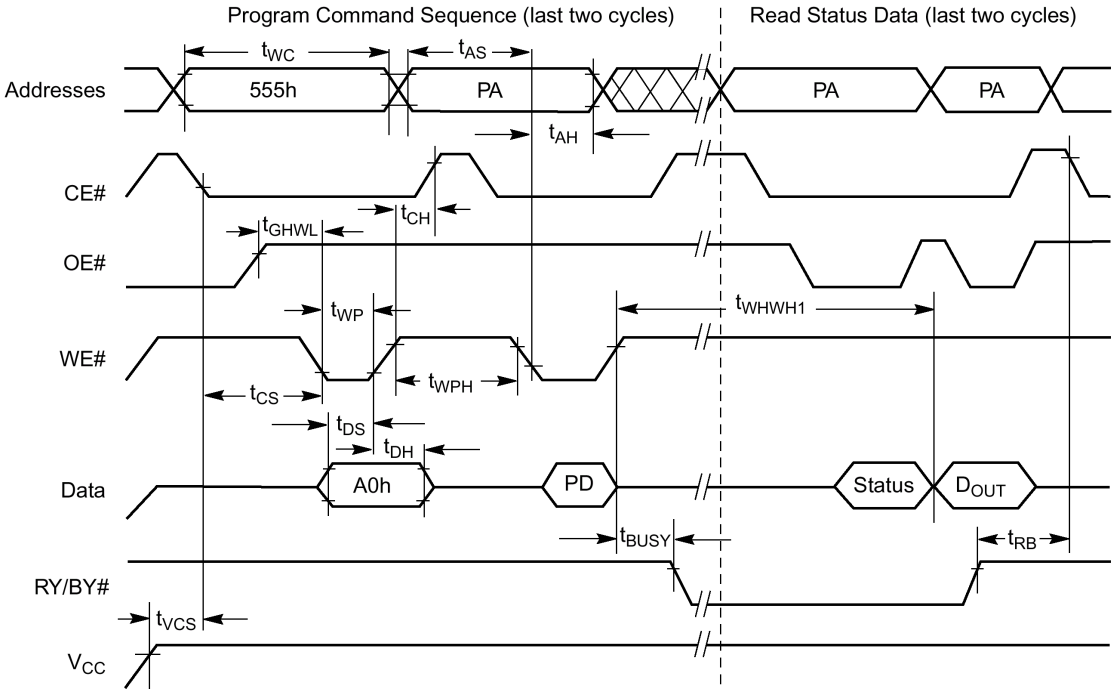
u READ OPERATIONS TIMING



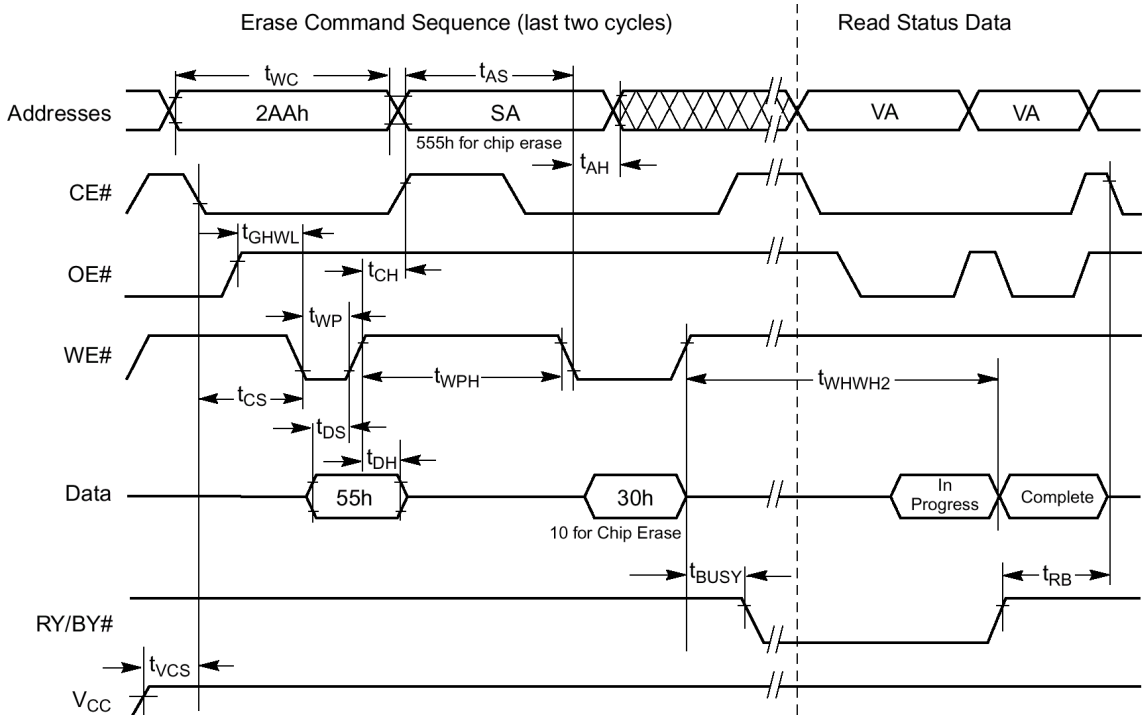
u RESET TIMING



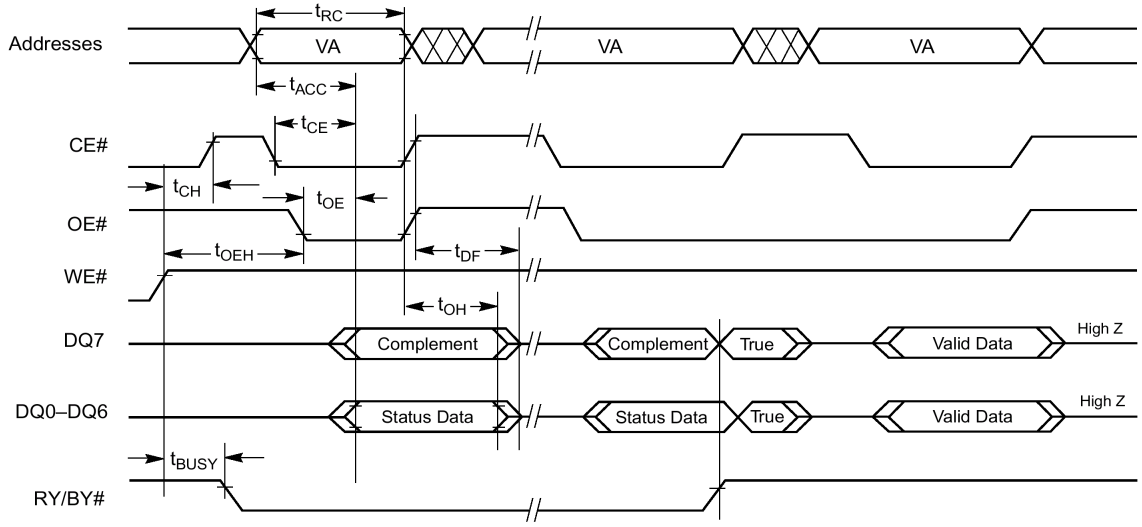
u PROGRAM OPERATIONS TIMING



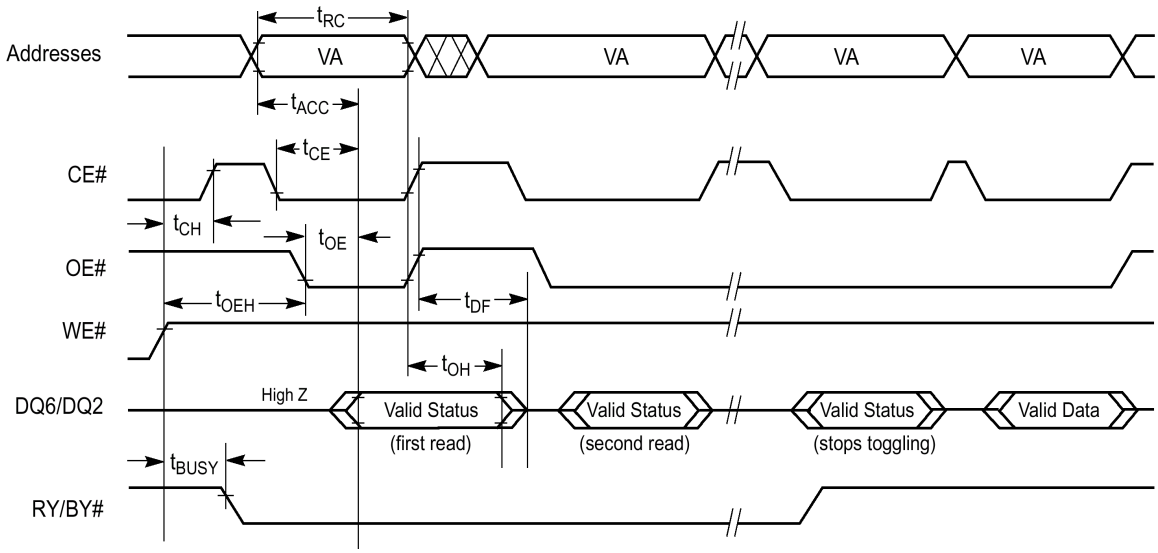
u CHIP/SECTOR ERASE OPERATION TIMINGS



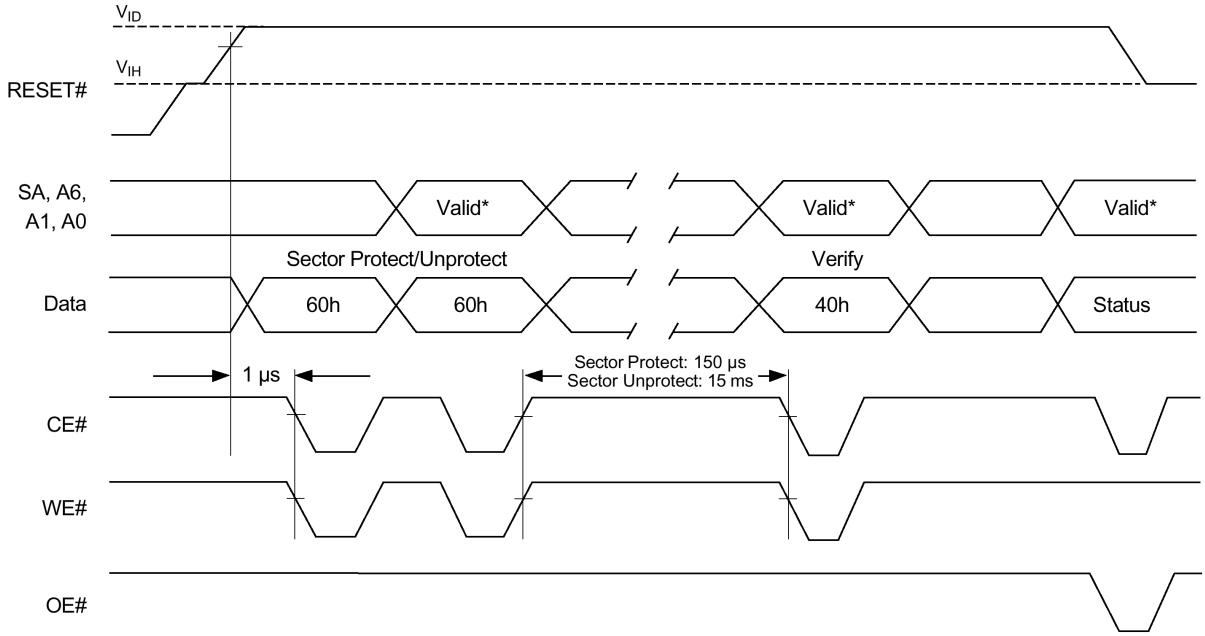
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



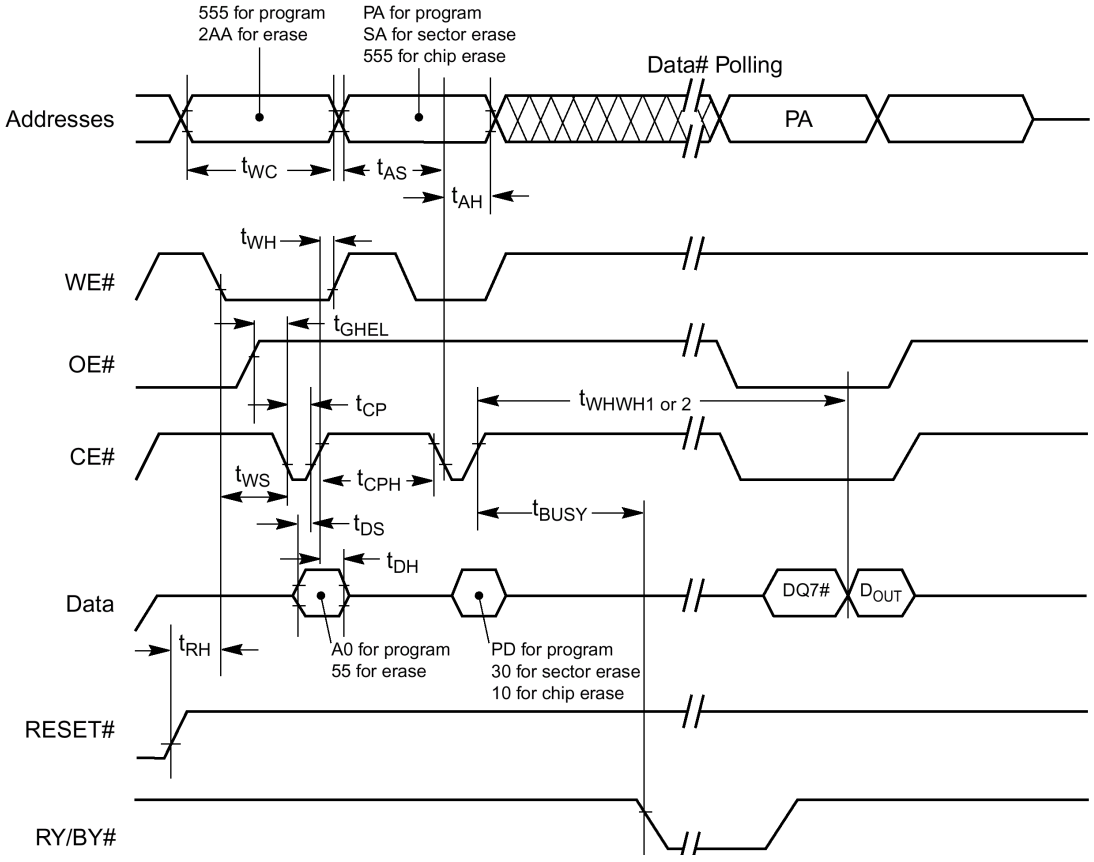
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



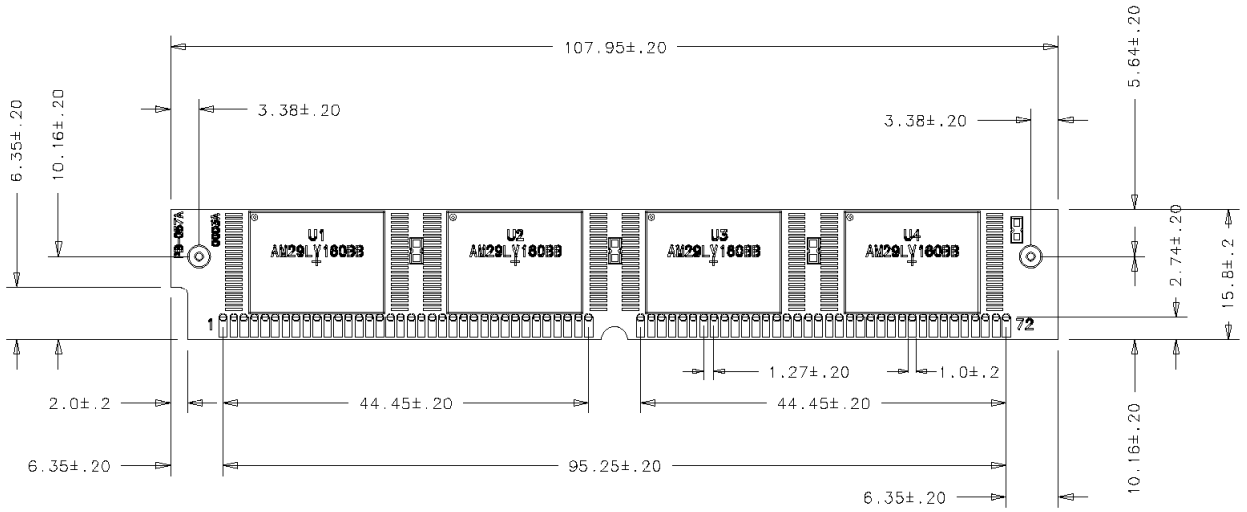
u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

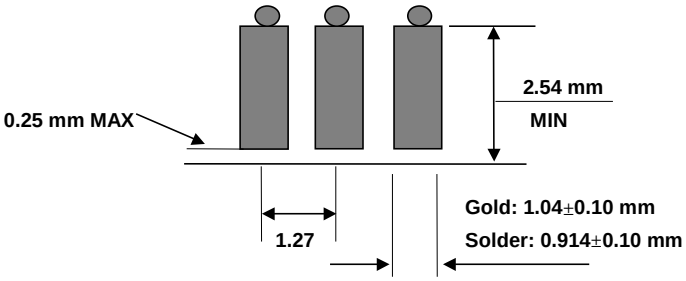


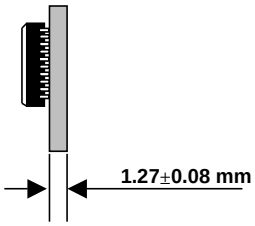
u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



PACKAGE DIMENSIONS







(Solder & Gold Plating)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF2M32M4VGL-70	8MByte	2Mx 32Bit	72Pin -SIMM	4EA	3.3V	70ns
HMF2M32M4VGL-80	8MByte	2Mx 32Bit	72Pin -SIMM	4EA	3.3V	80ns
HMF2M32M4VGL-90	8MByte	2Mx 32Bit	72Pin -SIMM	4EA	3.3V	90ns
HMF2M32M4VGL-120	8MByte	2Mx 32Bit	72Pin -SIMM	4EA	3.3V	120ns