

Product Preview

**Low-Voltage 1.8/2.5/3.3V
16-Bit Transparent Latch
With 3.6V-Tolerant Inputs and
Outputs (3-State, Non-Inverting)**

The MC74VCX16373 is an advanced performance, non-inverting 16-bit transparent latch. It is designed for very high-speed, very low-power operation in 1.8V, 2.5V or 3.3V systems. The VCX16373 is byte controlled, with each byte functioning identically, but independently. Each byte has separate Output Enable and Latch Enable inputs. These control pins can be tied together for full 16-bit operation.

When operating at 2.5V (or 1.8V) the part is designed to tolerate voltages it may encounter on either inputs or outputs when interfacing to 3.3V busses. It is guaranteed to be over-voltage tolerant to 3.6V.

The MC74VCX16373 contains 16 D-type latches with 3-state 3.6V-tolerant outputs. When the Latch Enable (LEn) inputs are HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, (a latch output will change state each time its D input changes). When LE is LOW, the latch stores the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state outputs are controlled by the Output Enable (OEn) inputs. When OE is LOW, the outputs are enabled. When OE is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

- Designed for Low Voltage Operation: $V_{CC} = 1.8-3.6V$
- 3.6V Tolerant Inputs and Outputs
- High Speed Operation: 3.0ns max for 3.0 to 3.6V
3.4ns max for 2.3 to 2.7V
6.0ns max for 1.8V
- Static Drive: $\pm 24mA$ Drive at 3.0V
 $\pm 18mA$ Drive at 2.3V
 $\pm 6mA$ Drive at 1.8V
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0V$
- Near Zero Static Supply Current in All Three Logic States (20 μA)
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds $\pm 300mA$
- ESD Performance: Human Body Model >2000V; Machine Model >200V

MC74VCX16373

VCX

**LOW-VOLTAGE 1.8/2.5/3.3V
16-BIT TRANSPARENT LATCH**



DT SUFFIX
48-LEAD PLASTIC TSSOP PACKAGE
CASE 1201-01

PIN NAMES

Pins	Function
OEn	Output Enable Inputs
LEn	Latch Enable Inputs
D0-D15	Inputs
O0-O15	Outputs

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC74VCX16373

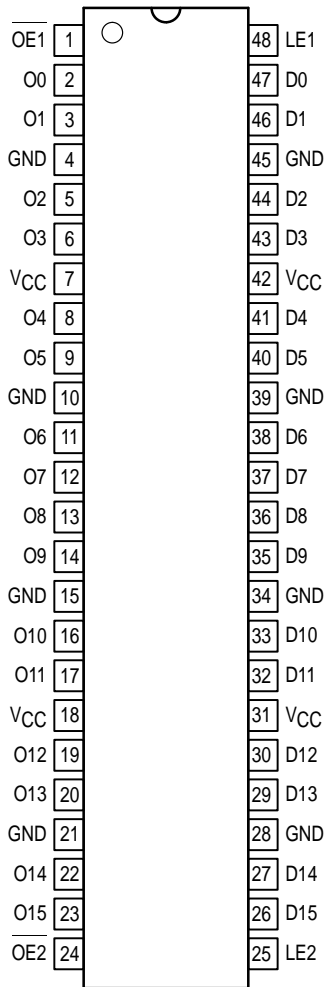


Figure 1. 48-Lead Pinout (Top View)

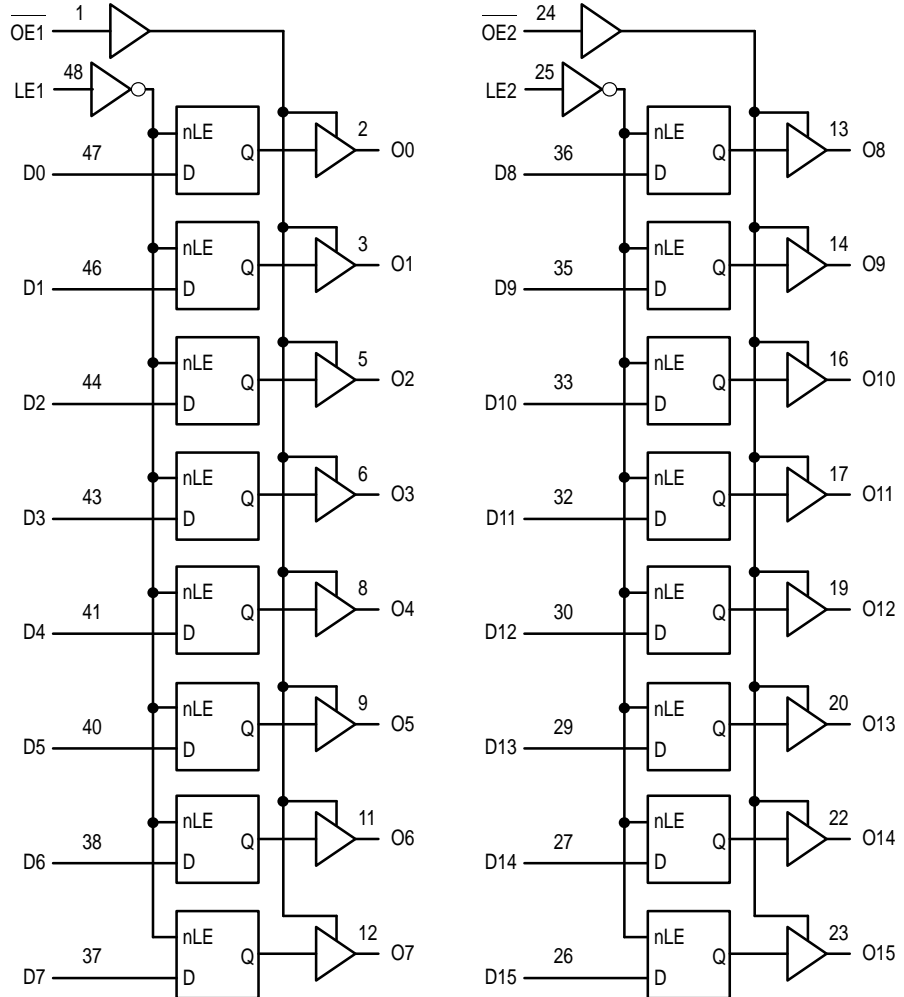


Figure 2. Logic Diagram

Inputs			Outputs	Inputs			Outputs
LE1	OE1	D0:7	O0:7	LE2	OE2	D8:15	O8:15
X	H	X	Z	X	H	X	Z
H	L	L	L	H	L	L	L
H	L	H	H	H	L	H	H
L	L	X	O0	L	L	X	O0

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	-0.5 to +4.6		V
V _I	DC Input Voltage	-0.5 ≤ V _I ≤ +4.6		V
V _O	DC Output Voltage	-0.5 ≤ V _O ≤ +4.6	Output in 3-State	V
		-0.5 ≤ V _O ≤ V _{CC} + 0.5	Note 1.; Outputs Active	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Supply Voltage	Operating	1.8	3.6	V
		Data Retention Only	1.2	3.6	
V _I	Input Voltage	-0.3	3.6	V	
V _O	Output Voltage	(Active State)	0	V _{CC}	V
		(3-State)	0	3.6	
I _{OH}	HIGH Level Output Current, V _{CC} = 3.0V – 3.6V		-24	mA	
I _{OL}	LOW Level Output Current, V _{CC} = 3.0V – 3.6V		24	mA	
I _{OH}	HIGH Level Output Current, V _{CC} = 2.3V – 2.7V		-18	mA	
I _{OL}	LOW Level Output Current, V _{CC} = 2.3V – 2.7V		18	mA	
I _{OH}	HIGH Level Output Current, V _{CC} = 1.8V		-6	mA	
I _{OL}	LOW Level Output Current, V _{CC} = 1.8V		6	mA	
T _A	Operating Free-Air Temperature	-40	+85	°C	
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from 0.8V to 2.0V, V _{CC} = 3.0V	0	10	ns/V	

DC ELECTRICAL CHARACTERISTICS ($2.7V < V_{CC} \leq 3.6V$)

Symbol	Characteristic	Condition	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2.)	$2.7V < V_{CC} \leq 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 2.)	$2.7V < V_{CC} \leq 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V < V_{CC} \leq 3.6V; I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.7V; I_{OH} = -12\text{mA}$	2.2		
		$V_{CC} = 3.0V; I_{OH} = -18\text{mA}$	2.4		
		$V_{CC} = 3.0V; I_{OH} = -24\text{mA}$	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V < V_{CC} \leq 3.6V; I_{OL} = 100\mu\text{A}$		0.2	V
		$V_{CC} = 2.7V; I_{OL} = 12\text{mA}$		0.4	
		$V_{CC} = 3.0V; I_{OL} = 18\text{mA}$		0.4	
		$V_{CC} = 3.0V; I_{OL} = 24\text{mA}$		0.55	
I_I	Input Leakage Current	$2.7V < V_{CC} \leq 3.6V; 0V \leq V_I \leq 3.6V$		± 5.0	μA
I_{OZ}	3-State Output Current	$2.7V < V_{CC} \leq 3.6V; 0V \leq V_O \leq 3.6V;$ $V_I = V_{IH} \text{ or } V_{IL}$		± 10	μA
I_{OFF}	Power-Off Leakage Current	$V_{CC} = 0V; 0V \leq (V_I, V_O) \leq 3.6V$		10	μA
I_{CC}	Quiescent Supply Current	$2.7V < V_{CC} \leq 3.6V; V_I = \text{GND or } V_{CC}$		20	μA
		$2.7V < V_{CC} \leq 3.6V; V_{CC} \leq (V_I, V_O) \leq 3.6V$		± 20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7V < V_{CC} \leq 3.6V; V_{IH} = V_{CC} - 0.6V$		750	μA

2. These values of V_I are used to test DC electrical characteristics only.

DC ELECTRICAL CHARACTERISTICS ($2.3V \leq V_{CC} \leq 2.7V$)

Symbol	Characteristic	Condition	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 3.)	$2.3V \leq V_{CC} \leq 2.7V$	1.6		V
V_{IL}	LOW Level Input Voltage (Note 3.)	$2.3V \leq V_{CC} \leq 2.7V$		0.7	V
V_{OH}	HIGH Level Output Voltage	$2.3V \leq V_{CC} \leq 2.7V; I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.3V; I_{OH} = -6\text{mA}$	2.0		
		$V_{CC} = 2.3V; I_{OH} = -12\text{mA}$	1.8		
		$V_{CC} = 2.3V; I_{OH} = -18\text{mA}$	1.7		
V_{OL}	LOW Level Output Voltage	$2.3V \leq V_{CC} \leq 2.7V; I_{OL} = 100\mu\text{A}$		0.2	V
		$V_{CC} = 2.3V; I_{OL} = 12\text{mA}$		0.4	
		$V_{CC} = 2.3V; I_{OL} = 18\text{mA}$		0.6	
I_I	Input Leakage Current	$2.3V \leq V_{CC} \leq 2.7V; 0V \leq V_I \leq 3.6V$		± 5.0	μA
I_{OZ}	3-State Output Current	$2.3V \leq V_{CC} \leq 2.7V;$ $0V \leq V_O \leq 3.6V; V_I = V_{IH} \text{ or } V_{IL}$		± 10	μA
I_{OFF}	Power-Off Leakage Current	$V_{CC} = 0V; 0V \leq (V_I, V_O) \leq 3.6V$		10	μA
I_{CC}	Quiescent Supply Current	$2.3V \leq V_{CC} \leq 2.7V; V_I = \text{GND or } V_{CC}$		20	μA
		$2.3V \leq V_{CC} \leq 2.7V; V_{CC} \leq (V_I, V_O) \leq 3.6V$		± 20	μA

3. These values of V_I are used to test DC electrical characteristics only.

DC ELECTRICAL CHARACTERISTICS ($1.8V \leq V_{CC} < 2.3V$)

Symbol	Characteristic	Condition	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage	$1.8V \leq V_{CC} < 2.3V$	$0.7 \times V_{CC}$		V
V_{IL}	LOW Level Input Voltage	$1.8V \leq V_{CC} < 2.3V$		$0.2 \times V_{CC}$	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = 1.8V; I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 1.8V; I_{OH} = -6\text{mA}$	1.4		
V_{OL}	LOW Level Output Voltage	$V_{CC} = 1.8V; I_{OL} = 100\mu\text{A}$		0.2	V
		$V_{CC} = 1.8V; I_{OL} = 6\text{mA}$		0.3	
I_I	Input Leakage Current	$V_{CC} = 1.8V; 0 \leq V_I \leq 3.6V$		± 5.0	μA
I_{OZ}	3-State Output Current	$V_{CC} = 1.8V; 0 \leq V_O \leq 3.6V; V_I = V_{IH} \text{ or } V_{IL}$		± 10	μA
I_{OFF}	Power-Off Leakage Current	$V_{CC} = 0V; 0V \leq (V_I, V_O) \leq 3.6V$		10	μA
I_{CC}	Quiescent Supply Current	$V_{CC} = 1.8V; V_I = V_{CC} \text{ or } \text{GND}$		20	μA
		$V_{CC} = 1.8V; V_{CC} \leq (V_I, V_O) \leq 3.6V$		± 20	

AC CHARACTERISTICS (Note 4.; $t_R = t_F = 2.0\text{ns}$; $C_L = 30\text{pF}$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits						Unit
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$						
			$V_{CC} = 3.0V \text{ to } 3.6V$		$V_{CC} = 2.3V \text{ to } 2.7V$		$V_{CC} = 1.8V$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Dn to On	1	0.8 0.8	3.0 3.0	1.0 1.0	3.4 3.4		6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to On	1	0.8 0.8	3.1 3.1	1.0 1.0	3.9 3.9		6.0 6.0	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	0.8 0.8	3.5 3.5	1.0 1.0	4.6 4.6		7.0 7.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	0.8 0.8	3.5 3.5	1.0 1.0	3.8 3.8		5.0 5.0	ns
t_s	Setup Time, High or Low Dn to LE	3	1.5		1.5		2.5		ns
t_h	Hold Time, High or Low Dn to LE	3	1.0		1.0		1.0		ns
t_w	LE Pulse Width, High	3	1.5		1.5		3.0		ns
t_{OSHL} t_{OSLH}	Output-to-Output Skew (Note 5.)			0.5 0.5		0.5 0.5		0.5 0.5	ns

- These AC parameters are preliminary and may be modified prior to release. For $C_L = 50\text{pF}$, add approximately 300ps to the AC maximum specification.
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

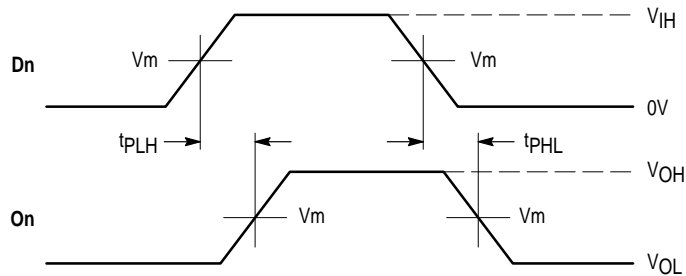
Symbol	Characteristic	Condition	T _A = +25°C	
			Typ	Unit
V _{OLP}	Dynamic LOW Peak Voltage (Note 6.)	V _{CC} = 1.8V, C _L = 30pF, V _{IH} = V _{CC} , V _{IL} = 0V	0.25	V
		V _{CC} = 2.5V, C _L = 30pF, V _{IH} = V _{CC} , V _{IL} = 0V	0.6	
		V _{CC} = 3.3V, C _L = 30pF, V _{IH} = V _{CC} , V _{IL} = 0V	0.8	
V _{OLV}	Dynamic LOW Valley Voltage (Note 6.)	V _{CC} = 1.8V, C _L = 30pF, V _{IH} = V _{CC} , V _{IL} = 0V	-0.25	V
		V _{CC} = 2.5V, C _L = 30pF, V _{IH} = V _{CC} , V _{IL} = 0V	-0.6	
		V _{CC} = 3.3V, C _L = 30pF, V _{IH} = V _{CC} , V _{IL} = 0V	-0.8	
V _{OHV}	Dynamic HIGH Valley Voltage (Note 7.)	V _{CC} = 1.8V, C _L = 30pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.5	V
		V _{CC} = 2.5V, C _L = 30pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.9	
		V _{CC} = 3.3V, C _L = 30pF, V _{IH} = V _{CC} , V _{IL} = 0V	2.2	

- 6. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.
- 7. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the HIGH state.

CAPACITIVE CHARACTERISTICS

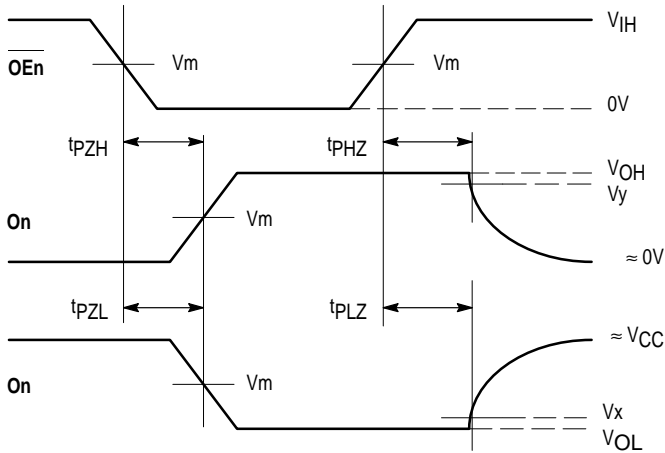
Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	Note 8.	6	pF
C _{OUT}	Output Capacitance	Note 8.	7	pF
CPD	Power Dissipation Capacitance	Note 8., 10MHz	20	pF

8. V_{CC} = 1.8, 2.5 or 3.3V; V_I = 0V or V_{CC}.

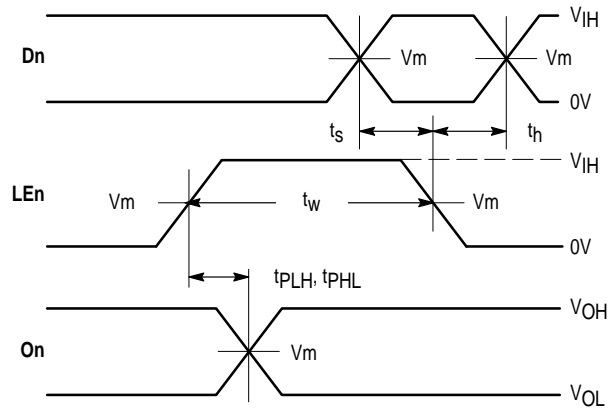


WAVEFORM 1 – PROPAGATION DELAYS
 t_R = t_F = 2.0ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 3. AC Waveforms



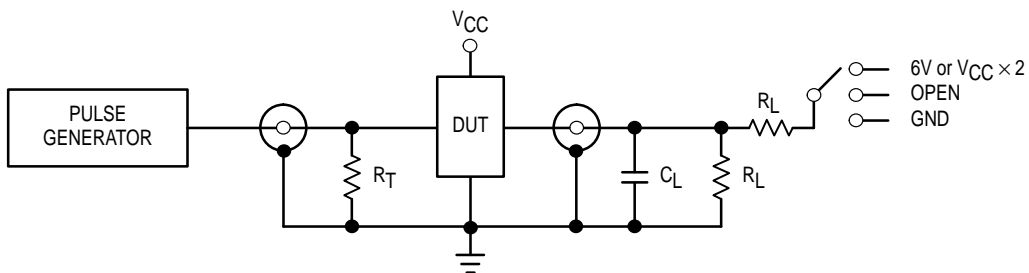
WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.0\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$



WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
 $t_R = t_F = 2.0\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$ except when noted

Figure 4. AC Waveforms

Symbol	VCC		
	3.3V ±0.3V	2.5V ±0.2V	1.8V
VIH	2.7V	VCC	VCC
Vm	1.5V	VCC/2	VCC/2
Vx	VOL + 0.3V	VOL + 0.15V	VOL + 0.15V
Vy	VOH - 0.3V	VOH - 0.15V	VOH - 0.15V



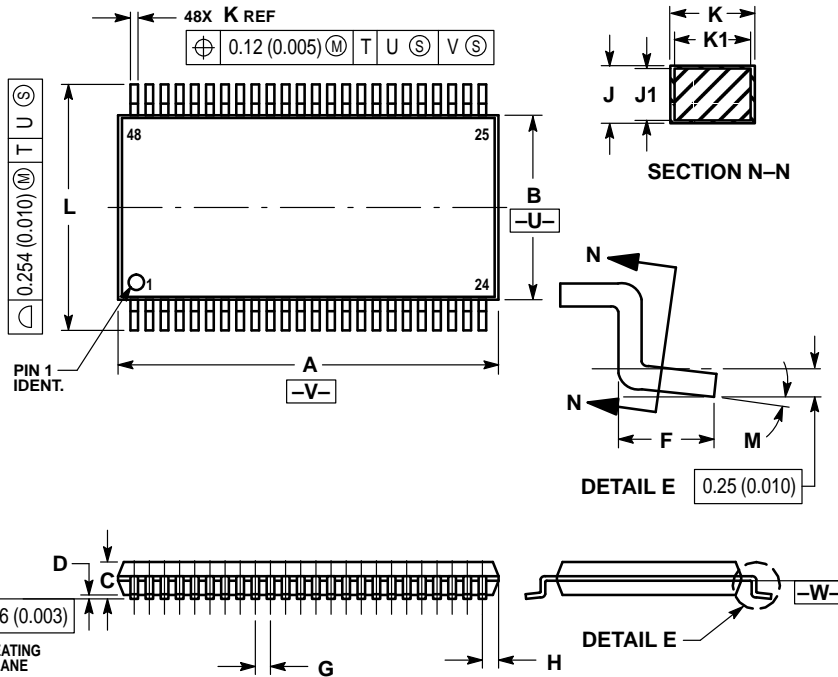
TEST	SWITCH
tPLH, tPHL	Open
tPZL, tPLZ	6V at VCC = 3.3 ±0.3V; VCC × 2 at VCC = 2.5 ±0.2V; 1.8V
tpZH, tpHZ	GND

CL = 30pF or equivalent (Includes jig and probe capacitance)
 RL = 500Ω or equivalent
 RT = ZOUT of pulse generator (typically 50Ω)

Figure 5. Test Circuit

OUTLINE DIMENSIONS

DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 1201-01
 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC	—	0.0197 BSC	—
H	0.37	—	0.015	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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