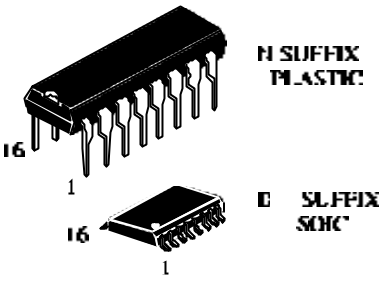
Presettable Up/Down Counter

High-Voltage Silicon-Gate CMOS



ORDERING INFORMATION
SL4516BN Plastic
SL4516BD SOIC
T_A = -55° to 125° C for all packages

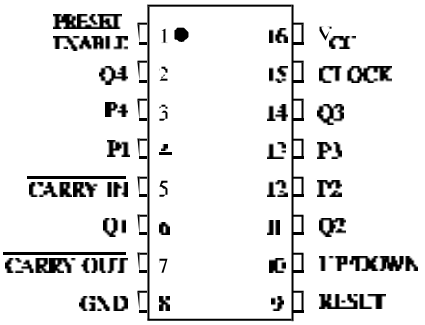
The SL4516B Presettable Binary Up/Down Counter consists of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. This counter can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line.

If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage.

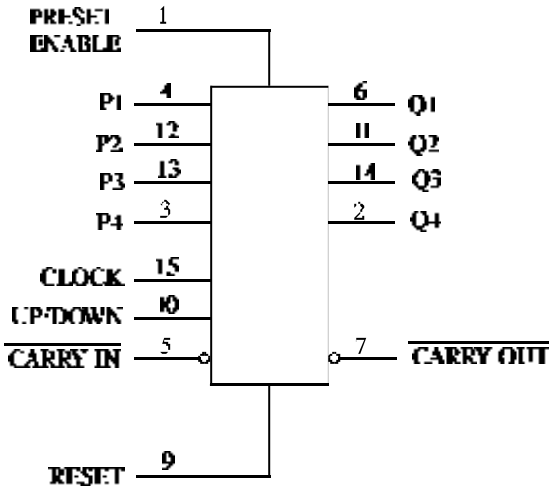
The SL4516B can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1.0 V min @ 5.0 V supply
  2.0 V min @ 10.0 V supply
  2.5 V min @ 15.0 V supply

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16=V_{CC}
PIN 8= GND

FUNCTION TABLE

Inputs					Outputs
CL	$\overline{CI}$	U/D	PE	R	Mode
X	H	X	L	L	NO COUNT
⎍	L	H	L	L	COUNT UP
⎍	L	L	L	L	COUNT DOWN
X	X	X	H	L	PRESET
X	X	X	X	H	RESET

X = don’ t care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125 °C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}= 0.5 V or V_{CC} - 0.5V V_{OUT}= 1.0 V or V_{CC} - 1.0 V V_{OUT}= 1.5 V or V_{CC} - 1.5V	5.0 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}= 0.5 V or V_{CC} - 0.5V V_{OUT}= 1.0 V or V_{CC} - 1.0 V V_{OUT}= 1.5 V or V_{CC} - 1.5V	5.0 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	5 10 20 100	5 10 20 100	150 300 600 3000	μA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} U_{OL}=0.4 V U_{OL}=0.5 V U_{OL}=1.5 V	 5.0 10 15	 0.64 1.6 4.2	 0.51 1.3 3.4	 0.36 0.9 2.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} U_{OH}=2.5 V U_{OH}=4.6 V U_{OH}=9.5 V U_{OH}=13.5 V	 5.0 5.0 10 15	 -2 -0.64 -1.6 -4.2	 -1.6 -0.51 -1.3 -3.4	 -1.15 -0.36 -0.9 -2.4	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=200kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q (Figure 1)	5.0 10 15	400 200 150	400 200 150	800 400 300	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Reset to Q (Figure 1)	5.0 10 15	420 210 160	420 210 160	840 420 320	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Carry Out (Figure 1)	5.0 10 15	480 240 180	480 240 180	960 480 360	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Carry In to Carry Out (Figure 1)	5.0 10 15	250 120 100	250 120 100	500 240 200	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Reset to Carry Out (Figure 1)	5.0 10 15	640 320 250	640 320 250	1280 640 500	ns
t_{THL}, t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS (C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
t_{su}	Minimum Setup Time, P to Preset Enable (Figure 1)	5.0 10 15	25 10 10	25 10 10	50 20 20	ns
t_{su}	Minimum Setup Time, Up/Down to Clock (Figure 1)	5.0 10 15				ns
t_{su}	Minimum Setup Time, Carry In to Clock (Figure 1)	5.0 10 15				ns
t_h	Minimum Hold Time, Clock to Carry In (Figure 1)	5.0 10 15	60 30 30	60 30 30	120 60 60	ns
t_h	Minimum Hold Time, Clock to Up/Down (Figure 1)	5.0 10 15	30 30 30	30 30 30	60 60 60	ns
t_h	Minimum Hold Time, Preset enable to P (Figure 1)	5.0 10	70 40	70 40	140 80	ns

		15	40	40	80	

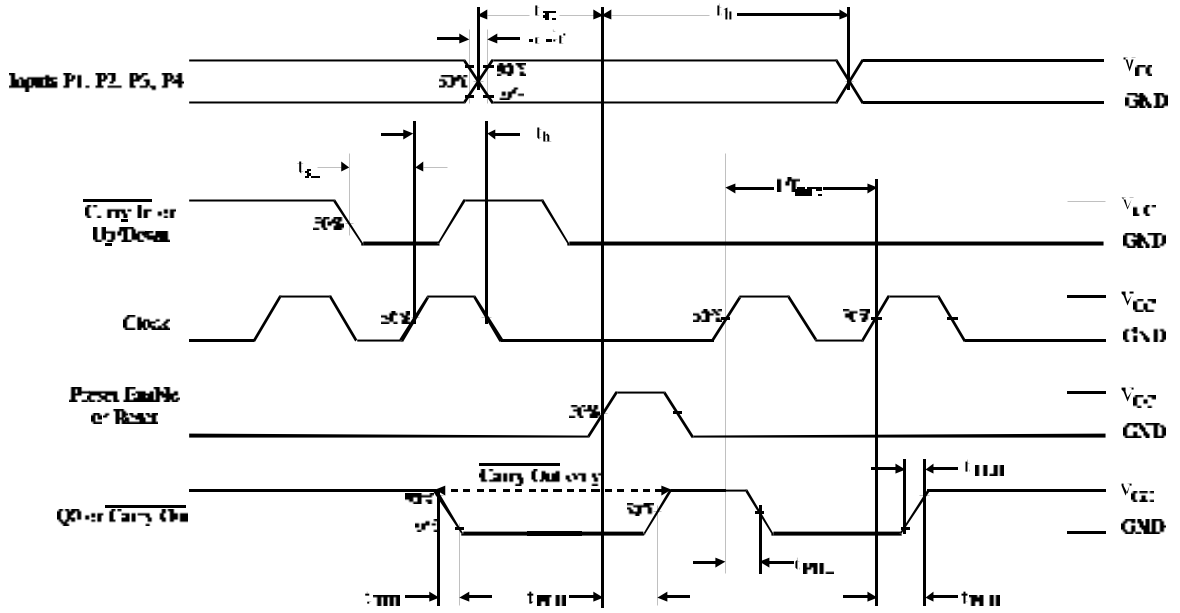
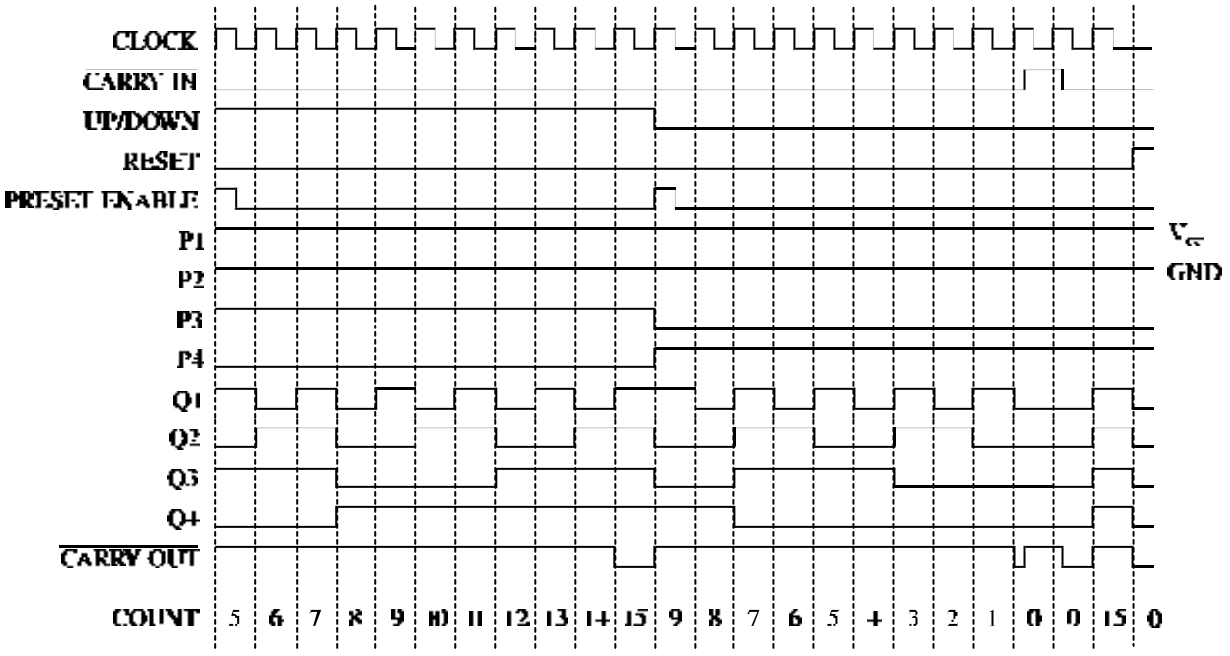


Figure 1. Switching Waveforms

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM